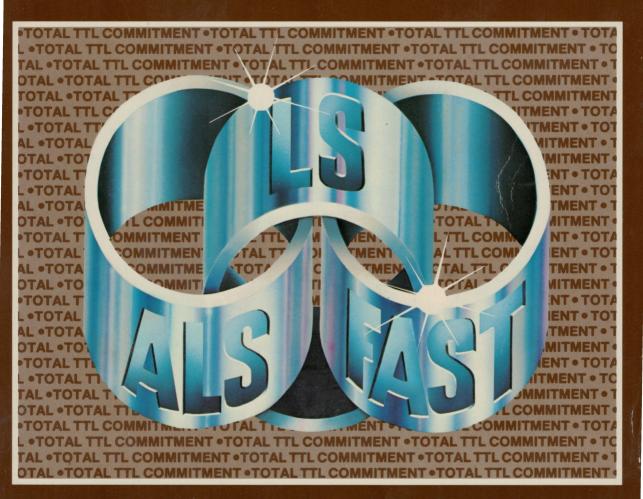
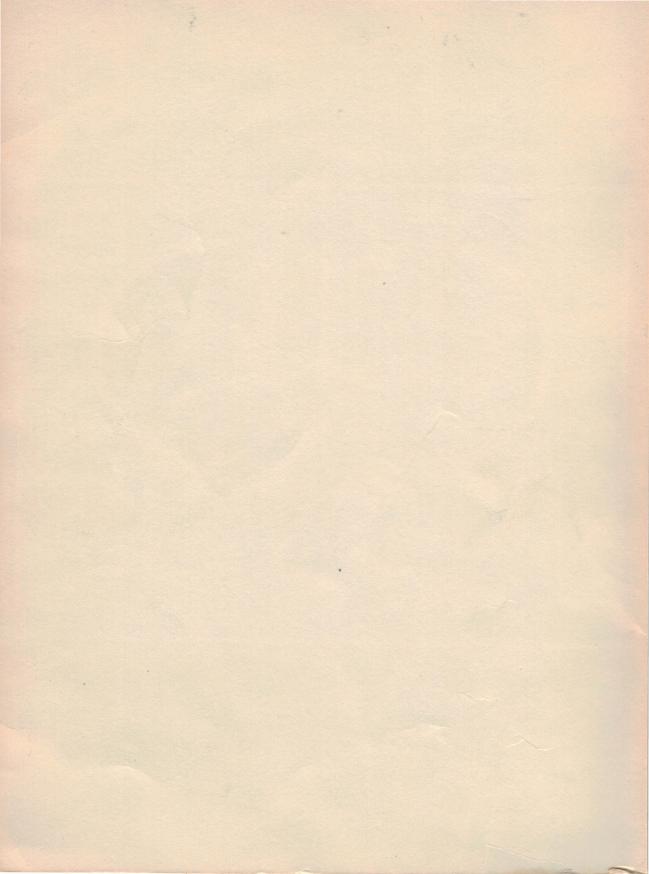


MOTOROLA INC.



SCHOTTKY TTL DATA



Selection	Infor	mation
L.	S/ALS	S/FAST

LS/FASI

Circuit Characteristics

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Design Considerations Symbol Definitions and Testing

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SCHOTTKY TTL

ALS Data Sheets

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FAST Data Sheets

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RAM/PROM Data Sheets

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SCHOTTKY TTL

Prepared by Technical Information Center

Low Power Schottky (LSTTL) has become the industry standard logic in recent years, replacing the original 7400 TTL with lower power and higher speeds. In addition to offering the standard LS TTL circuits, Motorola offers the Advanced Low Power Schottky TTL family (ALS) and the FAST Schottky TTL family. Complete specifications for each of these families are provided in data sheet form. Functional selector guides not only provide an overview of already introduced devices but planned introduction dates of new products.

This book also provides data sheets for TTL RAMs/PROMs and information regarding circuit characteristics, design considerations and testing, reliability data and package outlines.

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Device	Description		Page
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SN54LS/74LS12 SN54LS/74LS13 SN54LS/74LS14 SN54LS/74LS15 SN54LS/74LS20	Dual 4-Dual Schmitt Trigger Hex Schmitt Trigger Triple 3-Input AND Gate, Open-Co	Collector	
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SN54LS/74LS30 SN54LS/74LS32 SN54LS/74LS33 SN54LS/74LS37 SN54LS/74LS38	Quad 2-Input OR Gate Quad 2-Input NOR Buffer, Open-C Quad 2-Input NAND Buffer	Collector	

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SN54LS/74LS85 SN54LS/74LS86 SN54LS/74LS90 SN54LS/74LS91 SN54LS/74LS92	4-Bit Magnitude Comparator Quad Exclusive OR Gate Decade Counter 8-Bit Shift Register Divide-by-12 Counter	
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SN54LS/74LS244 SN54LS/74LS245 SN54LS/74LS247 SN54LS/74LS248 SN54LS/74LS249	Octal 3-State Driver, Noninverting	4-217 4-219 4-219
SN54LS/74LS251 SN54LS/74LS253 SN54LS/74LS256 SN54LS/74LS257A SN54LS/74LS258A	8-Input Multiplexer, 3-State Dual 4-Input Multiplexer, 3-State Dual 4-Bit Addressable Latch Quad 2-Input Multiplexer, 3-State Quad 2-Input Multiplexer, 3-State	
SN54LS/74LS259 SN54LS/74LS260 SN54LS/74LS266 SN54LS/74LS273 SN54LS/74LS279	8-Bit Addressable Latch (9334) Dual 5-Input NOR Gate Quad Exclusive NOR Gate, Open-Collector Octal D-Type Flip-Flop with Clear Quad Set-Reset Latch.	
SN54LS/74LS280 SN54LS/74LS283 SN54LS/74LS290 SN54LS/74LS293 SN54LS/74LS295A	9-Bit Odd/Even Parity Generator/Checker. 4-Bit Full Adder (Rotated LS83A) Decade Counter 4-Binary Counter 4-Bit Shift Register, 3-State.	
SN54LS/74LS298 SN54LS/74LS299 SN54LS/74LS322A SN54LS/74LS323 SN54LS/74LS348	Quad 2-Input Multiplexer with Output Register. 8-Bit Shift/Storage Register, 3-State. 8-Bit Shift Register with Sign Extend 8-Bit Universal Shift/Storage Register, 3-State 8-Input to 3-Line Priority Encoder, 3-State	
SN54LS/74LS352 SN54LS/74LS353 SN54LS/74LS365A SN54LS/74LS366A SN54LS/74LS367A	Dual 4-Input Multiplexer	
SN54LS/74LS368A SN54LS/74LS373 SN54LS/74LS374 SN54LS/74LS375 SN54LS/74LS377	Hex Inverter, 4-Bit and 2-Bit, 3-State Octal Transparent Latch, 3-State. Octal D-Type Flip-Flop, 3-State	

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SN54LS/74LS540 SN54LS/74LS541 SN54LS/74LS568 SN54LS/74LS569 SN54LS/74LS604	Octal Inverting Bus/Line Driver		4-318 4-318 4-321 4-321
SN54LS/74LS605 SN54LS/74LS606 SN54LS/74LS607 SN54LS/74LS620 SN54LS/74LS621	16-to-8 Multiplexer, Open Collector		4-326 4-326 4-330
SN54LS/74LS622 SN54LS/74LS623 SN54LS/74LS640 SN54LS/74LS641 SN54LS/74LS642	Octal Transceiver with Storage, Open-Colle Octal Transceiver with Storage, 3-State Octal Bus Transceiver with 3-State Output . Octal Bus Transceiver with 3-State Output . Octal Bus Transceiver with 3-State Output .		4-330 4-334 4-334
SN54LS/74LS643 SN54LS/74LS644 SN54LS/74LS645 SN54LS/74LS668 SN54LS/74LS669	Octal Bus Transceiver, True, Inverting, 3-Sta Octal Bus Transceiver, True, Inverting, Ope Octal Bus Transceiver with 3-State Output . Synchronous 4-Bit Up/Down Decade Count Synchronous 4-Bit Up/Down Binary Counte	n-Collectorer	4-334 4-334 4-338
SN54LS/74LS670 SN54LS/74LS673 SN54LS/74LS674 SN54LS/74LS682 SN54LS/74LS683	4 x 4 Register File, 3-State		4-347 4-347 4-351
SN54LS/74LS684 SN54LS/74LS685 SN54LS/74LS686 SN54LS/74LS687 SN54LS/74LS688	8-Bit Magnitude Comparator, 3-State 8-Bit Magnitude Comparator, Open-Collector 8-Bit Magnitude Comparator with Enable, 3 8-Bit Magnitude Comparator with Enable, C 8-Bit Magnitude Comparator, 3-State	rState -State pen-Collector	4-351 4-351 4-351
SN54LS/74LS689 SN54LS/74LS716 SN54LS/74LS718 SN74LS724 SN54LS/74LS748	8-Bit Magnitude Comparator, Open-Collector Programmable Decade Counter (MC4016) Programmable Binary Counter (MC4018) Voltage Controlled Oscillator		4-358 4-358 4-369
SN74LS783 SN54LS/74LS795 SN54LS/74LS796 SN54LS/74LS797 SN54LS/74LS798 SN54LS/74LS848	Synchronous Address Multiplexer (MC6883 Octal Buffer (81LS95), 3-State Octal Buffer (81LS96), 3-State Octal Buffer (81LS97), 3-State Octal Buffer (81LS98), 3-State 8-Input to 3-Line Priority Encoder, 3-State (6		4-397 4-397 4-397 4-397

Selection Information LS/ALS/FAST

SCHOTTKY TTL



GENERAL INFORMATION

TTL in Perspective

Since its introduction, TTL has become the most popular digital logic family. It has evolved from gold doped saturated logic, to Schottky clamped logic and finally to Advanced Schottky clamped logic. The popularity of TTL stems from its ease of use, low cost, medium-to-high speed operation, and good output drive capability.

Motorola offers three Schottky clamped TTL logic families — LS, ALS, and FAST™. All three families are pin and functionally compatible and can easily be combined in a system to achieve maximum performance at minimum cost

LS, Low-Power Schottky, is currently the largest and most popular of the three. It is low-cost and provides moderate speed at low power.

ALS, Advanced Low-Power Schottky, offers an im-

proved speed — power product compared to LS as a result of advanced MOSAIC (oxide isolated) processing. Other important features of ALS include improved noise margins, reduced input currents, and superior line driving characteristics.

FAST™, another advanced Schottky TTL line, offers a 20-to-30 percent improvement in speed over standard Schottky logic at about 20 percent of the power. As with ALS, FAST™ offers improved noise margins, reduced input currents and superior line driving characteristics. Additionally, FAST designs incorporate powerdown circuitry on three-state outputs, and buffered outputs on all storage devices. These design improvements provide the logic designer with additional flexibility and more reliable system operation.

TTL Family Comparisons

General Characteristics for Schottky TTL Logic

ALL MAXIMUM RATING	is)	Ĺ	s		ALS		FΔ	ST]
Characteristic Sy		54LSxxx	74LSxxx	54ALSxxx		Sxxx	54Fxxx	74Fxxx	Units
Operating Voltage Range	VCC	5 ± 10%	5 ± 5%	5 ± 10%	5 ± 10%	5 ± 5%	5 ± 10%	5 ± 5%	Vdc
Operating Temperature Range	ТА	– 55 to 125	0 to 70	– 55 to 125	0 to 70	0 to 70	- 55 to 125	0 to 70	°C
Input Current	IN IH	20	20	20	20	20	20	20	μА
	III IIL	- 400	- 400	- 100	- 100	- 100	- 600	- 600	μΑ
Output Drive	ЮН	-0.4	-0.4	- 0.4	- 0.4	-0.4	-1.0	- 1.0	mA
Standard Output	lOL	4.0	8.0	4.0	8.0	8.0	20	20	mA
	Isc	- 20 to - 100	- 20 to 100	- 25 to - 150	- 25 to - 150	- 25 to - 150	- 60 to - 150	- 60 to - 150	mA
	ЮН	- 12	- 15	- 12	- 15	- 15	- 12	- 15	mA
Buffer Output	lOL	12	24	12	24	24	48	64	mA
	Isc	-40 to -225	-40 to -225	-50 to -225	- 50 to - 225	- 50 to - 225	- 100 to - 225	- 100 to - 225	mA
Buffer Line Driving Capability:						,è			
Minimum R _t into 2.5 V		178	84	178	84	84	43	32	Ω
Minimum R _t into 5.0 V		381	189	381	189	189	95	71	Ω

Speed/Power Characteristics for Schottky TTL Logic⁽¹⁾

(ALL TYPICAL RATINGS)

Characteristic	Symbol	LS	ALS	FAST	Units
Quiescent Supply Current/Gate	IG	0.4	0.2	1.1	mA
Power/Gate (Quiescent)	PG	2.0	1.0	5.5	mW
Propagation Delay	tp	9.0	5.0	3.7	ns
Speed Power Product	_	18	5.0	19.2	рЈ
Clock Frequency (D-F/F)	fmax	33	35	125	MHz
Clock Frequency (Counter)	fmax	40	45	125	MHz

NOTES: 1. Specifications are shown for the following conditions

a) $V_{CC} = 5.0 \text{ Vdc (AC)}$;

b) $T_A = 25^{\circ}C$

c) CL = 50 pF for ALS, FAST; 15 pF for LS

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High Performance ALS-TTL-Compatible Macrocell Arrays

In addition to standard logic lines, Motorola also offers a variety of TTL-compatible Macrocell Arrays. These products provide a means for developing economical custom LSI/VLSI logic circuits. Performance is achieved by the combination of an advanced MOSAIC I (Motorola Oxide-Isolated Self-Aligned Implanted Circuit) oxide isolated bipolar integrated circuit process and a series gated emitter-coupled logic (ECL) macrocell circuit technology. Input and output circuits provide level translation to and from the internal array logic for standard TTL/MOS interface.

Each cell within the arrays contains a number of unconnected transistors and resistors. Stored within a computer are the specifications to automatically interconnect these elements forming SSI/MSI logic cells (rather than simple gates) called macrocells. These macrocells take the form of standard logic blocks such as dual type D flip-flops, dual full adders, quad latches and many other pre-defined "library" functions. Presently, the macrocell library for the ALS-TTL arrays contains more than 80 logic functions.

Generating an LSI/VLSI design is simply a matter of selecting the appropriate macrocells and describing the proper interconnection network to implement the design. Motorola's CAD (Computer-Aided-Design) interface provides automatic placement and routing of the cells (intraconnection of the cell itself is automatically accomplished when placed), full logic and fault-testing

MCA500ALS MCA1300ALS MCA2800ALS

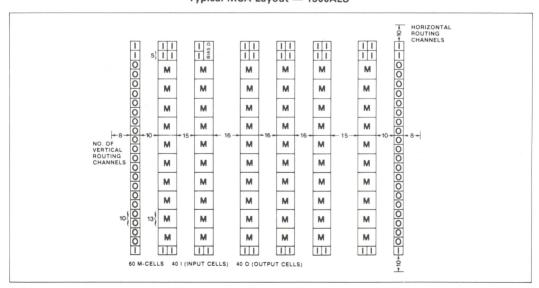
capabilities, AC delay simulations, generation of test tapes and custom metallization to complete the IC processing sequence.

The ability to stockpile fully diffused wafers provides a very fast turnaround time (the time from customer notification of a completed design to delivery of finished parts) of currently nine weeks.

ALS-TTL MCA Selection Chart

	MCA 500ALS	MCA 1300ALS	MCA 2800ALS
Configuration Max Gate Equivalent Major Macrocells I/O Ports Input/Interface Cells Output Macrocells	533 24 57 26 24	1280 60 76 40 40	2720 130 120
Performance Max Gate Delay (M Cell) Max Toggle Frequency	4.0 ns 80 MHz	3.0 ns 80 MHz	1.1 ns 125 MHz
Maximum Power Dissipation	1.0 W	1.4 W	2.5 W
Packages Dual-In-Line Chip Carrier	28, 40, 48 68	40, 48 68, 84	_ 149PG
Temperature Range	0-70°C	0-70°C	0-70°C
Supply Voltage	5.0 V ±5%	5.0 V ±5%	5.0 V ± 5%
Availability	Now	Now	Now

Typical MCA Layout — 1300ALS



LS TTL

SN54LS00 Series (-55 to +125°C) SN74LS00 Series (0 to +70°C)

Suffix: N . . . Plastic (only 74-series)
J . . . Ceramic (54/74 series)

Device	Function	Samples	Pins
LS00	Quad 2-Input NAND Gate	А	14
LS01	Quad 2-Input NAND Gate, Open-Collector	A	14
LS02	Quad 2-Input NOR Gate	A	14
LS03	Quad 2-Input NAND Gate, Open-Collector	- A	14
LS04	Hex Inverter	A	14
LS05	Hex Inverter, Open-Collector	А	14
LS08	Quad 2-Input AND Gate	Α	14
LS09	Quad 2-Input AND Gate, Open-Collector	Α	14
LS10	Triple 3-Input NAND Gate	Α	14
LS11	Triple 3-Input AND Gate	А	14
LS12	Triple 3-Input NAND Gate, Open-Collector	Α	14
LS13	Dual 4-Input Schmitt Trigger	A	14
LS14	Hex Schmitt Trigger	А	14
LS15	Triple 3-Input AND Gate, Open-Collector	А	14
LS20	Dual 4-Input NAND Gate	A	14
LS21	Dual 4-Input AND Gate	Α	14
LS22	Dual 4-Input NAND Gate, Open-Collector	A	14
LS26	Quad 2-Input NAND, High Voltage	Α	14
LS27	Triple 3-Input NOR Gate	Α	14
LS28	Quad 2-Input NOR Buffer	A	14
LS30	8-Input NAND Gate	A	14
LS32	Quad 2-Input OR Gate	A	14
LS32	Quad 2-Input NOR Buffer, Open-Collector	A	14
LS37	Quad 2-Input NAND Buffer	A	14
LS38	Quad 2-Input NAND Buffer, Open-Collector		14
LS40	Dual 4-Input NAND Buffer	A	14
LS42	1-of-10 Decoder	A	16
LS47	BCD to 7-Segment Decoder/Driver,		
L34/	Open-Collector	A	16
LS48	BCD to 7-Segment Decoder/Driver,		'
L340	with Pull-Ups	A	16
LS49	BCD to 7-Segment Decoder/Driver,		10
L549	Open-Collector	A	16
LS51	Dual AND-OR-INVERT Gate	A	14
LS54	3-2-2-3 Input AND-OR-INVERT Gate	A	14
LS54 LS55	2-Wide 4-Input AND-OR-INVERT Gate	A	14
LS73A	Dual JK Flip-Flop	A	14
LS73A LS74A	Dual D Flip-Flop	A	14
LS74A LS75	4-Bit Bi-Stable Latch with Q and Q	A	16
LS76A	Dual JK Flip-Flop	A	16
LS76A	4-Bit Bi-Stable Latch	A	14
LS77	Dual JK Flip-Flop with Preset	A	14
LS83A	4-Bit Full Adder	A	16
LS83A LS85	4-Bit Magnitude Comparator	A	16
LS85	Quad Exclusive OR Gate	A	14
L380	Quad Exclusive On Gate	_ ^	14

Device	Function	Samples	Pins
LS90	Decade Counter	Α .	14
LS91	8-Bit Shift Register Serial-In/Serial-Out	A	14
LS92	Divide-By-12 Counter	A	14
LS93	4-Bit Binary Counter	A	14
LS95B	4-Bit Shift Register	A	14
LS107A	Dual JK Flip-Flop with Clear	A	14
LS109A	Dual JK Flip-Flop with Preset	Α	16
LS112A	Dual JK Edge-Triggered Flip-Flop	Α	16
LS113A	Dual JK Edge-Triggered Flip-Flop	A	14
LS114A	Dual JK Edge-Triggered Flip-Flop	Α	14
LS122	Retriggerable Monostable Multivibrator	A	14
LS123	Dual Retriggerable Monostable		
	Multivibrator	A	16
LS125A	Quad Buffer, Low Enable, 3-State	A	14
LS126A	Quad Buffer, High Enable, 3-State	Α .	14
LS132	Quad 2-Input Schmitt Trigger	Α	14
LS133	13-Input NAND Gate	Α	16
LS136	Quad Exclusive OR Gate, Open-Collector	Α	14
LS137	3-Line to 8-Line Decoder/Demultiplexer	A	16
LS138	1-of-8 Decoder/Demultiplexer	A	16
LS139	Dual 1-of-4 Decoder/Demultiplexer	A	16
LS145	1-of-10 Decoder/Driver, Open-Collector	A	16
LS147	10-Line Decimal to 4-Line Priority Encoder	A	16
LS148	8-Input to 3-Line Priority Encoder	A	16
LS151	8-Input Multiplexer	A	16
LS153	Dual 4-Input Multiplexer	A	16
LS155	Dual 1-of-4 Decoder	A	16
LS155 LS156	Dual 1-of-4 Decoder, Open-Collector	A	16
LS150	Quad 2-Input Multiplexer, Non-Inverting	A	16
LS157	Quad 2-Input Multiplexer, Non-Inverting	A	16
LS160	BCD Decade Counter, Asynchronous Reset	Α	10
LS160 LS161A	(9310 Type)	А	16
LSIBIA	4-Bit Binary Counter, Asynchronous Reset		4.0
	(9316 Type)	A	16
LS162A	BCD Decade Counter, Synchronous Reset	A	16
LS163A	4-Bit Binary Counter, Synchronous Reset	A	16
LS164	8-Bit Serial-In/Parallel-Out Shift Register	A	14
LS165	8-Bit Parallel-In/Serial-Out Shift Register	A	16
LS166	8-Bit Parallel-In/Serial-Out Shift Register	A	16
LS168	Up/Down Decade Counter	A	16
LS169	Up/Down Binary Counter	A	16
LS170	4 x 4 Register File, Open-Collector	A	16
LS173A	4-Bit D Register, 3-State	A	16
LS174	Hex D Flip-Flop with Clear	A	16
LS175	Quad D Flip-Flop with Clear	A	16
LS181	4-Bit ALU	A	24
LS182	Look Ahead Carry Generator	A	16
LS183	Dual Carry/Save Full Adder	A	14
LS190	Up/Down Decade Counter	A	16
LS191	Up/Down Binary Counter	A	16
LS192	Up/Down Decade Counter with Clear	A	16
LS193	Up/Down Binary Counter with Clear	A	16
LS194A	4-Bit Right/Left Shift Register	A	16
LS195A LS196	4-Bit Shift Register (9300 Type) Decade Counter, Asynchronously	A	16
LS197	Presettable 4-Bit Binary Counter, Asynchronously Presettable	A	14
	Liesellanie	Α	14

A = Announced

Device	Function	Samples	Pins
LS221	Dual One-Shot (Very Stable)	Α	16
LS240	Octal Bus/Line Driver, Inverting 3-State	Α	20
LS241	Octal Bus/Line Driver, 3-State	A	20
LS242	Quad Bus Transceiver, Inverting, 3-State	Α	14
LS243	Quad Bus Transceiver, Non-Inverting, 3-State	A	14
LS244	Octal Driver, Non-Inverting, 3-State	A	20
LS245	Octal Bus Transceiver, Non-Inverting, 3-State	A	20
LS247	BCD to 7-Segment Decoder/Driver, Open-Collector	A	16
LS248	BCD to 7-Segment Decoder/Driver with Pull-Ups	A	16
LS249	BCD to 7-Segment Decoder/Driver,		
	Open-Collector	A	16
LS251	8-Input Multiplexer, 3-State	Α	16
LS253	Dual 4-Input Multiplexer, 3-State	Α	16
LS256 LS257A	Dual 4-Bit Addressable Latch Quad 2-Input Multiplexer, Non-Inverting,	A	16
	3-State	Α	16
LS258A	Quad 2-Input Multiplexer, Inverting 3-State	A	16
LS259	8-Bit Addressable Latch (9334)	Α	16
LS260	Dual 5-Input NOR Gate	Α	14
LS266	Quad Exclusive NOR Gate, Open-Collector	Α	14
LS273	Octal D Flip-Flop with Clear	A	20
LS279	Quad Set/Reset Latch	A	16
LS280	8-Bit Odd/Even Parity Generator/Checker	A	14
LS283	4-Bit Full Adder (Rotated LS83A)	A	16
		A	14
LS290	Decade Counter (Divide By 2 and 5)	A	16
LS293	4-Bit Binary Counter		
LS295A	4-Bit Shift Register, 3-State	A	14
LS298	Quad 2-Multiplexer, with Output Register	Α	16
LS299 LS322A	8-Bit Shift/Storage Register, 3-State 8-Bit Shift Register with Sign Extend,	Α	20
	3-State	Α	20
LS323	8-Bit Shift/Storage Register, 3-State	A	20
LS348	8-Input to 3-Line Priority Encoder, 3-State	Α	16
LS352	Dual 4-Multiplexer (Inverting LS153)	Α	16
LS353	Dual 4-Multiplexer (3-State LS352)	Α	16
LS365A	Hex Buffer, Common Enable, 3-State	Α	16
LS366A	Hex Inverter, Common Enable, 3-State	Α	16
LS367A	Hex Buffer, 4-Bit and 2-Bit, 3-State	Α	16
LS368A	Hex Inverter, 4-Bit and 2-Bit, 3-State	Α	16
LS373	Octal Transparent Latch, 3-State	A	20
LS374	Octal D Flip-Flop, 3-State	A	20
LS374	Quad Latch	A	16
LS375	Octal D Flip-Flop with Enable	A	20
		A	16
LS378	Hex D Flip-Flop with Enable	A	16
LS379	4-Bit D Flip-Flop with Enable	A	20
LS385	Quad 4-Bit Adder/Subtractor		
LS386	2-Input Quad/Exclusive OR Gate	A	14
LS390	Dual Decade Counter	A	16
LS393	Dual 4-Bit Binary Counter	Α	14
LS395 LS398	4-Bit Shift Register, 3-State Quad 2-Input Multiplexer with Output	A	16
LS399	Register Quad 2-Input Multiplexer with Output	Α	20
	Register	A	16

Device	Function	Samples	Pins
LS490	Dual Decade Counter	Α	16
LS540	Octal Buffer/Line Driver, 3-State	A	20
LS541	Octal Buffer/Line Driver, 3-State	A	20
LS568	Decade Up/Down Counter, 3-State	A	20
LS569	Binary Up/Down Counter, 3-State	Α	20
LS604	16-to-8 Multiplexer, 3-State	A	28
LS605	16-to-8 Multiplexer, Open-Collector	A	28
LS606	16-to-8 Multiplexer, 3-State	A	28
LS607	16-to-8 Multiplexer, Open-Collector	Â	28
LS620	Octal Transceiver with Storage, 3-State	Â	20
LS621	Octal Transceiver with Storage,	A	
LS622	Open-Collector Octal Transceiver with Storage,	A	20
	Open-Collector	A	20
LS623	Octal Transceiver with Storage, 3-State	A	20
LS640	Octal Bus Transceiver, Inverting, 3-State	A	20
LS641	Octal Bus Transceiver, Mon-Inverting, Open-Collector	A	20
LS642	Octal Bus Transceiver, Inverting,	A	20
	Open-Collector	A	20
LS643	Octal Bus Transceiver, True, Inverting,		
	3-State	А	20
LS644	Octal Bus Transceiver, True, Inverting, Open-Collector	A	20
LS645	Octal Bus Transceiver, Non-Inverting,		2.0
L3045	3-State	Α	20
LS668	Synchronous 4-Bit Up/Down Decade		
	Counter	A	16
LS669	Synchronous 4-Bit Up/Down Binary		,,,
L3003	Counter	A	16
LS670		A	16
	4 x 4 Register File, 3-State	A	10
LS673	16-Bit Serial-In/Serial-Out Shift Register, 3-State	A	24
LS674	16-Bit Parallel-In/Serial-Out Shift Register,		
L0074	3-State	A	24
LS682	8-Bit Magnitude Comparator	A	20
LS683		_ A	20
L5683	8-Bit Magnitude Comparator,		20
	Open-Collector	A	20
LS684	8-Bit Magnitude Comparator	Α	20
LS685	8-Bit Magnitude Comparator,		
	Open-Collector	A	20
LS686	8-Bit Magnitude Comparator with Enable	A	24
LS687	8-Bit Magnitude Comparator with Enable	A	24
LS688	8-Bit Magnitude Comparator	A	20
LS689	8-Bit Magnitude Comparator, Open-Collector	A	20
LS716	Programmable Decade Counter (MC4016)	A	16
LS718	Programmable Binary Counter (MC4018)	A	16
LS716 LS724	Voltage Controlled Multivibrator	Ä	8
		A	16
LS748	8-Input to 3-Line Priority Encoder	A	10
LS783*	Synchronous Address Multiplexer (MC6883)	A	40
LS795	Octal Buffer (81LS95), 3-State	A	20
	Octal Buffer (81LS96), 3-State	A	20
	Octal Dallel (O'LOSO), S-Otate		
	Octal Ruffer (811 S97) 2 State	Δ	20
LS796 LS797 LS798	Octal Buffer (81LS97), 3-State Octal Buffer (81LS98), 3-State	A	20

^{*74}LS only.

FAST TTL

MC54F00 Series (-55 to +125°C) MC74F00 Series (0 to +70°C)

Suffix: N... Plastic (only 74-series)
J... Ceramic (54/74 series)

Device	Function	Samples	Pins
F00	Quad 2-Input NAND Gate	А	14
F02	Quad 2-Input NOR Gate	Α	14
F04	Hex Inverter	Α	14
F08	Quad 2-Input AND Gate	Α	14
F10	Triple 3-Input NAND Gate	Α	14
F11	Triple 3-Input AND Gate	Α	14
F20	Dual 4-Input NAND Gate	Α	14
F32	Quad 2-Input OR Gate	Α	14
F64	4-2-2-3 Input AND-OR-INVERT Gate	А	14
F74	Dual D Flip-Flop	Α	14
F86	Quad Ex/OR Gate	3Q83	14
F109	Dual J-K Flip-Flop w/Preset	Α	16
F112	Dual J-K Flip-Flop	3Q83	16
F113	Dual J-K Flip-Flop	3083	14
F114	Dual J-K Flip-Flop	3083	14
F138	1-of-8 Decoder/Demultiplexer	3Q83	16
F139	Dual 1-of-4 Decoder/Demultiplexer	3Q83	16
F151	8-Input Multiplexer	4Q83	16
F153	Dual 4-Input Multiplexer	Α	16
F157	Quad 2-Input Multiplexer	4Q83	16
F158	Quad 2-Input Multiplexer	4Q83	16
F160	BCD Decade Counter, Asynchronous Reset	4083	16
F161	4-Bit Binary Counter, Asynchronous Reset	4Q83	16
F162	BCD Decade Counter, Synchronous Reset	4083	16
F163	4-Bit Binary Counter, Synchronous Reset	4Q83	16
F168	Up/Down Decade Counter	1H84	16
F169	Up/Down Binary Counter	1H84	16
F174	Hex D Flip-Flop	3Q83	16
F175	Quad D Flip-Flop	3Q83	16
F181	4-Bit ALU	1H84	24
F182	Look Ahead Carry Generator	1H84	16
F189	64-Bit RAM/3-State	2H84	16
F190	Up/Down Decade Counter	4Q83	16
F191	Up/Down Binary Counter	4Q83	16
F192	Up/Down Decade Counter with Clear	4083	16
F193	Up/Down Binary Counter with Clear	4Q83	16
F194	Universal Shift Register	4Q83	16
F195	4-Bit Shift Register	4Q83	16
F240	Octal Bus/Line Driver/Inverting/3-State	Α	20
F241	Octal Bus/Line Driver/3-State	A	20
F242	Quad Bus Transceiver/Inverting/3-State	A	14
F243	Quad Bus Transceiver/Non-Inverting/		
	3-State	A	14
F244	Octal Bus Driver/Non-Inverting/3-State	A	20
F245	Octal Bus Transceiver	A	20
F251	8-Input Multiplexer/3-State	4Q83	16
F253	Dual 4-Input Multiplexer/3-State	A	16
F257	Quad 2-Input Multiplexer/3-State	4Q83	16
F258	Quad 2-Input Multiplexer, Inverting/3-State	4Q83	16
F280	9-Bit Odd/Even Parity Gen/Checker	2H84	14
F283	4-Bit Full Adder	2H84	20
F289	64-Bit RAM, Open-Collector	2H84	16
F299	8-Bit Shift/Store Register	1H84	20
F323	8-Bit Universal Shift/Storage Register	1H84	20
F350	4-Bit Shifter/3-State	1H84	16
F352	Dual 4-Input Multiplexer	A	16
F353	Dual 4-Input Multiplexer/3-State	A	20

Device	Function	Samples	Pins
F373	Octal Transparent Latch/3-State	3Q83	16
F374	Octal D Flip-Flop/3-State	Α	16
F378	Hex Parallel D Register w/Enable	3Q83	20
F379	Quad Parallel Register w/Enable	3Q83	20
F381	4-Bit ALU	1H84	20
F382	4-Bit ALU	1H84	20
F521	Octal Comparitor	1Q84	20
F533	Octal Transparent Latch/3-State	Α	20
F534	Octal D Flip-Flop/3-State	Α	20
F537	1-of-10 Decoder/3-State	1H84	20
F538	1-of-8 Decoder/3-State	1H84	20
F539	1-of-4 Decoder/3-State	1H84	20
F620	Octal Bus Transceiver/Inverting/3-State	3083	20
F623	Octal Bus Transceiver/3-State	3083	20
F640	Octal Bus Transceiver/Inverting/3-State	3083	20
F643	Octal Bus Transceiver/Inverting/True/		
	3-State	3083	20
F2960	Error Detection and Correction Unit (EDAC)	3083	48
F2961	EDAC Bus Buffer, Inverting	1H84	24
F2962	EDAC Bus Buffer, Non-Inverting	1H84	24
F2968	Dynamic Memory Controller	4Q83	48
F2969	Memory Timing Controller w/EDAC	4Q83	48
F2970	Memory Timing Controller w/o EDAC	4Q83	24

ALS TTL

SN54ALS00 Series (-55 to +125°C) SN74ALS00 Series (0 to +70°C)

Suffix: N... Plastic (only 74-series)
J... Ceramic (54/74 series)

Device	Function	Samples	Pins
ALS00	Quad 2-Input NAND Gate	Α	14
ALS01	Quad 2-Input NAND Gate, Open-Collector	4Q83	14
ALS02	Quad 2-Input NOR Gate	Α	14
ALS03	Quad 2-Input NAND Gate, Open-Collector	A	14
ALS04	Hex Inverter	A	14
ALS05	Hex Inverter, Open-Collector	A	14
ALS08	Quad 2-Input AND Gate	A	14
ALS09	Quad 2-Input AND Gate, Open-Collector	A	14
ALS10	Triple 3-Input NAND Gate	A	14
ALS11	Triple 3-Input AND Gate	A	14
ALS12	Triple 3-Input NAND Gate, Open-Collector	A	14
ALS13	Dual 4-Input Schmitt Trigger	4Q83	14
ALS14	Hex Schmitt Trigger	4Q83	14
ALS15	Triple 3-Input NAND Gate, Open-Collector	Α	14
ALS20	Dual 4-Input NAND Gate	A	14
ALS21	Dual 4-Input AND Gate	A	14
ALS22	Dual 4-Input NAND Gate, Open-Collector	A	14
ALS27	Triple 3-Input NOR Gate	Α .	14
ALS28	Quad 2-Input NOR Buffer	4Q83	14
ALS32	Quad 2-Input OR Gate	4Q83	14
ALS33	Quad 2-Input NOR Buffer, Open-Collector	4Q83	14

Device	Function	Samples	Pins
ALS37	Quad 2-Input NAND Buffer	Α	14
ALS38	Quad 2-Input NAND Buffer, Open-Collector	Α	14
ALS40	Dual 4-Input NAND Buffer	4Q83	14
ALS51	Dual 2-Wide, 2-3-Input AND-OR-INVERT		
	Gate	Α	14
ALS55	2-Wide, 4-Input AND-OR-INVERT Gate	Α	14
ALS74	Dual D Flip-Flop	Α	14
ALS91	8-Bit Serial-In/Serial-Out Shift Register	1H84	14
ALS109	Dual J-K Flip-Flop w/Preset	4Q83	16
ALS132	Quad 2-Input Schmitt Trigger	4Q83	14
ALS138	1-of-8 Decoder/Demultiplexer	4Q83	16
ALS139	Dual 1-of-4 Decoder/Demultiplexer	4Q83	16
ALS151	8-Input Multiplexer	3Q83	16
ALS153	Dual 4-Input Multiplexer	1Q84	16
ALS157	Quad 2-Input Multiplexer/Non-Inverting	А	16
ALS158	Quad 2-Input Multiplexer/Inverting	A	16
ALS160	BCD Decade Counter/Asynchronous Reset		
ALOTOO	(9310 Type)	Α	16
ALS161	4-Bit Binary Counter, Asynchronous Reset		10
ALOTOT	(9316 Type)	Α	16
ALS162	BCD Decade Counter/Synchronous Reset	A	16
ALS 162 ALS 163	4-Bit Binary Counter/Synchronous Reset	A	16
ALS 163 ALS 164	8-Bit Serial-In/Parallel-Out Shift Register	1H84	14
		11104	14
ALS168	4-Bit Up/Down Decade Counter/	4000	4.0
	Synchronous Reset	4Q83	16
ALS169	4-Bit Up/Down Binary Counter/		
	Synchronous Reset	4Q83	16
ALS190	Up/Down Decade Counter	Α	16
ALS191	Up/Down Binary Counter	Α	16
ALS192	Up/Down Decade Counter w/Clear	Α	16
ALS193	Up/Down Binary Counter w/Clear	Α	16
ALS238	1-of-8 Decoder/Demultiplexer/(Active High)	4Q83	16
ALS239	Dual 1-of-4 Decoder/Demultiplexer/		
	(Active High)	4Q83	16
ALS240	Octal Bus/Line Driver/Inverting/3-State	Α	20
ALS241	Octal Bus/Line Driver/3-State	Α	20
ALS242	Quad Bus Transceiver/Inverting/3-State	А	14
ALS243	Quad Bus Transceiver/Non-Inverting/		
	3-State	Α	14
ALS244	Octal Driver/Non-Inverting/3-State	A	20
ALS245	Octal Bus Transceiver/Non-Inverting/		
7120240	3-State	Α	20
ALS251	8-Input Multiplexer/3-State	3Q83	16
ALS253	Dual 4-Input Multiplexer/3-State	1H84	16
ALS253	Quad 2-Input Multiplexer/Non-Inverting/	11104	10
AL3237	3-State	1H84	16
ALS258	Quad 2-Input Multiplexer/Inverting/3-State	1H84	16
ALS258 ALS273	Octal D Flip-Flop w/Clear	A	20
ALS273 ALS352		1H84	16
	Dual 4-Multiplexer/Inverting ALS153	1H84	16
ALS353	Dual 4-Multiplexer/3-State ALS352		
ALS373	Octal Transparent Latch/3-State	3Q83	20
ALS374	Octal D Flip-Flop/3-State	3083	20
ALS377	Octal D Flip-Flop w/Enable	A	20
ALS533	Octal Transparent Latch/Inverting	1H84	20
ALS534	Octal D-Type Flip-Flop/Inverting	1H84	20
ALS537	1-of-10 Decoder/3-State	1H84	20
ALS538	1-of-8 Decoder/3-State	1H84	20
ALS539	Dual 1-of-4 Decoder/3-State	1H84	20
ALS540	Octal Buffer/3-State	4Q83	20
ALS541	Octal Buffer/3-State	4Q83	20
ALS560	4-Bit Decade Counter 3-State	Α	20
	4-Bit Binary Counter/3-State	Α	20
ALS561	8-Bit Latch/3-State	1H84	20
			20
ALS563	Octal D Flip-Flop/3-State	1H84	
ALS563 ALS564	Octal D Flip-Flop/3-State	1H84 4Q83	
ALS563 ALS564 ALS568	Decade Up/Down Counter 3-State	4Q83	20
ALS563 ALS564			20

ALS575		Samples	Pins
	Octal D Flip-Flop/Synchronous Clear/		
	3-State	1H84	20
ALS576	Octal D Flip-Flop/Inverting/3-State	1H84	20
ALS577	Octal D Flip-Flop/Inverting/Synchronous		
	Clear/3-State	1H84	20
ALS580	Octal Transparent Latch/Inverting/3-State	1H84	20
ALS620	Octal Transceiver w/Storage/3-State	A	20
ALS621	Octal Transceiver w/Storage/	Α	
41.0000	Open-Collector	А	20
ALS622	Octal Transceiver w/ Storage/ Open-Collector	Α	20
ALS623	Octal Transceiver w/Storage/3-State	A	20
ALS623 ALS638	Octal Transceiver W/Storage/3-State Octal Bus Transceiver/Inverting/3-State	A	20
ALS639	Octal Bus Transceiver/3-State	Δ	20
ALS640	Octal Bus Transceiver/Inverting/3-State	A	20
ALS641	Octal Bus Transceiver/Non-Inverting/	^	20
AL3041	Open-Collector	Α	20
ALS642	Octal Bus Transceiver/Inverting/		20
AL0042	Open-Collector	А	20
ALS643	Octal Bus TransceiverTrue/Inverting/3-State	, ,	20
ALS644	Octal Bus Transceiver/True/Inverting/		20
ALGOTT	Open-Collector	Α	20
ALS646	Octal Transceiver/Latch/Multiplexer/		20
AL3040	Non-Inverting/3-State	1H84	24
ALS647	Octal Transceiver/Latch/Multiplexer/	11104	24
AL3047	Non-Inverting/Open-Collector	1H84	24
ALS648	Octal Transceiver/Latch/Multiplexer/	11104	24
AL3040	Inverting/3-State	1H84	24
ALS649	Octal Transceiver/Latch/Multiplexer/	11104	24
AL3043	Inverting/Open-Collector	1H84	24
ALS651	Octal Bus Transceiver/Register/3-State	1H84	24
ALS652	Octal Bus Transceiver/Register/3-State	1H84	24
ALS653	Octal Bus Transceiver/Register	1H84	24
ALS654	Octal Bus Transceiver/Register	1H84	24
ALS671	Bidirectional Shift Register/Latch/	11104	24
ALGOVI	Multiplexer/3-State	4Q83	20
ALS672	Bidirectional Shift Register/Latch/	4000	
	Multiplexer/3-State	4Q83	20
ALS690	Decade Counter/Latch/Multiplexer/		
	Asynchronous Reset/3-State	Α	20
ALS691	Binary Counter/Latch/Multiplexer/	1.6	
	Asynchronous Reset/3-State	Α	20
ALS692	Decade Counter/Latch/Multiplexer/		
	Synchronous Reset/3-State	Α	20
ALS693	Binary Counter/Latch/Multiplexer/		
	Synchronous Reset/3-State	Α	20
ALS694	Decade Counter/Latch/Multiplexer/		
	Synchronous/Asynchronous Reset/		
	3-State	Α	20
ALS695	Binary Counter/Latch/Multiplexer/		
	Synchronous/Asynchronous Reset/		
	3-State	Α	20
ALS696	Decade Counter/Register/Multiplexer/		
	3-State	4Q83	20
ALS697	Binary Counter/Register/Multiplexer/3-State	4Q83	20
ALS698	Decade Counter/Register/Multiplexer/		
	3-State	4Q83	20
ALS699	Binary Counter/Register/Multiplexer/3-State	4Q83	20
ALS790	Error Detection and Correction Circuit	see	
		F2960	
ALS873	Octal Transparent Latch	2H84	24
ALS874	Octal D Flip-Flop	2H84	24
ALS876	Octal D Flip-Flop/Inverting	2H84	24
ALS878	Dual 4-Bit D Flip-Flop/Synchronous Clear		
	3-State	2H84	24
ALS879	Dual 4-Bit D Flip-Flop Inverting		
		2H84 2H84	24 24

TTL Memories

MCM76xxx Series PROM MCM93xxx Series RAM

*Suffix: D . . . Ceramic DIP

P... Plastic DIP

C... 0 to $+75^{\circ}$ C (Commercial) M... -55 to $+125^{\circ}$ C (Military)

*Example: MCM7621DC, MCM7621DM, etc.

Device	Function	T _A A (ns)	Samples	Pins
MCM27S25	512 x 8 PROM, 3-State, Registered	30/15*	2Q84	24
MCM27S27	512 x 8 PROM, 3-State, Registered	35/20*	2Q84	22
MCM27S35	1k x 8 PROM, 3-State, Registered	35/20*	2Q84	24
MCM27S37	1k x 8 PROM, 3-State, Registered	35/20*	2Q84	24
MCM27S45	2k x 8 PROM, 3-State, Registered	35/20*	1Q84	24
MCM27S47	2k x 8 PROM, 3-State, Registered	35/20*	1Q84	24
MCM7621	512 x 4 PROM, 3-State	70	Α	16
MCM7621A	512 x 4 PROM, 3-State	60	Α .	16
MCM7641	512 x 8 PROM, 3-State	70	- A	24
MCM7641A	512 x 8 PROM, 3-State	60	А	24
MCM7643	1024 x 4 PROM, 3-State	70	A	18
MCM7643A	1024 x 4 PROM, 3-State	50	Α	18
MCM7649	512 x 8 PROM, 3-State	70	A	20
MCM7649A	512 x 8 PROM, 3-State	50	3Q83	20
MCMXXXXX	512 x 8 PROM, 3-State	35	1984	20
MCM7681	1024 x 8 PROM, 3-State	70	А	24
MCM7681A	1024 x 8 PROM, 3-State	50	3Q83	24
MCMXXXXX	1k x 8 PROM, 3-State	35	1984	24
MCM7685	2048 x 4 PROM, 3-State	70	A	18
MCM7685A	2048 x 4 PROM, 3-State	55	A	18
MCM76161	2048 x 8 PROM, 3-State	70	Α	24
MCM76161A	2048 x 8 PROM, 3-State	60	Α	24
MCMXXXXXX	2k x 8 PROM, 3-State	35	1984	24
MCM76165A	4096 x 4 PROM, 3-State	50	3Q83	20
MCM93422	256 x 4 RAM, 3-State	45	Α	22
MCM93L422	256 x 4 RAM, 3-State	60	А	22
MCM93415	1024 x 1 RAM, Open-Collector	45	A	18
MCM93425	1024 x 1 RAM, 3-State	45	A	18

^{*}For Registered PROMs, tSA tPHL (Address setup time propagation delay, clock to output)

Functional Selection

Abbreviations

S = Synchronous

A = Asynchronous

B = Both Synchronous and Asynchronous

2S = 2-State Output

3S = 3-State Output

OC = Open-Collector Output

P = Planned (See Numeric List for latest availability status.)

Inverters

Description	Type of Output	No.	LS	ALS	FAST
Hex	2S	04	X	X	×
	OC	05	X	X	

AND Gates

Description	Type of Output	No.	LS	ALS	FAST
Quad 2-Input	2S OC	08 09	X	X	X
Triple 3-Input	2S OC	11 15	X	X	Х
Dual 4-Input	2S	21	X	X	

NAND Gates

Description	Type of Output	No.	LS	ALS	FAST
Quad 2-Input	2S	00	Х	Х	Х
	OC	01	X	X	
	OC	03	X	X	
Quad 2-Input, High Voltage	OC	26	X		
Triple 3-Input	2S	10	X	X	×
	OC	12	X	X	
Dual 4-Input	2S	20	X	×	X
	OC	22	×	×	
8-Input	2S	30	X		
13-Input	2S	133	X		

OR

Description	Type of Output	No.	LS	ALS	FAST
Quad 2-Input	2S	32	X	Р	X

NOR

Description	Type of Output	No.	LS	ALS	FAST
Quad 2-Input	2S	2	Х	X	Х
Triple 3-Input	2S	27	X	X	
Dual 5-Input	2S	260	X		

Exclusive OR

Description	Type of Output	No.	LS	ALS	FAST
Quad 2-Input	2S	86	×		Р
	OC	136	X		
	2S	386	X		

Exclusive NOR

Description	Type of Output	No.	LS	ALS	FAST
Quad 2-Input	ОС	266	Х		

AND-OR-INVERT Gates

Description	Type of Output	No.	LS	ALS	FAST
Dual 2-Wide, 2-Input/3-Input	2S	51	X	Х	
4-Wide, 2-3-2-3-Input	2S	54	X		
2-Wide, 4-Input	2S	55	X	Х	
4-Wide, 4-2-2-3-Input	2S	64			Х

Schmitt Triggers

Description	Type of Output	No.	LS	ALS	FAST
Dual 4-Input NAND Gate	2S	13	Х	Р	
Hex, Inverting	2S	14	X	Р	
Quad 2-Input NAND Gate	2S	132	X	Р	

SSI Flip-Flops

Description	Clock Edge	No.	LS	ALS	FAST
Dual D w/Set & Clear	Pos	74	Х	Х	Х
Dual JK w Set	Neg	113	X		Р
Dual JK w/Clear	Neg Neg	73 107	X		
Dual JK w/Set & Clear	Neg Neg	76 78	×		
	Neg Neg	112 114	×		P P
Dual JK w Set & Clear	Pos	109	X	Р	Х

Multiplexers

Description	Type of Output	No.	LS	ALS	FAST
Quad 2-to-1, Non-Inverting	2S 3S	157 257	X	X P	P P
Quad 2-to-1, Inverting	2S 3S	158 258	X	X P	P P
Dual 4-to-1, Non-Inverting	2S 3S	153 253	X	P P	X
Dual 4-to-1, Inverting	2S 3S	352 353	X	P P	X
8-to-1	2S 3S	151 251	X	P P	P P
Quad 2-to-1 with Output Register	2S 2S 2S	298 398 399	X X X		

Encoders

Description	Type of Output	No.	LS	ALS	FAST
10- to 4-Line BCD	2S	147	Х		
8- to 3-Line Priority Encoder	2S	148	×		
	3S	348	X		
	2S	748	X		
	3S	848	X		

Register Files

Description	Type of Output	No.	LS	ALS	FAST
4 × 4	OC 3S	170 670	X		

Decoders/Demultiplexers

Description	Type of Output	No.	LS	ALS	FAST
Dual 1-of-4	2S	139	X	P	Р
	2S	155	X		
	oc	156	X		
	2S	239		P	
	3S	539		P	Р
1-of-8	2S	138	X	P	Р
	2S	238		P	
	3S	538		P	P
1-of-8 with Latch	2S	137	X		
1-of-10	2S	42	×		
	3S	537		P	P

Latches

	No. of	Type of				
Description	Bits	Output	No.	LS	ALS	FAST
Transparent, Non-	4	2S	77	Х		
Inverting	8	3S	373	X	Р	P
	8	3S	573		P	
Transparent, Inverting	8	3S	533		Р	X
	8	3S	563		Р	
	8	3S	580		P	
Transparent, Q and \overline{Q}	4	2S	75	×		
Outputs	4	2S	375	X		
Quad Set-Reset Latch	4	2S	279	X		
Addressable	8	2S	259	Χ		
Dual 4-Bit Addressable	4	2S	256	X		
Dual 4-Bit Transparent, Non-Inverting	8	3S	873		Р	
Dual 4-Bit Transparent, Inverting	8	3S	880		Р	

Shift Registers

	No. of	Type of			Mode*					
Description	Bits	Output	SR	SL	Hold	Reset	No.	LS	ALS	FAS
Serial In-Serial Out	8	2S	Х				91	Х	Р	
Serial In-Parallel Out	8	2S	×			Α	164	×	P	
Parallel In-Serial Out	8	2S	X		X		165	×		
	8	2S	X		×	Α	166	X		
	16	3S	X		X		674	×		
Parallel In-Parallel Out	4	2S	X				95	X		
	4	2S	X	X	×	Α	194	X		P
	4	2S	X			Α	195	X		Р
	4	3S	×				295	X		
	4	3S	X			Α	395	X		
Parallel In-Parallel Out, Bidirectional	8	3S	X	X	X	A	299	×		
	8	3S	×	X	X	S	323	X		Р
Sign Extended Bidirectional	8	3S	X		X	A	322	X		
Serial In-Parallel Out with Storage Register	16	25/35	×		×	S	673	Х		
Parallel In-Parallel Out with Storage Register/Mux	4	3S	×	×	X	A	671		P	
	4	3S	X	X	X	S	672		P	

^{*} SR = Shift Right SL = Shift Left

Asynchronous Counters — Negative Edge-Triggered*

Description	Load	Set	Reset	No.	LS	ALS	FAST
Decade (2/5)		Х	·X	90	- X		
	X		X	196	X		
		X	X	290	X		
Dual Decade (2/5)			X	390	X		-
Dual Decade		X	X	490	X		
Modulo 12 (2/6)			X	92	Х		
4-Bit Binary (2/8)			X	93	X		
	X		X	197	X		
			X	293	X		
Dual 4-Bit Binary			×	393	Х		
Divide-By-N (0-9)	X		Х	716*	X		
Divide-By-N (0-15)	Х		Х	718*	Х		

^{*}The 716 and 718 are positive edge-triggered.

Display Decoders/Drivers with Open-Collector Outputs*

Description	No.	LS	ALS	FAST
1-of-10	145	Х		
BCD-to-7 Segment	47	X		
-	48*	X		
	49	X		
	247	X		
	248*	X		
	249	Х		

^{*}The 48 and 248 have internal pullup resistors to VCC on their outputs.

Cascadable* Synchronous Counters — Positive Edge-Triggered

Description	Type of Output	Load	Reset	No.	LS	ALS	FAST
Decade	2S 2S 3S	S S B	A S B	160 162 560	X	X X P	P P
Decade, Up/Down	2S 2S 2S 3S	S A A S	A B	168 190 192 568	X X X	P X X P	P P P
4-Bit Binary	2S 2S 2S 3S	S S S	A S B	668 161 163 561	X X X	X X P	P P
4-Bit Binary, Up/Down	2S 2S 2S 3S 2S	S A A S	A B	169 191 193 569 669	X X X X	P X X P	P P P
Decade with Latch/Mux	3S 3S 3S	S S S	A S S	690 692 694	۸	P P P	
Decade with Register/Mux	3S 3S	S S	A S	696 698		P P	
4-Bit Binary w/ Latch/Mux	3S 3S 3S	S S S	A S S	691 693 695		P P P	
4-Bit Binary w/ Register/Mux	3S 3S	S S	A S	697 699		P P	

^{*}The 192 and 193 do not provide a clock enable for synchronous cascading.

MSI Flip-Flops/Registers

Description	No. of Bits	Type of Output	Set or Reset	Clock Enable	No.	LS	ALS	FAST
D-Type, Non-Inverting	4	3S	Α	Х	173	Х		
	4	2S		X	377	X	X	
	6	2S	Α		174	X		P
	6	2S		X	378	X		P
	8	2S	Α		273	X	X	
	8	3S			374	X	P	X
	8	35			574		P	
	8	3S	S		575		P	
D-Type, Inverting	8	3S			534		P	×
	8	3S			564		Р	
	8	3S			576		Р	
	8	3S	S		577		Р	
D-Type, Q and \overline{Q} Outputs	4	2S	Α		175	X		P
	4	2S		X	379	X		Р
Dual 4-Bit, Non-Inverting	8	3S	Α		874		Р	
	8	3S	S		878		Р	
Dual 4-Bit, Inverting	8	3S	Α		876	,	Р	
Dati 4 Dit, involving	8	3S	S		879		P	
Dual 8-Bit with Multiplexers	16	3S			604	×		
	16	oc			605	X		
	16	3S			606	X		
	16	oc			607	X		

Arithmetic Operators

Description	No.	LS	ALS	FAST
4-Bit Adder	. 83	×		
	283	X		P
4-Bit ALU	181	X		P
	381			P
	382			P
Look Ahead Carry Generator	182	×		Р
Quad 4-Bit Adder/Subtracter	385	X		
Dual Carry/Save Full Adder	183	×		
4-Bit Barrel Shifter	350			P

Magnitude Comparitors

Description	Type of Output	P = Q	P>Q	P <q< th=""><th>No.</th><th>LS</th><th>ALS</th><th>FAST</th></q<>	No.	LS	ALS	FAST
4-Bit	2S	Х	Х	Х	85	X		
8-Bit	2S	X	X		682	X		
	OC	X	X		683	X		
	2S	X	X		684	X		
	OC	X	X		685	X		
	2S	X			521			Р
8-Bit with	2S	X	X		686	X		
Output	OC	X	X		687	X		
Enable	2S	X			688	×		
	OC	X			689	X		

Parity Generators/Checkers

Description	No.	LS	ALS	FAST
9-Bit Odd/Even Parity Generator/ Checker	280	Х		Р

Dynamic Memory Support

Description	No.	LS	ALS	Fast
Synchronous Address Multiplexer (MC6883)	783	X		
Error Detection and Correction Circuit (EDAC)	2960			Р
EDAC Bus Buffer	2961			Р
	2962			Р
Dynamic Memory Controller	2968			Р
Dynamic Memory Timing Controller with EDAC	2969			Р
Dynamic Memory Timing Controller without EDAC	2970			Р

VCOs and Multivibrators

Description	No.	LS	ALS	FAST
Retriggerable Monostable Multivibrator	122	X		
Dual 122	123	×		
Precision Non-Retriggerable Monostable Multivibrator	221	X		
Voltage/Crystal Controlled Oscillator	724	X		

Buffers/Line Drivers

Description	Type of Output	No.	LS	ALS	FAST
Quad 2-Input NOR	2S OC	28 33	X	P P	
Quad 2-Input NAND	2S OC	37 38	X	X	
Dual 4-Input NAND	2S	40	X	Р	
Quad, Non-Inverting	3S 3S	125 126	X		
Hex, Non-Inverting	3S 3S	365 367	X		
Hex, Inverting	3S 3S	366 368	X		
Octal, Non-Inverting	3S 3S 3S 3S	241 244 541 795 797	X X X	X X P	P P
Octal, Inverting	3S 3S 3S 3S	240 540 796 798	X	X P	Р

Transceivers

	Type of				
Description	Output	No.	LS	ALS	FAST
Quad, Non-Inverting	3S	243	Х	Х	Р
Quad, Inverting	3S	242	×	X	P
Octal, Non-Inverting	3S	245	×	×	X
	3S	645	X		
	OC	621	X	X	
	3S	623	X	X	X
	3S/OC	639		X	
	OC	641	X	X	
Octal, Inverting	3S	620	×	×	X
	OC	622	X	X	
	3S/OC	638		X	
	3S	640	X	X	X
	OC	642	X	X	
	3S	643	X	X	X
	OC	644	X	X	
Octal, Non-Inverting with	3S	646		Р	
Register/Mux	OC	647		P	
	3S	652		Р	
	OC/3S	654		Р	
Octal, Inverting with	3S	648		Р	
Register/Mux	OC	649		Р	
	3S	651		Р	
	OC/3S	653		P,	

RAM

Description	Type of Output	No.	LS	ALS	FAST
16-by-4	3S OC	189 289			P P

Circuit Characteristics

SCHOTTKY TTL



CIRCUIT CHARACTERISTICS

FAMILY CHARACTERISTICS

LS TTL

The Low Power Schottky (LSTTL) family combines a current and power reduction improvement over standard 7400 TTL by a factor of 5. This is accomplished by using Schottky diode clamping to prevent saturation and advanced processing.

ALS TTL

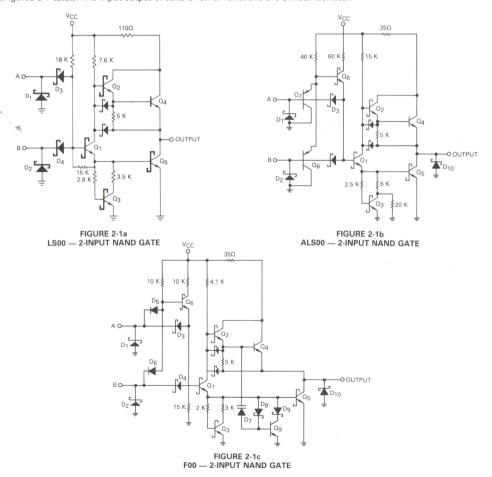
The Advanced Low Power Schottky TTL family (ALS TTL) provides a 50% power reduction compared to standard 54/74 LS TTL and yet offers improved circuit performance over standard LS due to Motorola's state-of-the-art oxide isolated process (MOSAIC). ALS also differs from LS in that PNP transistors on the input stage are utilized to lower input currents and raise thresholds.

FAST TTL

The FAST Schottky TTL family provides a 75-80% power reduction compared to standard Schottky (54/74S) TTL and yet offers a 20-40% improvement in circuit performance over the standard Schottky due to the MOSAIC process. Also, FAST circuits contain additional circuitry to provide a flatter power/frequency curve. The input configuration of FAST uses a lower input current which translates into higher fanout.

CIRCUIT FEATURES

Circuit features of LS, ALS and FAST are best understood by examining the TTL 2-input NAND gate of each family (Figures 2-1-a,b,c). The input/output circuits of other functions are almost identical.



INPUT CONFIGURATION. Motorola LSTTL circuits do not use the multi-emitter input structure that originally gave TTL its name. Most LS elements use a DTL type input circuit with Schottky diodes to perform the AND function, as exemplified by D3 and D4 in Figure 2-1a. Compared to the classical multi-emitter structure, this circuit is faster and increases the input breakdown voltage. Inputs of this type are tested for leakage with an applied input voltage of 7.0 V and the input breakdown voltage is typically 15 V or more.

The ALS00 differs from the LS00 in that Q6, Q7 and Q8 have been added to reduce input current (I_{|L}) by a factor of 4, and increase input threshold from approximately 1.1 to 1.5 volts.

The F00 input configuration utilizes a PN diode (D5 and D6) rather than the PNP transistor used in ALS. This is required due to the high speed response of FAST** logic. The PNP transistor, a relatively large device in current bipolar logic technology, has an associated capacitance large enough to make the gate input susceptible to ac noise. The PN diode results in much better ac noise immunity at the expense of increased input current.

Another input arrangement often used in LS MSI has three diodes connected as shown in Figure 2-2. This configuration gives a slightly higher input threshold than that of Figure 2-1a. A third input configuration that is sometimes used in LS TTL employs a vertical PNP transistor as shown in Figure 2-3. As with the ALS input, this arrangement also gives a higher input threshold and has the additional advantage of reducing the amount of current that the signal source must sink. Both the diode cluster arrangement and the PNP input configuration have breakdown voltage ratings greater than 7.0 V.

All inputs are provided with clamping diodes, exemplified by D1 and D2 in Figure 2-1a,b,c. These diodes conduct when an input signal goes negative, which limits undershoot and helps to control ringing on long signal lines following a HIGH-to-LOW transition. These diodes are intended only for the suppression of transient currents and should not be used as steady-state clamps in interface applications. A clamp current exceeding 2 mA and with a duration greater than 500 ns can activate a parasitic lateral NPN transistor, which in turn can steal current from internal nodes of an LS circuit and thus cause logic errors.

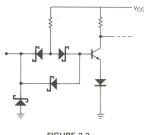
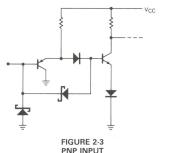


FIGURE 2-2 DIODE CLUSTER INPUT



INPUT CHARACTERISTICS — Figure 2-4 shows the typical input characteristics of LS, ALS, and FAST™. Typical transfer characteristics can be found in Figure 2-5 and input threshold variation with temperature information is provided in Table 2-1.

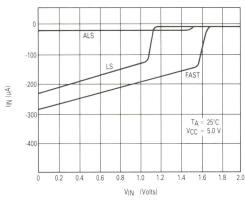


FIGURE 2-4
TYPICAL INPUT CURRENT VS. INPUT VOLTAGE

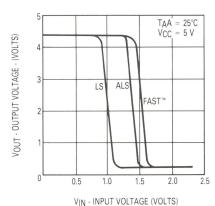


FIGURE 2-5

FIGURE 2-5 TYPICAL OUTPUT vs INPUT VOLTAGE CHARACTERISTIC

	-55°C	+ 25°C	+ 125°C
FAST	1.8	1.5	1.3
ALS	1.8	1.5	1.3
S	1.5	1.3	1.1
LS	1.2	1.0	0.8

TABLE 2.1
TYPICAL INPUT THRESHOLD VARIATION
WITH TEMPERATURE

OUTPUT CONFIGURATION. The output circuitry of LSTTL has several features not found in conventional TTL. A few of these features are discussed below.

Referring to Figures 2-1a,b,c, the base of the pull-down output transistor Q5 is returned to ground through Q3 and a pair of resistors instead of through a simple resistor. This arrangement is called a squaring network since it squares up the transfer characteristics (Figure 2-5) by preventing conduction in the phase splitter Q1 until the input voltage rises high enough to allow Q1 to supply base current to Q5. The squaring network also improves the propagation delay by providing a low resistance path to discharge capacitance at the base of Q5 during turn-off.

The output pull-up circuit is a 2-transistor Darlington circuit with the base of the output transistor returned through a 5k resistor to the output terminals, unlike 74H and 74S where it is returned to ground which is a more power consuming configuration. This configuration allows the output to pull up to one VBE below VCC for low values of output current.

The ALS00 and F00 outputs include clamping diodes to limit undershoot and control ringing on long signal lines. As with the input diode clamps, these diodes are intended for transient suppression only and should not be used as steady state clamps.

The F00 output configuration also includes additional circuitry to improve the rise time and decrease the power consumption at high operating frequencies. This circuit, which consists of Q9, D7, D8, and D9 causes Q5 to off more quickly on LOW to HIGH output transitions.

Figure 2-6 shows the extra circuitry used to obtain the "high Z" condition in 3-state ouputs. When the Output Enable signal is HIGH, both the phase splitter and the Darlington pull-up are turned off. In this condition the output circuitry is non-conducting, which allows the outputs of two or more such circuits to be connected together in a bus application wherein only one output is enabled at any particular time.

FAST™ 3-state outputs have some additional circuitry due to the nature of the environment in which they are used. The effective capacitive load of a 3-state output tends to increase at high bus rates. The addition of Q10 reduces this effect by clamping the base of Q5 low when the device is in the high impedance state. In the high Z state, the output capacitance is about 5 pF for 24 mA outputs and about 12 pF for 64 mA outputs.

An additional feature of many FAST™ 3-state devices is the incorporation of power-up circuitry to guarantee that the output will not sink current if the device is disabled during the application or removal of power.

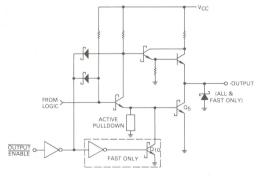


FIGURE 2-6
TYPICAL 3-STATE OUTPUT CONTROL

OUTPUT CHARACTERISTICS. Figure 2-7 shows the LOW-state output characteristics for LS, ALS and FAST™. For LOW IOL values, the pull-down transistor is clamped out of deep saturation to shorten the turn-off delay. Figure 2-8 shows the HIGH-state output characteristics.

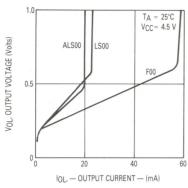


FIGURE 2-7a — OUTPUT LOW CHARACTERISTIC

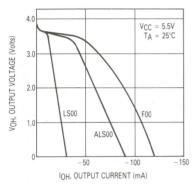


FIGURE 2-8a — OUTPUT HIGH CHARACTERISTIC

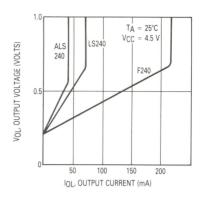


FIGURE 2-7b — OUTPUT LOW CHARACTERISTIC

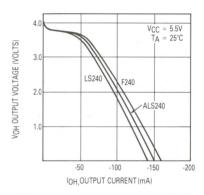
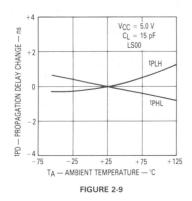


FIGURE 2-8b — OUTPUT HIGH CHARACTERISTIC

AC SWITCHING CHARACTERISTICS. The propagation through a logic element depends on power supply voltage, ambient temperature, and output load. The effect of each of these parameters on ac propagation is shown in Figures 2-9 through 2-11.

The delay through a logic element will increase to some extent when multiple outputs switch simultaneously due to inductance internal to the IC package. This effect can be seen by comparing Figures 2-11e and 2-11f.

For LS TTL, limits are guaranteed at 25° C, $V_{CC} = 5.0$ V, and CI = 15 pF (normally, resistive load has minimal effect on propagation delay). ALS and FAST[™] TTL limits are guaranteed over the commercial or military temperature and supply voltage ranges and with CI = 50 pF.



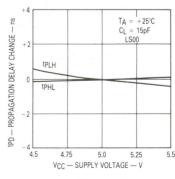


FIGURE 2-10

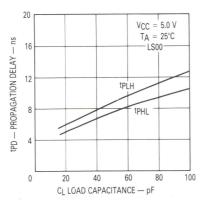


FIGURE 2-11a*

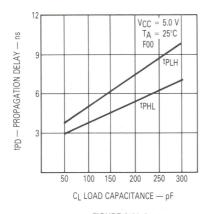


FIGURE 2-11c*

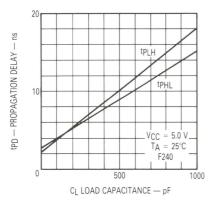


FIGURE 2-11e*

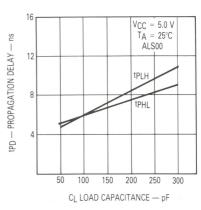


FIGURE 2-11b*

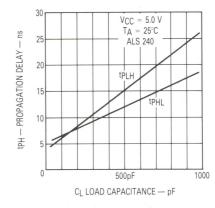


FIGURE 2-11d*

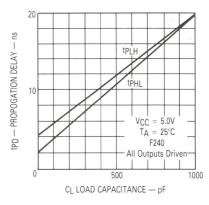


FIGURE 2-11f

^{*}Data for Figures 2-11a through 2-11e was taken with only one output switching at a time. Figure 2-11F data was taken with all 8 inputs of the F240 tied together.

Design Considerations Symbol Definitions and Testing

SCHOTTKY TTL



DESIGN CONSIDERATIONS

SELECTING TTL LOGIC. TTL Families may be mixed in a system for optimum performance. For instance, in new designs, ALS would commonly be used in non-critical speed paths to minimize power consumption while FAST™ TTL would be used in high speed paths. The ratio of ALS to FAST™ will depend on overall system design goals.

NOISE IMMUNITY. When mixing TTL families it is often desirable to know the guaranteed noise immunity for both LOW and HIGH logic levels. Table 3.1 lists the guaranteed logic levels for various TTL families and can be used to calculate noise margin. Table 3.2 specifies these noise margins for systems containing LS, S, ALS and/or FAST™ TTL. Note that Table 3.2 represents "worst case" limits and assumes a maximum power supply and temperature variation across the IC's which are interconnected, as well as maximum rated load. Increased noise immunity can be achieved by designing with decreased maximum allowable operating ranges.

TABLE 3.1 Worst Case TTL Logic Levels

Electrical Characteristics

	V ** . 'A	Milita	ary (—	55 to ±	125°C)	Com	mercia	I (0 to	70°C)	
	TTL Families	VIL	VIH	VOL	VOH	VIL	VIH	VOL	Vон	UNITS
TTL	Standard TTL 9000, 54/74	0.8	2.0	0.4	2.4	8.0	2.0	0.4	2.4	V
HTTL	High Speed TTL 54H/74H	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
LPTTL	Low Power TTL 93L00 (MSI)	0.7	2.0	0.3	2.4	8.0	2.0	0.3	2.4	V
STTL	Schottky TTL 54S/74S, 93S00	0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.7	V
LSTTL	Low Power Schottky TTL 54LS/74LS	0.7	2.0	0.4	2.5	8.0	2.0	0.5	2.7	V
ALS TTL (5% VCC)	Advanced LS TTL, 54ALS/74ALS					8.0	2.0	0.5	2.75	V
(10% V _{CC})		0.8	2.0	0.4	2.5	0.8	2.0	0.5	2.5	V
FAST TTL(5% V _{CC})	Advanced S TTL, 54F/74F					0.8	2.0	0.5	2.7	V
(10% V _{CC})		0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.5	V

V_{OL} and V_{OH} are the voltages generated at the output V_{IL} and V_{IH} are the voltage required at the input to generate the appropriate levels. The numbers given above are guaranteed worst-case values.

TABLE 3.2a

	To					
From		LS	S	ALS	FAST	Units
LS		300	400	400	400	mV
S		200	300	300	300	mV
ALS		300	400	400	400	mV
FAST™		200	300	300	300	mV

From "VOI" to "VII"

TABLE 3.2c LOW Level Noise Margins (Commercial)

	To					
From		LS	S	ALS	FAST	Units
LS		300	300	300	300	mV
S		300	300	300	300	mV
ALS		300	300	300	300	mV
FAST™		300	300	300	300	mV

From "VOL" to "VIL"

TABLE 3.2b HIGH Level Noise Margins (Military)

То					
From	LS	S	ALS	FAST	Units
LS	500	500	500	500	mV
S	500	500	500	500	mV
ALS	500	500	500	500	mV
FAST™	500	500	500	500	mV

From "VOH" to "VIH"

TABLE 3.2d HIGH Level Noise Margins (Commercial)

То					
From	LS	S	ALS	FAST	Units
LS	700	700	700	700	mV
S	700	700	700	700	mV
ALS (5% VCC)	750	750	750	750	mV
FAST (5% VCC)	700	700	700	700	mV
ALS (10% V _{CC})	500	500	500	500	mV
FAST (10% V _{CC})	500	500	500	500	mV

From "VOH" to "VIH"

POWER CONSUMPTION. With the exception of ECL, all logic families exhibit increased power consumption at high frequencies. Figure 3.1 shows this characteristic for common logic families. As indicated in the figure, TTL devices are more efficient at high frequencies than CMOS.

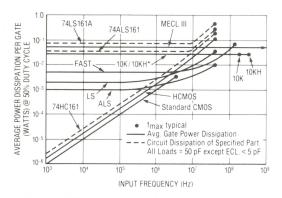


FIGURE 3-1 AVERAGE GATE POWER DISSIPATION versus FREQUENCY

FAN-IN AND FAN-OUT. In order to simplify designing with Motorola TTL devices, the input and output loading parameters of all families are normalized to the following values:

1 TTL Unit Load (U.L.) = 40 μA in the HIGH state (Logic "1")

1 TTL Unit Load (U.L.) = 1.6 mA in the LOW state (Logic "0")

Input loading and output drive factors of all products described in this handbook are related to these definitions.

EXAMPLES — INPUT LOAD

- 1. A 7400 gate, which has a maximum I_{IL} of 1.6 mA and I_{IH} of 40 µA is specified as having an input load factor of 1 U.L. (Also called a fan-in of 1 load.)
- 2. The 74LS95B which has a value of $I_{IL} = 0.8$ mA and I_{IH} of 40 μ A on the CP terminal, is specified as having an input LOW load factor of

$$\frac{0.8 \text{ mA}}{1.6 \text{ mA}}$$
 or 0.5 U.L. and an input HIGH load factor of $\frac{40 \,\mu\text{A}}{40 \,\mu\text{A}}$ or 1 U.L.

3. The 74LS00 gate which has an I_{IL} of 0.4 mA and an I_{IH} of 20 µA, has an input LOW load factor of

$$\frac{0.4\,\mathrm{mA}}{1.6\,\mathrm{mA}}$$
 or 0.25 U.L. an input HIGH load factor of $\frac{20\,\mu\mathrm{A}}{40\,\mu\mathrm{A}}$ or 0.5 U.L.

EXAMPLES — OUTPUT DRIVE

1. The output of the 7400 will sink 16 mA in the LOW (logic "O") state and source 800 μ A in the HIGH (logic "1") state. The normalized output LOW drive factor is therefore

$$\frac{16 \text{ mA}}{1.6 \text{ mA}} = 10 \text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{800 \, \mu A}{40 \, \mu A}$$
 or 20 U.L.

2. The output of the 74LS00 will sink 8.0 mA in the LOW state and source 400 μ A in the HIGH state. The normalized output LOW drive factor is

and the output HIGH drive factor is

$$\frac{400 \,\mu\text{A}}{40 \,\mu\text{A}}$$
 or 10 U.L.

Relative load and drive factors for the basic TTL families are given in Table 3.3.

FARAU V	INPUT	LOAD	OUTPUT DRIVE		
FAMILY	HIGH	LOW	HIGH	LOW	
74LS00	0.5 U.L.	0.25 U.L.	10 U.L.	5 U.L.	
7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.	
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.	
74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.	
74S00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.	
74 ALS	0.5 U.L.	0.0625 U.L.	10 U.L.	5 U.L.	
74 FAST	0.5 U.L.	0.375 U.L.	25 U.L.	12.5 U.L.	

TABLE 3.3

Values for MSI devices vary significantly from one element to another. Consult the appropriate data sheet for actual characteristics.

WIRED-OR APPLICATIONS. Certain TTL devices are provided with an "open" collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fan-out of the OR tie and the number of devices in the OR tie. The pull-up resistor value is chosen from a range between maximum value (established to maintain the required V_{OH} with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fan-out is not exceeded when only one output is LOW).

MINIMUM AND MAXIMUM PULL-UP RESISTOR VALUES

$$\mathsf{R}_{\mathsf{X}(\mathsf{MIN})} = \ \frac{\mathsf{V}_{\mathsf{CC}(\mathsf{MAX})} - \mathsf{V}_{\mathsf{OL}}}{\mathsf{I}_{\mathsf{OL}} - \mathsf{N}_{\mathsf{2}}(\mathsf{LOW}) \bullet 1.6 \ \mathsf{mA}} \\ \mathsf{R}_{\mathsf{X}(\mathsf{MAX})} = \frac{\mathsf{V}_{\mathsf{CC}(\mathsf{MIN})} - \mathsf{V}_{\mathsf{OH}}}{\mathsf{N}_{\mathsf{1}} \bullet \mathsf{I}_{\mathsf{OH}} + \mathsf{N}_{\mathsf{2}}(\mathsf{HIGH}) \bullet 40 \ \mu \mathsf{A}} \\ \mathsf{R}_{\mathsf{MAX}} = \frac{\mathsf{V}_{\mathsf{CC}(\mathsf{MIN})} - \mathsf{V}_{\mathsf{OH}}}{\mathsf{N}_{\mathsf{1}} \bullet \mathsf{I}_{\mathsf{OH}} + \mathsf{N}_{\mathsf{2}}(\mathsf{HIGH}) \bullet 40 \ \mu \mathsf{A}} \\ \mathsf{R}_{\mathsf{MAX}} = \frac{\mathsf{V}_{\mathsf{CC}(\mathsf{MIN})} - \mathsf{V}_{\mathsf{OH}}}{\mathsf{N}_{\mathsf{1}} \bullet \mathsf{I}_{\mathsf{OH}} + \mathsf{N}_{\mathsf{2}}(\mathsf{HIGH}) \bullet 40 \ \mu \mathsf{A}} \\ \mathsf{R}_{\mathsf{MAX}} = \frac{\mathsf{V}_{\mathsf{CC}(\mathsf{MIN})} - \mathsf{V}_{\mathsf{OH}}}{\mathsf{N}_{\mathsf{1}} \bullet \mathsf{I}_{\mathsf{OH}} + \mathsf{N}_{\mathsf{2}}(\mathsf{HIGH}) \bullet 40 \ \mu \mathsf{A}} \\ \mathsf{R}_{\mathsf{MAX}} = \frac{\mathsf{V}_{\mathsf{CC}(\mathsf{MIN})} - \mathsf{V}_{\mathsf{OH}}}{\mathsf{N}_{\mathsf{1}} \bullet \mathsf{I}_{\mathsf{OH}} + \mathsf{N}_{\mathsf{2}}(\mathsf{HIGH}) \bullet 40 \ \mu \mathsf{A}} \\ \mathsf{R}_{\mathsf{MAX}} = \frac{\mathsf{V}_{\mathsf{CC}(\mathsf{MIN})} - \mathsf{V}_{\mathsf{OH}}}{\mathsf{N}_{\mathsf{1}} \bullet \mathsf{I}_{\mathsf{OH}} + \mathsf{N}_{\mathsf{2}}(\mathsf{HIGH}) \bullet 40 \ \mu \mathsf{A}} \\ \mathsf{N}_{\mathsf{1}} = \frac{\mathsf{V}_{\mathsf{CC}(\mathsf{MIN})} - \mathsf{V}_{\mathsf{OH}}}{\mathsf{N}_{\mathsf{1}} \bullet \mathsf{I}_{\mathsf{1}} \bullet \mathsf{I}_{\mathsf{1}}} \\ \mathsf{N}_{\mathsf{1}} = \frac{\mathsf{V}_{\mathsf{CC}(\mathsf{MIN})} - \mathsf{V}_{\mathsf{OH}}}{\mathsf{N}_{\mathsf{1}} \bullet \mathsf{I}_{\mathsf{1}} \bullet \mathsf{I}_{\mathsf{1}}} \\ \mathsf{N}_{\mathsf{1}} = \frac{\mathsf{V}_{\mathsf{CC}(\mathsf{MIN})} - \mathsf{V}_{\mathsf{OH}}}{\mathsf{N}_{\mathsf{1}} \bullet \mathsf{I}_{\mathsf{1}}} \\ \mathsf{N}_{\mathsf{1}} = \frac{\mathsf{N}_{\mathsf{1}} \mathsf{N}_{\mathsf{1}} \bullet \mathsf{N}_{\mathsf{1}}}{\mathsf{N}_{\mathsf{1}}} \\ \mathsf{N}_{\mathsf{1}} = \frac{\mathsf{N}_{\mathsf{1}} \mathsf{N}_{\mathsf{1}} \bullet \mathsf{N}_{\mathsf{1}}}{\mathsf{N}_{\mathsf{1}}} \\ \mathsf{N}_{\mathsf{1}} = \frac{\mathsf{N}_{\mathsf{1}} \mathsf{N}_{\mathsf{1}}}{\mathsf{N}_{\mathsf{1}}} \\ \mathsf{N}_{\mathsf{1}} = \frac{\mathsf{N}_{\mathsf{1}}}{\mathsf{N}_{\mathsf{1}}} \\ \mathsf{N}_{\mathsf{1}} = \frac{\mathsf{N}_{\mathsf{1}}}{\mathsf{N}_{\mathsf{1}} \\ \mathsf{N}_{\mathsf{1}} \\ \mathsf{N}_{\mathsf{1}} = \frac{\mathsf{N}$$

where:

R_X = External Pull-up Resistor N₁ = Number of Wired-OR Outputs

N2 = Number of Input Unit Loads (U.L.) being Driven

VOL = Output LOW Voltage Level (0.5 V) VOH = Output HIGH Voltage Level (2.4 V)

VCC = Power Supply Voltage

Example: Four 74LS03 gate outputs driving four other LS gates or MSI inputs.

$$RX(MIN) = \frac{5.25 \text{ V} - 0.5 \text{ V}}{8 \text{ mA} - 1.6 \text{ mA}} = \frac{4.75 \text{ V}}{6.4 \text{ mA}} = 742 \Omega$$

$$VOH = 2.4 \text{ V}$$

$$RX(MAX) = \frac{4.75 \text{ V} - 2.4 \text{ V}}{4 \cdot 100 \mu\text{A} + 2 \cdot 40 \mu\text{A}} = \frac{2.35 \text{ V}}{0.48 \text{ mA}} = 4.9 \text{ k}\Omega$$
where:
$$N_1 = 4$$

$$N_2 \text{ (HIGH)} = 4 \cdot 0.5 \text{ U.L.} = 2 \text{ U.L.}$$

$$N_2 \text{ (LOW)} = 4 \cdot 0.25 \text{ U.L.} = 1 \text{ U.L.}$$

$$IOH = 100 \mu\text{A}$$

$$IOL = 8 \text{ mA}$$

$$VOL = 0.5 \text{ V}$$

$$VOH = 2.4 \text{ V}$$

Any value of pull-up resistor between 742 Ω and 4.9 k Ω can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

UNUSED INPUTS. For best noise immunity and switching speed, unused TTL inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways of handling unused inputs are:

- 1. Connect unused input to V_{CC}. LS, ALS and FAST™ TTL inputs have a breakdown voltage > 7.0 V and require, therefore, no series resistor.
- 2. Connect the unused input to the output of an unused gate that is forced HIGH.

CAUTION: Do not connect an unused LS, ALS or FAST * input to another input of the same NAND or AND function. This method, recommended for normal TTL, increases the input coupling capacitance and thus reduces the ac noise immunity.

INPUT CAPACITANCE. As a rule of thumb, LS, ALS and FAST™ TTL inputs have an average capacitance of 5 pF for DIP packages. For an input that serves more than one internal function, each additional function adds approximately 1.5 pF.

LINE DRIVING — Because of its superior capacitive drive charateristics, TTL logic is often used in line driving applications which require various termination techniques to maintain signal integrity. Parameters associated with this application are listed in Table 3.4.

It is also often necessary to construct load lines to determine reflection waveforms in line driving applications. The input and output characteristic graphs of section 2 (Figs. 2-4, 2-7 and 2-8) can be very useful for this purpose.

OUTPUT RISE AND FALL TIMES provide important information in determining reflection waveforms and crosstalk coefficients. Typical rise and fall times are approximately 6.0 ns for ALS and LS and about 2.0 ns for FAST with a 50 pF load (measured 10-90%). Output rise and fall times become longer as capacitive load is increased.

INTERCONNECTION DELAYS. For those parts of a system in which timing is critical, designers should take into account the finite delay along the interconnections. These range from about 0.12 to 0.15 ns/inch for the type of interconnections normally used in TTL systems. Exceptions occur in systems using ground planes to reduce ground noise during a logic transition; ground planes give higher distributed capacitance and delays of about 0.15 to 0.22 ns/inch.

Most interconnections on a logic board are short enough that the wiring and load capacitance can be treated as a lumped capacitance for purposes of estimating their effect on the propagation delay of the driving circuit. When an interconnection is long enough that its delay is one-fourth to one-half of the signal transition time, the driver output waveform exhibits noticeable slope changes during a transition. This is evidence that during the initial portion of the output voltage transition the driver sees the characteristic impedance of the interconnection (normally $100~\Omega$ to $200~\Omega$), which for transient conditions appears as a resistor returned to the quiescent voltage existing just before the beginning of the transition. This characteristic impedance forms a voltage divider with the driver output impedance, tending to produce a signal transition having the same rise or fall time as in the no-load condition but with a reduced amplitude. This attenuated signal travels to the far end of the interconnection, which is essentially an unterminated transmission line, where upon the signal starts doubling. Simultaneously, a reflection voltage is generated which has the same amplitude and polarity as the original signal, e.g., if the driver output signal is positive-going the reflection will be positive-going, and as it travels back toward the driver it adds to the line voltage. At the instant the reflection arrives at the driver it adds algebraically to the still-rising driver output, accelerating the transition rate and producing the noticeable change in slope.

(ALL MAXIMUM RATINGS)		L	S		ALS		FA	ST	
Characteristic	Symbol	54LSxxx	74LSxxx	54ALxxx	74AL	Sxxx	54Fxxx	74Fxxx	Units
Operating Voltage Range	VCC	5 ± 10%	5 ± 5%	5 ± 10%	5 ± 10%	5 ± 5%	5 ± 10%	5 ± 5%	Vdc
Output Drive:	IOH	-0.4	- 0.4	-0.4	- 0.4	- 0.4	- 1.0	- 1.0	mA
Standard Output	OL	4.0	8.0	4.0	8.0	8.0	20	20	mA
	Isc	-20 to -100	- 20 to - 100	- 25 to - 150	- 25 to - 150	- 25 to - 150	-60 to -150	-60 to -150	mA
2 " 0	ЮН	- 12	- 15	- 12	- 12	- 15	- 12	- 15	mA
Buffer Output	lOL	12	24	12	12	24	48	64	mA
	ISC	-40 to -225	-40 to -225	-50 to -225	-50 to -225	-50 to -225	- 100 to - 225	- 100 to - 225	mA
Buffer Line Driving									
Capability:						8			
Minimum Rt into 2.5 v		178	84	178	84	84	43	32	Ω
Minimum Rt into 5.0 v		381	189	381	189	189	95	71	Ω

TABLE 3.4
OUTPUT CHARACTERISTICS FOR SCHOTTKY TTL LOGIC

If an interconnection is of such length that its delay is longer than half the signal transition time, the attenuated output of the driver has time to reach substantial completion before the reflection arrives. In the limit, the waveform observed at the driver output is a 2-step signal with a pedestal. In this circumstance the first load circuit to receive a full signal is the one at the far end, because of the doubling effect, while the last one to receive a full signal is the one nearest the driver since it must wait for the reflection to complete the transition. Thus, in a worst-case situation, the net contribution to the overall delay is twice the delay of the interconnection because the initial part of the signal must travel to the far end of the line and the reflection must return.

When load circuits are distributed along an interconnection, the input capacitance of each will cause a small reflection having a polarity opposite that of the signal transition, and each capacitance also slows the transition rate of the signal as it passes by. The series of small reflections, arriving back at the driver, is subtractive and has the effect of reducing the apparent amplitude of the signal. The successive slowing of the transition rate of the transmitted signal means that it takes longer for the signal to rise or fall to the threshold level of any particular load circuit. A rough but workable approach is to treat the load capacitances as an increase in the intrinsic distributed capacitance of the interconnection. Increasing the distributed capacitance of a transmission line reduces its impedance and increases its delay. A good approximation for ordinary TTL interconnections is that distributed load capacitance decreases the characteristic impedance by about one-third and increases the delay by one-half.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

	LS	ALS	FAST
Storage Temperature	-65°C to $+150^{\circ}\text{C}$	$-65^{\circ}\text{C to } + 150^{\circ}\text{C}$	- 65°C to + 150°C
Temperature (Ambient) Under Bias	−55°C to +125°C	−55°C to +125°C	−55°C to +125°C
VCC Pin Potential to Ground Pin	-0.5 V to +7.0 V	-0.5 V to +7.0 V	-0.5 V to +7.0 V
*Input Voltage (dc) Diode Inputs	-0.5 V to 15 V	-0.5 V to 5.5 V	−0.5 V to 5.5 V
*Input Current (dc)	-30 mA to $+5.0$ mA	-30 mA to $+5.0$ mA	-30 mA to $+5.0$ mA
Voltage Applied to Open Collector			
Outputs (Output HIGH)	-0.5 V to + 10 V	-0.5 V to +5.5 V	-0.5 V to +5.5 V
High Level Voltage Applied to			
Disabled 3-State Output	5.5 V	5.5 V	5.5 V

^{*}Either input voltage limit or input circuit limit is sufficient to protect the inputs — Circuits with 5.5 V maximum limits are listed below

Device types having inputs limited to 5.5 V are as follows:

SN74LS242/243, SN74LS245
SN74LS640/641/642/645
SN74LS299/322A/323
SN74LS673/674
— Inputs connected to outputs.
— Inputs connected to outputs.
— Certain Inputs.
— Certain Inputs.

DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATABOOK

CURRENTS — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

ICC	Supply Current — The current flowing into the VCC supply terminal of a circuit with the specified input
	conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case
	operation.

I_IH Input HIGH current — The current flowing into an input when a specified HIGH voltage is applied.

IIL Input LOW current — The current flowing out of an input when a specified LOW voltage is applied.

Output HIGH current. The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the IOH is the current flowing out of an output which is in the HIGH state.

IOL Output LOW current — The current flowing into an output which is in the LOW state.

Output short-circuit current — The current flowing out of an output which is in the HIGH state when that output is short circuit to ground (or other specified potential).

Output off current HIGH — The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.

Output off current LOW — The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

VOLTAGES — All voltages are referenced to ground. Negative voltage limits are specified as absolute values (*i.e.*, -10 V is greater than -1.0 V).

VCC	Supply voltage — The range of power supply voltage over which the device is guaranteed to operate within
	the specified limits.

VIK(MAX) Input clamp diode voltage — The most negative voltage at an input when 18 mA is forced out of that input terminal. This parameter guarantees the integrity of the input diode which is intended to clamp negative ringing at the input terminal.

VIH Input HIGH voltage — The range of input voltages that represents a logic HIGH in the system.

VIH(MIN) Minimum input HIGH voltage — The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.

V_{II} Input LOW voltage — The range of input voltages that represents a logic LOW in the system.

V_{IL(MAX)} Maximum input LOW voltage — The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.

VOH(MIN) Output HIGH voltage — The minimum voltage at an output terminal for the specified output current IOH and at the minimum value of VCC.

VOL(MAX) Output LOW voltage — The maximum voltage at an output terminal sinking the maximum specified load current IoL.

 V_{T+} **Positive-going threshold voltage** — The input voltage of a variable threshold device (*i.e.*, Schmitt Trigger) that is interpreted as a V_{IH} as the input transition rises from below $V_{T-(MIN)}$.

 V_{T-} **Negative-going threshold voltage** — The input voltage of a variable threshold device (*i.e.,* Schmitt Trigger) that is interpreted as a V_{IL} as the input transition falls from above $V_{T+(MAX)}$.

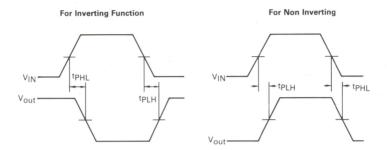
AC SWITCHING PARAMETERS AND WAVEFORMS

tPLH Propagation delay LOW-TO-HIGH:

The time delay from when the input is 1.3 V (1.5 for FAST) to when the output reaches 1.3 V (1.5 for FAST), while the output changes to a logic HIGH.

tPHL Propagation delay HIGH-TO-LOW:

The time delay from when the input is 1.3 V (1.5 for FAST) to when the output reaches 1.3 V (1.5 for FAST), while the output changes to a logic LOW.



waveform Rise Time:

tf

LOW to HIGH logic transition time, measured from the 10% to 90% points of the waveform.

Waveform Fall Time:

HIGH to LOW logic transition time, measured the 90% to the 10% points of the waveform.

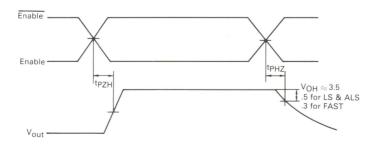


TPHZ Output disable time: HIGH to Z

The time delay between the specified amplitude point on the enable input and when the output falls 0.5 V (0.3 V for FAST) from the steady-state HIGH level.

tPZH Output enable time: Z to HIGH

The time delay between the specified amplitude points on the enable input and the output, when the output is going from a disabled state to a logic HIGH state.

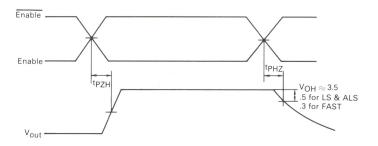


tPLZ Output disable time: LOW to Z

The time delay between the specified amplitude point on the enable input and when the output rises 0.5 V (0.3 V for FAST) from the steady-state LOW level.

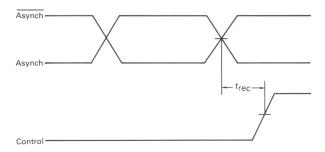
tpzL Output enable time: Z to LOW

The time delay between the specified amplitude points on the enable input and the output when the output is going from a disabled state to a logic LOW state.



t_{rec} Recovery time

Time required between an asynchronous signal (SET, RESET, CLEAR or PARALLEL load) and the active edge of a synchronous control signal, to insure that the device will properly respond to the synchronous signal.

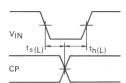


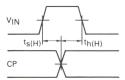
th Hold Time

The interval of time from the active edge of the control signal (usually the clock) to when the data to be recognized is no longer required to ensure proper interpretation of the data. A negative hold time indicates that the data may be removed at some time prior to the active edge of the control signal.

t_S Setup time

The interval of time during which the data to be recognized is required to remain constant prior to the active edge of the control signal to ensure proper data recognition.





t_w or

Pulse width

tpw

The time between the specified amplitude points (1.3 V for LS & ALS, 1.5 V for FAST) on the leading and trailing edges of a pulse.



fMAX

Toggle frequency/operating frequency

The maximum rate at which clock pulses meeting the clock requirements (i.e., t_{WH} , t_{WL} , and t_r , t_f) may be

applied to a sequential circuit. Above this frequency the device may cease to function.

fMAXmin

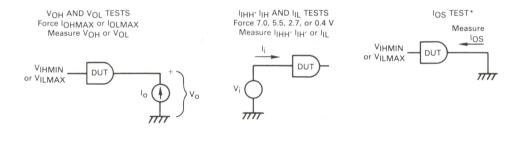
Guaranteed maximum clock frequency

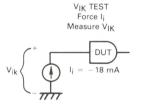
The lowest possible value for fMAX.

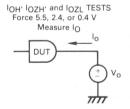
TESTING

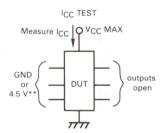
DC TEST CIRCUITS

The following test circuits and forcing functions represent Motorola's typical DC test procedures









^{*}The test for I_O (ALS devices) is performed in the same manner as I_{OS} except 2.25 volts is forced on the output instead of 0.0 V.

^{**}Unless otherwise indicated, input conditions are selected to produce a worst case condition.

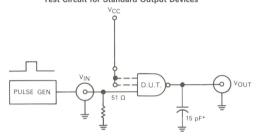
AC TEST CIRCUITS The following test circuits and conditions represent Motorola's typical test procedures. AC waveforms and terminology can be found on pages 3-8 to 3-10.

Proper testing requires that care be taken in the construction of AC test fixtures. This is especially true of FAST™ TTL.

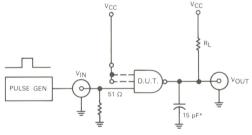
Maintaining a 50 Ω environment on the ac test fixture, as well as the use of multilayer boards with internal V_{CC} and ground planes is highly recommended for FAST^{∞} TTL. Bypassing with both electrolytic and high quality RF type capacitors should be provided on the board. Lead lengths for all components should be kept as short as possible (Motorola uses and recommends chip capacitors and resistors for ac test fixtures). Following these rules will result in cleaner waveforms as well as better correlation between Motorola and the FAST $^{\infty}$ TTL consumer.

LS TEST CIRCUITS

Test Circuit for Standard Output Devices

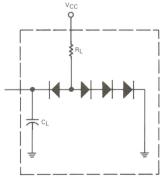


Test Circuit for Open Collector Output Devices



*includes all probe and jig capacitance

Optional LS Load (Guaranteed—Not Tested)

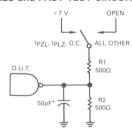


PULSE GENERATOR SETTINGS (UNLESS OTHERWISE SPECIFIED)

	LS	ALS	FAST
Frequency =	1MHZ	1MHZ	1MHZ
Duty Cycle =	50%	50%	50%
$1_{TLH} (t_r) =$	6 ns (15)*	6ns	2.5ns
$1_{THL}(t_f) =$	6ns (15)*	6ns	2.5ns
Amplitude =	0 to 3 V	0 to 3 V	0 to 3 V

*The specified propagation delay limits can be guaranteed with a 15 ns input rise time on all parameters except those requiring narrow pulse widths. Any frequency measurement over 15 MHz or pulse width less than 30 ns must be performed with a 6 ns input rise time.

ALS and FAST TEST CIRCUITS



*jncludes all probe and jig capacitance

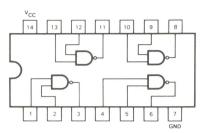
Note: for ALS open collector outputs with I $_{OL}=8$ mA, replace R1 and R2 with 1000 Ω resistors.

SCHOTTKY TTL

AIS LIST

LS Data Sheets





SN54LS00 SN74LS00

QUAD 2-INPUT NAND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

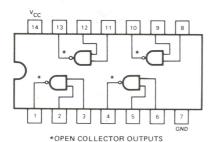
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
IOH	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMADOL	PARAMETER			LIMITS		UNITS	TECT	CONDITIONS	
SYMBOL	PARAMETER	1	MIN	TYP	MAX	UNITS	, IESI (CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	out HIGH Voltage for	
		54			0.7	.,		out LOW Voltage for	
V _{IL}	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	, V	V _{CC} = MIN, I _{IN} = -18 mA		
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{CC}$		
VOH	Output mon voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC}$		
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	V _{CC} = MAX, V	IN = 2.7 V	
lн	Input HIGH Current				0.1	mA	V _{CC} = MAX, V	IN = 7.0 V	
IIL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V	IN = 0.4 V	
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$		
Icc	Power Supply Current Total, Output HIGH Total, Output LOW				1.6	mA	V _{CC} = MAX		
	Total, Output LOVV	Total, Output LOVV			4.4				

SYMBOL	PARAMETER	LIMITS			UNITS	TEST COMPLIANC	
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH	Turn Off Delay, Input to Output		9.0	15	ns	V _{CC} = 5.0 V	
^t PHL	Turn On Delay, Input to Output		10	15	ns	$C_L = 15 pF$	





SN54LS01 SN74LS01

QUAD 2-INPUT NAND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

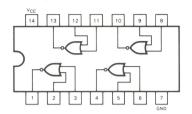
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
VOH	Output Voltage — High	54,74			5.5	V
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST	ONDITIONS
STIVIBUL	PARAIVIETER		MIN	TYP	MAX	UNITS	TEST C	ONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
		54			0.7	.,		ut LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$	
loн	Output HIGH Current	54,74			100	μΑ	V _{CC} = MIN, V _{OH} = MAX	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	VIN = VIL or VIH per Truth Table
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V
IIL	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_I$	N = 0.4 V
lcc	Power Supply Current Total, Output HIGH Total, Output LOW				1.6 4.4	mA	V _{CC} = MAX	

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
^t PLH	Turn Off Delay, Input to Output		17	32	ns	V _{CC} = 5.0 V
tPHL	Turn On Delay, Input to Output	-	15	28	ns	$C_L = 15 \text{ pF}, R_L = 2.0 \text{ k}\Omega$





SN54LS02 SN74LS02

QUAD 2-INPUT NOR GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 O	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lor	Output Current — Low	54 74			4.0 8.0	mA

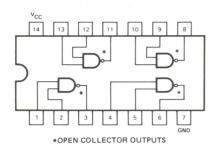
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS			TEST	ONDITIONS
STIVIBUL	PANAIVIETER		MIN	TYP	MAX	UNITS	IEST	ONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
					0.7	.,	Guaranteed Inp	ut LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN$, $I_{IN} = -18 \text{ mA}$	
Voн	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH}$	
VОН	Output High Voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	- V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
	1				20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V
I _{IL}	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_I$	N = 0.4 V
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
lcc	Power Supply Current Total, Output HIGH Total, Output LOW				3.2 5.4	mA.	$V_{CC} = MAX$	
			1	1		I	1	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			LINUTO	TEST COMPLETIONS
	PANAIVIETEN	MIN	TYP	MAX	UNITS	TEST CONDITIONS
^t PLH	Turn Off Delay, Input to Output		10	15	ns	V _{CC} = 5.0 V
^t PHL	Turn On Delay, Input to Output		10	15	ns	$C_L = 15 pF$





SN54LS03 SN74LS03

QUAD 2-INPUT NAND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

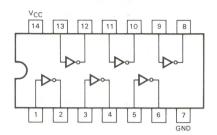
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
VOH	Output Voltage — High	54,74			5.5	V
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS	
STIVIBUL	FARAIVIETER	1	MIN	TYP	MAX	UNITS	TEST C	ONDITIONS
VIH	Input HIGH Voltage	put HIGH Voltage				V	Guaranteed Inp All Inputs	ut HIGH Voltage for
.,	1	54			0.7	,,		ut LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
ОН	Output HIGH Current	54,74			100	μΑ	$V_{CC} = MIN, V_{OH} = MAX$	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
V _{OL}	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V
IIL	Input LOW Current	Input LOW Current			-0.4	mA	$V_{CC} = MAX, V_{IN} = 0.4 V$	
Icc	Power Supply Current Total, Output HIGH Total, Output LOW				1.6	- mA	V _{CC} = MAX	

SYMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
^t PLH	Turn Off Delay, Input to Output		17	32	ns	$V_{CC} = 5.0 \text{ V}$
^t PHL	Turn On Delay, Input to Output		15	28	ns	$C_L = 15 \text{ pF}, R_L = 2.0 \text{ k}\Omega$





SN54LS04 SN74LS04

HEX INVERTER

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

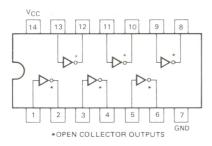
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V 1
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lor	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYME	201	PARAMETER	,		LIMITS		UNITS	TEST	ONDITIONS	
STIVIE	OL	TANAMETER		MIN	TYP	MAX	UNITS	TEST	ONDITIONS	
VIH		Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
			54			0.7		Guaranteed Input LOW Voltage fo		
VIL		Input LOW Voltage	74			0.8	V	All Inputs		
VIK		Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA	
Vон		Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OI}	$H = MAX, V_{IN} = V_{IH}$	
VОН		Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth Table		
		Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL			74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
						20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
IH		Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
IL		Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V	
los		Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
Icc		Power Supply Current Total, Output HIGH Total, Output LOW				2.4	mA	V _{CC} = MAX		

SYMBOL	PARAMETER		LIMITS		UNITS	TEST COMPITIONS
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
^t PLH	Turn Off Delay, Input to Output		9.0	15	ns	V _{CC} = 5.0 V
^t PHL	Turn On Delay, Input to Output		10	15	ns	$C_L = 15 \text{ pF}$





SN54LS05 SN74LS05

HEX INVERTER

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

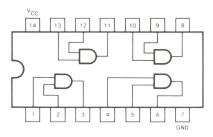
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
Vон	Output Voltage — High	54,74			5.5	V
IOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMBOL	PARAMETER			LIMITS		LINUTC	TEST CONDITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp	ut HIGH Voltage for
	Input LOW Voltage	54			0.7	.,		ut LOW Voltage for
VIL		74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA
ГОН	Output HIGH Current	54,74			100	μΑ	V _{CC} = MIN, V _C	DH = MAX
	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN$
VOL		74		0.35	0.5	٧	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
	'				20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V
l _{IL}	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_{IN} = 0.4 V$	
lcc	Power Supply Current C Total, Output HIGH				2.4	mA	V _{CC} = MAX	y *
	Total, Output LOW				6.6		VCC - IVIAX	

CVAADOL	DADAMETER		LIMITS		UNITS	TEST CONDITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
tPLH	Turn Off Delay, Input to Output		17	32	ns	$V_{CC} = 5.0 V$	
t _{PHL}	Turn On Delay, Input to Output		15	28	ns	$C_L = 15 \text{ pF}, R_L = 2.0 \text{ k}\Omega$	





SN54LS08 SN74LS08

QUAD 2-INPUT AND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

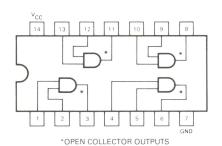
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
Тд	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ПОН	Output Current — High	54,74			-0.4	mA
lor	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST	ONDITIONS	
STIVIBUL	FARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS			
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
.,		54			0.7	.,		ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	V All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	= -18 mA	
Vон	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN}		
VOH	Output High Voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table	
. ,	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	VIN = VIL or VIH per Truth Table	
					20	μΑ	V _{CC} = MAX, V	N = 2.7 V	
Ін -	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _I	N = 7.0 V	
IL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	(, V _{IN} = 0.4 V	
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$		
lcc	Power Supply Current Total, Output HIGH				4.8	mA	V _{CC} = MAX		
	Total, Output LOW				8.8		VCC IVIAX		

SYMBOL	PARAMETER	LIMITS			UNITS	TECT COMPLETIONS
STIVIBOL	FARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
^t PLH	Turn Off Delay, Input to Output		8.0	15	ns	V _{CC} = 5.0 V
^t PHL	Turn On Delay, Input to Output		10	20	ns	C _L = 15 pF





SN54LS09 SN74LS09

QUAD 2-INPUT AND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

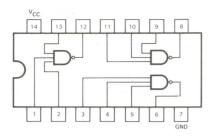
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
Vон	Output Voltage — High	54,74			5.5	V
IOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS		
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	1231 CONDITIONS			
VIH Input HIGH Voltage			2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
		54	-		0.7	.,		ut LOW Voltage for	
V _{IL}	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	ΛΙΝ, I _{IN} =− 18 mA	
loн	Output HIGH Current	54,74			100	μΑ	$V_{CC} = MIN, V_{C}$	$_{H}=MAX$	
	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	$V_{CC} = MAX, V$	IN = 2.7 V	
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_{IN} = 7.0 V$		
l _L	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V		
Icc	Power Supply Current Total, Output HIGH				4.8	mA	V _{CC} = MAX		
	Total, Output LOW				8.8		00		

CVAADOL	DADAMETED	LIMITS			UNITS	TEST CONDITIONS		
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
^t PLH	Turn Off Delay, Input to Output		20	35	ns	V _{CC} = 5.0 V		
^t PHL	Turn On Delay, Input to Output		17	35	ns	$C_L = 15 \text{ pF}, R_L = 2.0 \text{ k}\Omega$		





J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

SN54LS10 SN74LS10

TRIPLE 3-INPUT NAND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

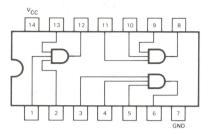
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
Vcc	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST	CONDITIONS	
STIVIBUL	FARAIVIETER	\	MIN	TYP	MAX	UNITS	TEST	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
		54			0.7	.,		out LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA	
Voh	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH}		
VOH	Output Hight voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	V _{CC} = MAX, V	N = 2.7 V	
lн	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _I	N = 7.0 V	
IIL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V	N = 0.4 V	
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current Total, Output HIGH Total, Output LOW		,: ,:		1.2	- mA	V _{CC} = MAX		

CVMPOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
SYMBOL		MIN	TYP	MAX	UNITS	TEST CONDITIONS
tPLH	Turn Off Delay, Input to Output		9.0	15	ns	V _{CC} = 5.0 V
^t PHL	Turn On Delay, Input to Output		10	15	ns	$C_L = 15 pF$





SN54LS11 SN74LS11

TRIPLE 3-INPUT AND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

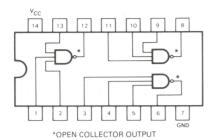
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS	
STIVIBUL	PARAIVIETER	1	MIN	TYP	MAX	UNITS	TEST	ONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
	54				0.7	.,	Guaranteed Inp	ut LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA
Voн	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$
VOH	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
		•			20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V
IIL	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_I$	N = 0.4 V
los	Short Circuit Current	Short Circuit Current			-100	mA	$V_{CC} = MAX$	
ICC	Power Supply Current Total, Output HIGH Total, Output LOW				3.6 6.6	- mA	V _{CC} = MAX	

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH	Turn Off Delay, Input to Output		8.0	15	ns	V _{CC} = 5.0 V	
^t PHL	Turn On Delay, Input to Output		10	20	ns	$C_L = 15 pF$	





SN54LS12 SN74LS12

TRIPLE 3-INPUT NAND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
Vон	Output Voltage — High	54,74			5.5	V
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMETER	PARAMETER		LIMITS		LINUTC	TEST CONDITIONS	
SYMBOL	PARAMETER	(MIN	TYP	MAX	UNITS	TEST	UNDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
		54			0.7	.,		ut LOW Voltage for
VIL	Input LOW Voltage				0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN$, $I_{IN} = -18 \text{ mA}$	
ГОН	Output HIGH Current	54,74			100	μΑ	$V_{CC} = MIN, V_{OH} = MAX$	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
					20	μΑ	V _{CC} = MAX, V _I	N = 2.7 V
lн	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _I	N = 7.0 V
l _I L	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V
lcc	Power Supply Current Total, Output HIGH				1.4	mA	V _{CC} = MAX	
	Total, Output LOW				3.3		ACC INIXX	

AC CHARACTERISTICS: $T_{\mbox{\scriptsize A}} = 25\,^{\circ}\mbox{\scriptsize C}$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST COMPLICATE	
	FARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH	Turn Off Delay, Input to Output		17	32	ns	V _{CC} = 5.0 V	
^t PHL	Turn On Delay, Input to Output		15	28	ns	$C_L = 15 \text{ pF}, R_L = 2.0 \text{ k}\Omega$	



DESCRIPTION — The SN54LS/74LS13 and SN54LS/74LS14 contain logic gates/inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional inverters

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

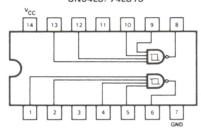
SN54LS/74LS13 SN54LS/74LS14

SCHMITT TRIGGERS DUAL GATE/HEX INVERTER

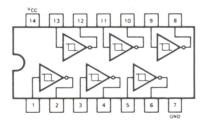
LOW POWER SCHOTTKY

LOGIC AND CONNECTION DIAGRAMS

SN54LS/74LS13



SN54LS/74LS14



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

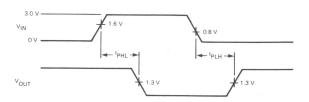
GUARANTEED OPERATING RANGES

GOMBANTE	D OI EIDTING IDTITUED					
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
Vcc	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMAROL	DADAMETED			LIMITS			TEST COMPITIONS
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{T+}	Positive-Going Thresho	ld Voltage	1.5		2.0	V	V _{CC} = 5.0 V
V _T -	Negative-Going Thresh	Negative-Going Threshold Voltage			1.1	V	V _{CC} = 5.0 V
V _T +-V _T -	Hysteresis		0.4	0.8		V	V _{CC} = 5.0 V
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$
V	0	54	2.5	3.4			V MIN I 400 V V
VOH	Output HIGH Voltage	74	2.7	3.4		V	$V_{CC} = MIN, I_{OH} = -400 \mu A, V_{IN} = V_{IL}$
VOL	Output LOW Voltage	54,74		0.25	0.4	V	$V_{CC} = MIN, I_{OL} = 4.0 \text{ mA}, V_{IN} = 2.0 \text{ V}$
VOL .	Output LOVV Voltage	74		0.35	0.5	V	$V_{CC} = MIN, I_{OL} = 8.0 \text{ mA}, V_{IN} = 2.0 \text{ V}$
I _{T+}	Input Current at			-0.14		mA	Vac Foxey
'1+	Positive-Going Thresho	ld		0.14		l liiA	$V_{CC} = 5.0 \text{ V}, V_{IN} = V_{T+}$
l -	Input Current at			0.10		mA	Vac 50000
IT-	Negative-Going Thresh	old	ž	-0.18		1110	$V_{CC} = 5.0 \text{ V}, V_{IN} = V_{T}$
lus	Input HIGH Current			1.0	20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$
IH	Input High Current			-	0.1	mA	$V_{CC} = MAX, V_{IN} = 7.0 V$
IIL.	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_{IN} = 0.4V$
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX, V _{OUT} = 0 V
	Power Supply Current						
	Total, Output HIGH	LS13	2	2.9	6.0		
Icc		LS14		8.6	16	mA ·	VCC = MAX
.00	Total, Output LOW	LS13		4.1	7.0		
	. o.a., o a.pat Lovv	LS14		12	21		

	7-1				
SYMBOL	PARAMETER	M	ΑX	UNITS	TEST CONDITIONS
STIVIBOL		LS13	LS14		TEST CONDITIONS
^t PLH	Propagation Delay, Input to Output	22	22	ns	V _{CC} = 5.0 V
^t PHL	Propagation Delay, Input to Output	27	22	ns	$C_L = 15 pF$



V_{IN} VERSUS V_{OUT} TRANSFER FUNCTION

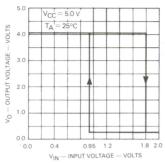


Fig. 1

THRESHOLD VOLTAGE AND HYSTERESIS VERSUS

POWER SUPPLY VOLTAGE

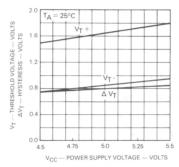


Fig. 2

THRESHOLD VOLTAGE HYSTERESIS VERSUS TEMPERATURE

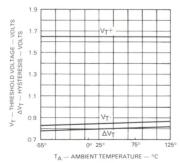
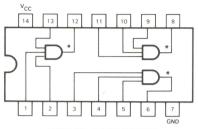


Fig. 3





*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

SN54LS15 SN74LS15

TRIPLE 3-INPUT AND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

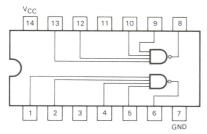
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
Voн	Output Voltage — High	54,74			5.5	V
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

PARAMETER			LIMITS		LINITS	TEST	ONDITIONS	
		MIN	TYP	MAX	UNITS	TEST CONDITIONS		
Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
	54			0.7		Guaranteed Inp	ut LOW Voltage for	
Input LOW Voltage	74			0.8	V	All Inputs		
Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
Output HIGH Current	54,74			100	μΑ	$V_{CC} = MIN, V_{CC}$	V _{CC} = MIN, V _{OH} = MAX	
Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$v_{CC} = v_{CC} MIN$,	
	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	VIN = VIL or VIH per Truth Table	
'				20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
Input LOW Current				-0.4	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$		
Power Supply Current Total, Output HIGH				3.6	- mA	V _{CC} = MAX		
	Input HIGH Voltage Input LOW Voltage Input Clamp Diode Volta Output HIGH Current Output LOW Voltage Input HIGH Current Input HIGH Current Power Supply Current	Input HIGH Voltage Input LOW Voltage Input Clamp Diode Voltage Output HIGH Current Output LOW Voltage 54,74 74 Input HIGH Current Input HIGH Current Input LOW Current Power Supply Current Total, Output HIGH	Input HIGH Voltage Input LOW Voltage Input Clamp Diode Voltage Output HIGH Current Output LOW Voltage Input LOW Voltage Input LOW Voltage Input HIGH Current Input HIGH Current Input LOW Current Power Supply Current Total, Output HIGH	PARAMETER	Name	PARAMETER MIN TYP MAX UNITS	PARAMETER	

SYMBOL	DADAMETED	LIMITS			LINUTC	TEST COMPITIONS		
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
t _{PLH}	Turn Off Delay, Input to Output		20	35	ns	V _{CC} = 5.0 V		
^t PHL	Turn On Delay, Input to Output		17	35	ns	$C_L = 15 \text{ pF}, R_L = 2.0 \text{ k}\Omega$		

MOTOROLA



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

SN54LS20 SN74LS20

DUAL 4-INPUT NAND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

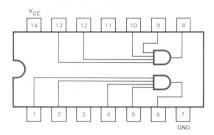
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	٧
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74	7		-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMADOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS		
SYMBOL	PARAIVIETER		MIN	TYP	MAX	UNITS	TEST C	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
		54			0.7	.,		ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA	
VoH	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{I}$		
VOH	Output high voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table	
	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
V _{OL}		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
		•			20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
IIL	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_I$	N = 0.4 V	
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
Icc	Total, Output HIGH	Power Supply Current Total, Output HIGH			0.8	mA	V _{CC} = MAX		
	Total, Output LOW				2.2		VCC - IVIAA		

CVMAROL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
SYMBOL		MIN	TYP	MAX	UNITS	TEST CONDITIONS
tPLH	Turn Off Delay, Input to Output		9.0	15	ns	V _{CC} = 5.0 v
tpHI	Turn On Delay, Input to Output		10	15	ns	$C_{L} = 15 pF$





SN54LS21 SN74LS21

DUAL 4-INPUT AND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA ^s

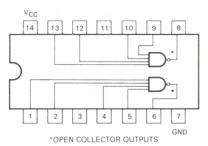
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	PARAMETER			LIMITS			TEST CONDITIONS		
SYMBOL			MIN	TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp	Guaranteed Input HIGH Voltage for All Inputs	
		54			0.7	.,		ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA	
Voн	Output HIGH Voltage	54	2.5	3.5	1	, V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} =		
VOH		74	2.7	3.5		V	or V _{IL} per Truth	Table	
	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN$,	
VOL		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	VIN = VIL or VIH per Truth Table	
					20	μΑ	V _{CC} = MAX, V	N = 2.7 V	
lН	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _I	N = 7.0 V	
ll L	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V	
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current Total, Output HIGH Total, Output LOW				2.4	mA	V _{CC} = MAX		

AC CHARACTERISTICS: $T_A = 25 \, ^{\circ} C$

SYMBOL	PARAMETER	LIMITS		LINUTC	TEST COMPLETIONS	
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
^t PLH	Turn Off Delay, Input to Output		8.0	15	ns	V _{CC} = 5.0 V
[†] PHL	Turn On Delay, Input to Output		10	20	ns	$C_L = 15 \text{ pF}$





SN54LS22 SN74LS22

DUAL 4-INPUT NAND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

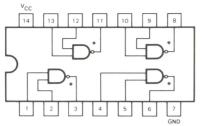
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
Тд	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
VOH	Output Voltage — High	54,74			5.5	V
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMDO	PARAMETER			LIMITS			TEST CONDITIONS	
SYMBOL			MIN	TYP	MAX	UNITS	TEST CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
		54			0.7	.,		ut LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	ige		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA
ГОН	Output HIGH Current	54,74			100	μΑ	$V_{CC} = MIN, V_{O}$	H = MAX
	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL		74		0.35	0.5	٧	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
					20	μΑ	$V_{CC} = MAX, V_{CC}$	N = 2.7 V
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V
IL	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_{IN} = 0.4 V$	
lcc	Power Supply Current Total, Output HIGH Total, Output LOW				0.8	mA	V _{CC} = MAX	

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
t _{PLH}	Turn Off Delay, Input to Output		17	32	ns	V _{CC} = 5.0 V
^t PHL	Turn On Delay, Input to Output		15	28	ns	$C_L = 15 \text{ pF}, R_L = 2.0 \text{ k}\Omega$





*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

SN54LS26 SN74LS26

QUAD 2-INPUT NAND BUFFER

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
VOH	Output Voltage — High	54,74			15	V
lor	Output Current — Low	54 74			4.0 8.0	mA

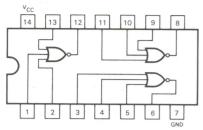
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS	
STIVIBUL	FARAIVIETER	1	MIN	TYP	MAX	UNITS	TEST C	ONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
		54			0.7	.,		ut LOW Voltage for
V_{IL}	Input LOW Voltage	74	-		0.8	V	All Inputs	
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA
ГОН	Output HIGH Current	54,74			1000	μΑ	V _{CC} = MIN, V _O	H = MAX
-011	Output mon current	54,74			50	μΑ	V _{CC} = MIN, V _O	H = 12 V
		54,74		0.25	0.4	V	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN$,
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
	1				20	μΑ	V _{CC} = MAX, V _I	N = 2.4 V
liH .	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V
IIL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V
ICC	Power Supply Current Total, Output HIGH Total, Output LOW				1.6	mA	V _{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25\,^{\circ}C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST COMPITIONS
31MBOL	FANAIVIETEN	MIN	TYP	MAX	UNITS	TEST CONDITIONS
tPLH	Turn Off Delay, Input to Output		17	32	ns	V _{CC} = 5.0 V
^t PHL	Turn On Delay, Input to Output		15	28	ns	$C_L = 15 \text{ pF}, R_L = 2.0 \text{ k}\Omega$





SN54LS27 SN74LS27

TRIPLE 3-INPUT NOR GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

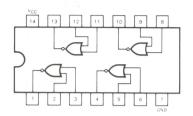
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
IOH	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DADAMETER	PARAMETER		LIMITS		UNITS	TEST	CNDITIONS
STIVIBUL	PARAIVIETER	1	MIN	TYP	MAX	UNITS	I IESI C	ONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage All Inputs	
.,		54			0.7	.,	Guaranteed Inp	ut LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	= -18 mA
VOH	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OI}	$H = MAX, V_{IN} = V_{IH}$
VOH	Output High Voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
.,		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V
lН	Input HIGH Current			,	0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V
ΊL	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_I$	N = 0.4 V
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
lcc	Power Supply Current Total, Output HIGH				4.0	mA	V _{CC} = MAX	
	Total, Output LOW				6.8			

CVMADOL	DADAMETED	LIMITS			LINUTC	TEST CONDITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH	Turn Off Delay, Input to Output		10	15	ns	V _{CC} = 5.0 V	
^t PHL	Turn On Delay, Input to Output		10	15	ns	$C_L = 15 pF$	





SN54LS28 SN74LS28

QUAD 2-INPUT NOR BUFFER

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

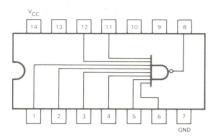
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-1.2	mA
lOL	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMBOL	PARAMETER			LIMITS		UNITS	TECT	CAIDITIONS
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST	CONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	out HIGH Voltage for
		54			0.7		Guaranteed Inp	out LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA
Voн	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OI}	$_{H} = MAX, V_{IN} = V_{IH}$
VOH	Output High Voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
		54,74		0.25	0.4	V	I _{OL} = 12 mA	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 24 mA V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	V _{CC} = MAX, V _I	N = 2.7 V
lН	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _I	N = 7.0 V
IIL	Input LOW Current	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V
los	Short Circuit Current		-30		-130	mA	V _{CC} = MAX	
lcc	Power Supply Current Total, Output HIGH Total, Output LOW				3.6	- mA	V _{CC} = MAX	
	Total, Output LOVV				13.8			

SYMBOL	PARAMETER	LIMITS			LIMITO	TEST COMPITIONS
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
^t PLH	Propagation Delay		12	24	ns	V _{CC} = 5.0 V
^t PHL	Propagation Delay		12	24	ns	$C_L = 45 \text{ pF}, R_L = 667 \Omega$





SN54LS30 SN74LS30

8-INPUT NAND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

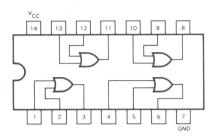
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		4 8	LIMITS		UNITS	TEST CONDITIONS	
STIVIBUL	PARAIVIETER	1	MIN	TYP	MAX	UNITS	TEST	CNDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
		54			0.7		Guaranteed Inp	ut LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA
VoH	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
V OH	Output mon voltage	74	2.7	3.5		V		
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V
ΙΗ	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _I	N = 7.0 V
I _I L.	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_I$	N = 0.4 V
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
Icc	Power Supply Current Total, Output HIGH Total, Output LOW		-		0.5	- mA	V _{CC} = MAX	

CVAADOL	DADAMETER	LIMITS			UNITS	TEST CONDITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
tPLH	Turn Off Delay, Input to Output		8.0	15	ns	V _{CC} = 5.0 V	
tPHL	Turn On Delay, Input to Output		13	20	ns	$C_L = 15 pF$	





SN54LS32 SN74LS32

QUAD 2-INPUT OR GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

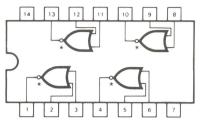
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DADAMETE			LIMITS		UNITS	TEST CONDITIONS		
STIVIBUL	PARAMETER	(MIN	TYP	MAX	UNITS	IEST	CNDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
		54			0.7	.,	Guaranteed Inp	ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA	
Voн	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{I}$ or V_{IL} per Truth Table		
VОН	Output High Voltage	74	2.7	3.5		V			
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN$,	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
IIL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V	
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current Total, Output HIGH				6.2	- mA	V _{CC} = MAX		
	Total, Output LOW				9.8				

SYMBOL	PARAMETER		LIMITS			TECT COMPITIONS	
STIVIBUL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH	Turn Off Delay, Input to Output		14	22	ns	V _{CC} = 5.0 V	
^t PHL	Turn On Delay, Input to Output		14	22	ns	$C_L = 15 pF$	





*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

SN54LS33 SN74LS33

QUAD 2-INPUT NOR BUFFER

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

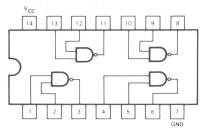
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
Тд	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
Voн	Output Voltage — High	54,74			5.5	V
lor	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

DADAMETER			LIMITS		LIMITO	TEST CONDITIONS	
PARAIVIETER	ı	MIN	TYP	MAX	UNITS	TEST	CNDITIONS
Input HIGH Voltage		2.0			V	Guaranteed Inp	out HIGH Voltage for
	54			0.7	.,		out LOW Voltage for
Input LOW Voltage	74			0.8	V	All Inputs	
Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA
Output HIGH Current	54,74			250	μΑ	$V_{CC} = MIN, V_{OH} = MAX$	
	54,74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN,
Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 24 mA	VIN = VIL or VIH per Truth Table
	•			20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V
Input HIGH Current				0.1	mA	V _{CC} = MAX, V _I	N = 7.0 V
Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V
Total, Output HIGH				3.6	- mA	V _{CC} = MAX	
	Input HIGH Voltage Input LOW Voltage Input Clamp Diode Voltage Output HIGH Current Output LOW Voltage Input HIGH Current Input HIGH Current Power Supply Current	Input LOW Voltage Input Clamp Diode Voltage Output HIGH Current Output LOW Voltage 74 Input LOW Voltage Input HIGH Current Input LOW Current Power Supply Current Total, Output HIGH	Input HIGH Voltage Input LOW Voltage Input Clamp Diode Voltage Output HIGH Current Output LOW Voltage Input LOW Voltage Input LOW Voltage Input HIGH Current Input HIGH Current Input LOW Current Power Supply Current Total, Output HIGH	PARAMETER	Name	Name	PARAMETER

CVAADOL	DADAMETED	LIMITS			UNITS	TEST CONDITIONS		
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
^t PLH	Turn Off Delay, Input to Output		20	32	ns	$V_{CC} = 5.0 \text{ V, R}_{L} = 667 \Omega$		
^t PHL	Turn On Delay, Input to Output		18	28	ns	C _L == 45 pF		





SN54LS37 SN74LS37

QUAD 2-INPUT NAND BUFFER

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
IOH	Output Current — High	54,74			-1.2	mA
lor	Output Current — Low	54 74			12 24	mA

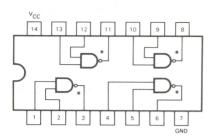
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	,		LIMITS		UNITS	TECT	CONDITIONS
STIVIBUL	PARAMETER	1	MIN	TYP	MAX	UNITS	TEST	CNDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp	out HIGH Voltage for
.,		54			0.7	.,		out LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA
Voн	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$
VОН	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
		54,74		0.25	0.4	V	I _{OL} = 12 mA	$V_{CC} = V_{CC} MIN$
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 24 mA	V _{IN} = V _{IL} or V _{IH} per Truth Table
					20	μΑ	V _{CC} = MAX, V	IN = 2.7 V
lН	Input HIGH Current				0.1	mA	V _{CC} = MAX, V	N = 7.0 V
4L	Input LOW Current				-0.4	mA	V _{CC} = MAX, V	IN = 0.4 V
los	Short Circuit Current		- 30		-130	mA	$V_{CC} = MAX$	
lcc	Power Supply Current Total, Output HIGH				2.0	mA	V _{CC} = MAX	
	Total, Output LOW		1		12			

AC CHARACTERISTICS: T_A = 25°C

	, .							
SYMBOL	PARAMETER	LIMITS		LIMITS		UNITS	TEST CONDITIONS	
STIVIBUL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
t _{PLH}	Turn Off Delay, Input to Output		12	24	ns	$V_{CC} = 5.0 \text{ V, R}_{L} = 667 \Omega$		
^t PHL	Turn On Delay, Input to Output		12	24	ns	$C_L = 45 \text{ pF}$		





*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

SN54LS38 SN74LS38

QUAD 2-INPUT NAND BUFFER

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

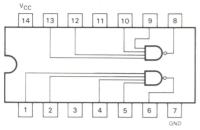
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
VOH	Output Voltage — High	54,74			5.5	V
IOL	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DADAMETER			LIMITS		LINITO	TECT	CAUDITIONIC
STIVIBUL	PARAMETER	ı	MIN	TYP	MAX	UNITS	TEST	CONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage f All Inputs	
		54			0.7		Guaranteed Inp	out LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN$, $I_{IN} = -18 \text{ mA}$	
ЮН	Output HIGH Current	54,74			250	μΑ	V _{CC} = MIN, V _C	OH = MAX
		54,74		0.25	0.4	V	I _{OL} = 12 mA	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 24 mA	V _{IN} = V _{IL} or V _{IH} per Truth Table
					20	μΑ	V _{CC} = MAX, V	IN = 2.4 V
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V
IIL	Input LOW Current		y		-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V
lcc	Power Supply Current Total, Output HIGH				2.0	mA	V _{CC} = MAX	eg 27 t
	Total, Output LOW				12			

SYMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS	1.2
STIVIBUL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH	Turn Off Delay, Input to Output		20	32	ns	$V_{CC} = 5.0 \text{ V, R}_{L} = 667 \Omega$	
^t PHL	Turn On Delay, Input to Output	-	18	28	ns	$C_L = 45 \text{ pF}$	





SN54LS40 SN74LS40

DUAL 4-INPUT NAND BUFFER

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-1.2	mA
lOL	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DADAMETER	PARAMETER		LIMITS		UNITS	TEST	ONDITIONS		
STIVIBUL	FARAIVIETER	١	MIN	TYP	MAX	UNITS	TEST	ONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage All Inputs			
V_{IL}		54			0.7	.,	Guaranteed Inp	ut LOW Voltage for		
	Input LOW Voltage	74			0.8	V	All Inputs	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$			
VoH	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _O	$H = MAX, V_{IN} = V_{IH}$		
VOH	Output High Voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table		
	Output LOW Voltage	54,74		0.25	0.4	V	I _{OL} = 12 mA	$V_{CC} = V_{CC} MIN,$		
VOL		74		0.35	0.5	V	I _{OL} = 24 mA	V _{IN} = V _{IL} or V _{IH} per Truth Table		
	1				20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$			
lн	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V		
ΊL	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_I$	N = 0.4 V		
los	Short Circuit Current	-30		-130	mA	V _{CC} = MAX				
Power Supply Current Total, Output HIGH					1.0	mA	V _{CC} = MAX			
	Total, Output LOW				6.0	1111/4	VCC - IVIAX			

AC CHARACTERISTICS: $T_A = 25 \, ^{\circ} C$

SYMBOL	PARAMETER		LIMITS		LINUTC	TEST COMPLETIONS				
STIVIBOL	FARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS				
^t PLH	Turn Off Delay, Input to Output		12	24	ns	$V_{CC} = 5.0 \text{ V}, R_L = 667 \Omega$				
^t PHL	Turn On Delay, Input to Output		12	24	ns	$C_L = 45 pF$				



DESCRIPTION — The LSTTL/MSI SN54LS/74LS42 is a Multipurpose Decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs. The LS42 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- MULTI-FUNCTON CAPABILITY
- MUTUALLY EXCLUSIVE OUTPUTS
- DEMULTIPLEXING CAPABILITY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

SN54LS42 SN74LS42

ONE-OF-TEN DECODER

LOW POWER SCHOTTKY

PIN NAMES

LOADING	G (Note a)
HIGH	LOW
0.5 U.L.	0.25 U.L.

10 U.L. 5(2.5) U.L.

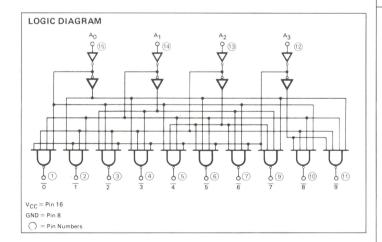
 $\frac{A_0 - A_3}{0 \text{ to } 9}$ Address Inputs Outputs, Active

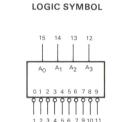
Outputs, Active LOW (Note b)

NOTES:

a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74)
Temperature Rances.





 $V_{CC} = Pin 16$ GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

NOTE:

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS42 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with LOW input enables.

The logic design of the LS42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input A_3 produces a useful inhibit function when the LS42 is used as a one-of-eight decoder. The A_3 input can also be used as the Data input in an 8-output demultiplexer application.

TRUTH TABLE

A ₀	Α1	Α2	А3	ō	<u>1</u>	<u>-</u> 2	3	4	5	<u>6</u>	7	8	9
L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
н	L	L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н
L	Н	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н
н	Н	L	L	Н	Н	Н	L	Н	Н	Н	Н	Н	Н
L	L	Н	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
н	L	Н	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	Н	Н	н	Н	Н	Н	Н	Н	Н	H,	Н	Н
н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
н	Н	Н	Н	н	Н	Н	Н	Н	Н	Н	Н	Н	Н

H = HIGH Voltage Level L = LOW Voltage Level

GUARANTEED OPERATING RANGES

GOAIDAITE	D OI EIGHING IGHGES					
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMADOL	DADAMETER		LIMITS		LINUTC	TEGT CONDITIONS					
SYMBOL	PARAMETER	PARAIVIETER			MAX	UNITS	TEST CONDITIONS				
VIH	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage f					
		54			0.7	.,		ut LOW Voltage for			
V _{IL} Inpu	Input LOW Voltage	74			0.8	V	All Inputs				
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} =-18 mA				
Vон	Output HIGH Voltage		2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$			
VOH	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Truth Table				
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN$,			
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table			
					20	μΑ	V _{CC} = MAX, V _I	N = 2.7 V			
IH	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V			
IL	Input LOW Current	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V			
OS	Short Circuit Current	-20		-100	mA	$V_{CC} = MAX$					
СС	Power Supply Current				13	mA	$V_{CC} = MAX$				

AC CHARACTERISTICS: $T_A = 25$ °C

SYMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS			
	PARAIVIETER	MIN	TYP	MAX	UNITS				
tPLH tPHL	Propagation Delay (2 Levels)		15 15	25 25	ns	Fig. 2	V _{CC} = 5.0 V		
^t PLH ^t PHL	Propagation Delay (3 Levels)		20 20	30 30	ns	Fig. 1	C _L = 15 pF		

AC WAVEFORMS

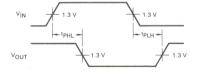


Fig. 1

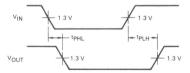


Fig. 2

MOTOROLA

DESCRIPTION — The SN54LS/74LS47 are Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN54LS/74LS47 are designed to withstand the relatively high voltages required for 7-segment indicators.

These outputs will withstand 15 V with a maximum reverse current of 250 μ A. Indicator segments requiring up to 24 mA of current may be driven directly from the SN74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The SN54LS/74LS47 incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time which the BI/RBO node is a HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity or to inhibit the outputs.

- LAMP INTENSITY MODULATION CAPABILITY
- OPEN COLLECTOR OUTPUTS
- LAMP TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

PIN NAMES

LOADING (Note a)

		HIGH	LOW
A, B, C, D	BCD Inputs	0.5 U.L.	0.25 U.L.
RBI	Ripple Blanking Input	0.5 U.L.	0.25 U.L.
LT	Lamp Test Input	0.5 U.L.	0:25 U.L.
BI/RBO	Blanking Input or	0.5 U.L.	0.75 U.L.
	Ripple Blanking Output	1.2 U.L.	2.0 U.L.
ā, to g	Outputs	Open-Collector	15 (7.5) U.L.

Notes:

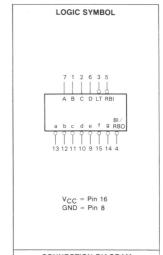
- a) 1 Unit Load (U.L.) = 40 μ A HIGH, 1.6 mA LOW
- b) Output current measured at $V_{OUT} = 0.5 \text{ V}$

Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges,

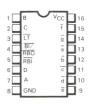
SN54LS47 SN74LS47

BCD TO 7-SEGMENT DECODER/DRIVER

LOW POWER SCHOTTKY

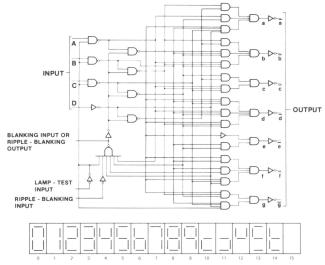






J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

LOGIC DIAGRAM



NUMERICAL DESIGNATIONS - RESULTANT DISPLAYS

TRUTH TABLE

	$\overline{}$		- 115	IPUT	5		$\neg \setminus / \neg$		(OUTP	UIS			/	
DECIMAL OR FUNCTION	ĒΤ	RBI	D	С	В	А	BI/RBO	a a	b	c	d	e	f	g	NOTE
0	н	Н	L	L	L	L	н	L	L	L	L	L	L	Н	А
1	Н	X	L	L	L	н	Н	Н	L	L	Н	Н	Н	Н	A
2	Н	Х	L	L	Н	L	Н	L	L	н	L	L	Н	L	
3	Н	Х	L	L	н	Н	Н	L	L	L	L	н	н	L	
4	Н	Х	L	Н	L	L	Н	н	L	L	Н	Н	L	L	
5	Н	Х	L	Н	L	Н	Н	L	Н	L	L	Н	L	L	
6	Н	Х	L	Н	Н	L	Н	Н	Н	L	L	L	L	L	
7	Н	X	L	Н	Н	Н	Н	L	L	L	Н	Н	Н	Н	
8	Н	Х	н	L	L	L	Н	L	L	L	L	L	L	L	
9	Н	Х	н	L	L	н	Н	L	L	L	Н	Н	L	L	
10	Н	Х	Н	L	Н	L	Н	Н	Н	Н	L	L	Н	L	
11	Н	Х	н	L	Н	н	Н	Н	Н	L	L	Н	Н	L	
12	Н	X	Н	Н	L	L	Н	Н	L	Н	Н	Н	L	L	
13	Н	Х	Н	Н	L	Н	Н	L	Н	Н	L	Н	L	L	
14	Н	Х	Н	Н	Н	L	Н	Н	Н	Н	L	L	L	L	
15	Н	X	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	
BI	· X	×	Х	Х	Х	Х	L	Н	Н	Н	Н	Н	Н	Н	В
RBI	Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	С
LT	L	Х	X	Х	X	X	Н	L	L	L	L	L	L	L	D

- (A) $\overline{\text{BI/RBO}}$ is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output ($\overline{\text{RBO}}$). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input $(\overline{\mathsf{RBI}})$ must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.
- (B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.
- (C) When ripple-blanking input (\overline{RBI}) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).
- (D) When the blanking input/ripple-blanking output ($\overline{B1/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High BI/RBO	54,74			-50	μΑ
lOL	Output Current — Low BI/RBO BI/RBO	54 74			1.6 3.2	mA
VO (off)	Off-State Output Voltage a to g	54,74			15	V
IO (on)	On-State Output Current \overline{a} to \overline{g} \overline{a} to \overline{g}	54 74			12 24	mA

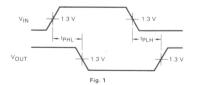
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

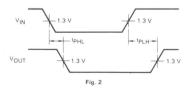
SYMBOL	DADAMETER			LIMITS		UNITS	TEST CONDITIONS
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
VIL	Input LOW Voltage	54 74			0.7 0.8	V	Guaranteed Input LOW Threshold Voltage for All Inputs
VIK	Input Clamp Diode Voltag	е		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$
Vон	Output HIGH Voltage, BI/	RBO	2.4	4.2		V	$V_{CC} = MIN$, $I_{OH} = -50 \mu A$, $V_{IN} = V_{IN}$ or V_{IL} per Truth Table
V/0:	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 1.6 \text{ mA}$ $V_{CC} = MIN, V_{IN} = V_{IN}$
VOL	BI/RBO	74		0.35	0.5	V	I _{OL} = 3.2 MA or V _{IL} per Truth Table
IO (off)	Off-State Output Current ā thru g				250	μΑ	$V_{CC} = MAX$, $V_{IN} = V_{IN}$ or V_{IL} per Truth Table, V_{O} (off) = 15 V
	On-State Output Voltage	54,74		0.25	0.4	V	$I_{O(on)} = 12 \text{ mA} V_{CC} = MAX, V_{IN} = V_{IH}$
V _O (on)	ā thru g	74		0.35	0.5	V	I _O (on) = 24 MA or V _{IL} per Truth Table
					20	μΑ	$V_{CC} = MAX, V_{IN} = 2.7 V$
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$
IIL	Input LOW Current BI/RE Any Input except BI/RBO				-1.2 -0.4	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$
IOS BI/RBO	Output Short Circuit Curr	ent	-0.3		-2.0	mA	V _{CC} = MAX, V _{OUT} = 0 V
Icc	Power Supply Current			7.0	13	mA	$V_{CC} = MAX$

AC CHARACTERISTICS: $T_{\mbox{\scriptsize A}} = 25 \ensuremath{^{\circ}}\mbox{\scriptsize C}$

SYMBOL	PARAMETER		LIMITS		UNITS	TECT COMPLICATION
STIVIBUL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
^t PHL ^t PLH	Propagation Delay, Address Input to Segment Output			100 100	ns ns	V _{CC} = 5.0 V
^t PHL ^t PLH	Propagation Delay, RBI Input To Segment Output			100 100	ns ns	$C_L = 15 pF$

AC WAVEFORMS





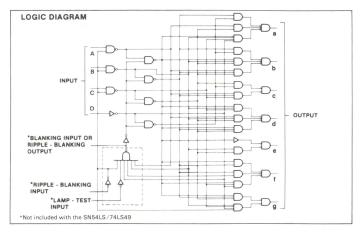
MOTOROLA

DESCRIPTION — The SN54LS/74LS48 and SN54LS/74LS49 are BCD to 7-Segment Decoders consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. The LS49 offers active HIGH open-collector outputs for current-sourcing applications to drive logic circuits or discrete, active components. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking input for the LS48. Four NAND gates and four input buffers provide BCD data and its complement and a buffer provides blanking input for the LS49.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive other components. The relative positive logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables.

The LS48 circuit incorporates automatic leading and/or trailing edge zero-blanking control (RBI and RBO). Lamp Test (LT) may be activated any time when the BI/RBO node is HIGH. Both devices contain an overriding blanking input (BI) which can be used to control the lamp intensity or to inhibit the outputs.

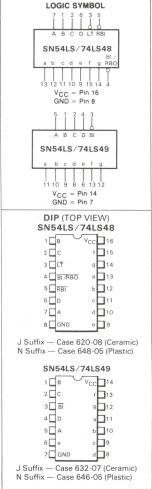
- LAMP INTENSITY MODULATION CAPABILITY
- INTERNAL PULL-UPS ELIMINATE NEED FOR EXTERNAL RESISTORS ON SN54LS/74LS48
- OPEN COLLECTOR OUTPUTS ON SN54LS/74LS49
- INPUT CLAMP DIODES ELIMINATE HIGH-SPEED TERMINATION EFFECTS



SN54LS/74LS48 SN54LS/74LS49

BCD TO 7-SEGMENT DECODER

LOW POWER SCHOTTKY



PIN NAMES

LOADING (Note a)

		HIGH	LOW
A, B, C, D,	BCD Inputs	0.5 U.L. 0.5 U.L.	0.25 U.L. 0.25 U.L.
RBI	Ripple Blanking (Active Low) Input	0.5 U.L.	0.25 U.L.
LT BI/RBO	Lamp Test (Active Low) Input Blanking Input or Ripple	0.5 U.L. 1.2 U.L.	0.75 U.L. 2(1) U.L.
BI	Blanking Output (Active Low)	0.5 U.L.	0.25 U.L.
a to g	Blanking (Active Low) Input Outputs (Note b)	Open Collector Open Collector	3.75 (1.25) U.L. (48) 5 (2.5) U.L. (49)

NOTES:

- a) Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW
- b) Output current measured at V_{OUT} = 0.5 V Output LOW drive factor is SNS4LS/74LS48: 1.25 U.L. for Military (54), 3.75 U.L. for Commercial (74). SNS4LS/74LS49: 2.5 U.L. for Military (54), 5 U.L. for Commercial (74) Temperature Ranges.



NUMERICAL DESIGNATIONS - RESULTANT DISPLAYS

TRUTH TABLE SN54LS/74LS48

	_		11	NPUT	s —		$\neg \neg$		_	DUT	PUTS	_	_		
DECIMAL OR FUNCTION	ĒΤ	RBI	D	С	В	А	BI/RBO	a	ь	с	d	е	f	9	NOT
0	Н	н	L	L	L	L	н	Н	н	н	Н	н	н	L	1
1	Н	Х	L	L	L	н	н	L	н	н	L	L	L	L	1
2	Н	Х	L	L	Н	L	Н	н	н	L	н	Н	L	н	
3	н	X	L	L	н	н	н	Н	Н	н	н	L	L	Н	
4	Н	X	L	н	L	L	Н	L	н	н	L	L	н	Н	
5	н	X	L	н	L	н	Н	Н	L	н	н	L	н	Н	
6	Н	X	L	н	н	L	Н	L	L	н	Н	н	н	Н	
7	н	X	L	н	н	н	Н	н	н	н	L	L	L	L	
8	н	X	Н	L	L	L	н	н	н	н	н	н	н	Н	
9	Н	X	н	L	L	н	н	н	н	н	L	L	н	Н	
10	Н	X	н	L	н	L	н	L	L	L	н	н	L	Н	
11	н	X	н	L	Н	н	Н	L	L	н	н	L	L	Н	
12	н	X	н	н	L	L	Н	L	н	L	L.	L	н	н	
13	Н	X	Н	н	L	н	Н	Н	L	L	Н	L	Н	Н	
14	н	X	н	н	Н	L	Н	L	L	L	н	н	н	Н	
15	Н	X	Н	Н	н	н	н	L	L	L	L	L	L	L	
Bī	X	X	Х	X	Х	Х	L	L	L	L	L	L	L	L	2
RBI	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	3
ĒΤ	L	×	Х	X	X	X	Н	н	н	н	н	н	н	Н	4

TRUTH TABLE SN54LS/74LS49

	_	-11	NPUT	s—	7/			OUT	PUTS	-		_	
DECIMAL OR FUNCTION	D	С	В	А	BĪ	a	ь	с	d	e	f	9	NOTE
0	L	L	L	L	н	н	н	н	н	н	н	L	1
1	L	L	L	н	н	L	н	н	L	L	L	L	
2	L	L	н	L	Н	н	Н	L	н	н	L	н	
3	L	L	н	н	Н	н	н	н	н	L	L	н	
4	L	н	L	L	Н	L	Н	н	L	L	н	н	
5	L	н	L	н	н	н	L	Н	н	L	н	н	
6	L	н	н	L	Н	L	L	н	н	Н	н	н	
7	L	н	н	н	Н	н	Н	Н	L	L	L	L	
8	Н	L	L	L	н	н	Н	Н	н	н	н	н	
9	Н	L	L	н	Н	н	н	н	L	L	н	Н	
10	Н	L	н	L	Н	L	L	L	н	н	L	н	
11	н	L	н	н	Н	L	L	н	н	L	L	Н	
12	н	н	L	L	н	L	н	L	L	L	н	Н	
13	Н	н	L	н	н	н	L	L	н	L	н	н	
14	Н	Н	Н	L	н	L	L	L	н	н	Н	Н	
15	Н	н	н	н	н	L	L	L	L	L	L	L	
BI	×	×	×	X	L	L	L	L	L	L	L	L	2

NOTES:

- (1) $\overline{BI/RBO}$ is wired-AND logic serving as blanking input $\overline{(BI)}$ and/or ripple-blanking output (RBO). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and rippleblanking input (RBI) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X=input may be HIGH or LOW.
- (2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.
- (3) When ripple-blanking input (RBI) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).
- (4) When the blanking input/ripple-blanking output (BI/ RBO) is open or held at a HIGH level, and a LOW level is applied to lamp-test input, all segment outputs go to a LOW level.

NOTES:

- (1) The blanking input must be open or held at a HIGH level when output functions 0 through 15 are desired.
- (2) When a LOW level is applied to the blanking input all segment outputs go to a LOW level regardless of the state of any other input condition. X = input may be HIGH or LOW.
- H = HIGH Voltage Level L = LOW Voltage Level
- X = Immaterial

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
VCC	Supply Voltage		54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperatur	re Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High a to	οg	54,74		7	-100	μΑ
ГОН	Output Current — High BI/	RBO	54,74			-50	μΑ
loL	Output Current — Low ā to	g	54 74			2.0 6.0	mA
lOL		RBO RBO	54 74			1.6 3.2	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	,		LIMITS		UNITS	TECT	CONDITIONS
STIVIBOL	PARAMETER	(MIN	TYP	MAX	UNITS	IESI	CONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for
VIL	Input LOW Voltage	54 74	,		0.7	V	Guaranteed In All Inputs	put LOW Voltage for
VIK	Input Clamp Diode Volta				-1.5	V	V _{CC} = MIN, I _{II}	N = −18 mA
VOH	Output HIGH Voltage		2.4	4.2		μΑ	$V_{CC} = MIN, I_{C}$ $V_{IN} = V_{IH}$ or U_{IN}	$_{ m DH} = -50\mu{ m A}$, J.L. per Truth Table
10	Output Current ā to g		-2.0	-1.3		mA	V _{CC} = MIN, V Input Condition	
	Output LOW Voltage	54,74			0.4	V	$I_{OL} = 2.0 \text{ mA}$	V _{CC} =MIN, V _{IH} =2.0 V
VOL	ā to \overline{g}	74			0.5	V	$I_{OL} = 6.0 \text{ mA}$	V _{IL} = V _{IL} MAX
	Output LOW Voltage	54,74			0.4	V	I _{OL} = 1.6 mA	V _{CC} =MAX, V _{IH} =2.0 V
VOL	BI/RBO	74			0.5	V	$I_{OL} = 3.2 \text{ mA}$	VIL = VIL MAX
	Input HIGH Current	•			20	μΑ	V _{CC} = MAX, \	/ _{IN} = 2.7 V
lН	(Except BI/RBO)				0.1	mA	V _{CC} = MAX, \	$I_{1N} = 7.0 \text{ V}$
IIL	Input LOW Current (Exc	ept BI/RBO)			-0.4	mA	V _{CC} = MAX, V	/IN = 0.4 V
ΙL	Input LOW Current BI/I	RBO			-1.2	mA	V _{CC} = MAX, V	/IN = 0.4 V
lcc	Power Supply Current			25	38	mA	$V_{CC} = MAX$	

AC CHARACTERISTICS: $V_{CC} = 5.0 \text{ V}$ $T_A = 25^{\circ}\text{C}$

CVAAROU	PARAMETER		LIMITS		UNITS	TEST CONDITIONS
SYMBOL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
^t PHL	Propagation delay time, HIGH-to- LOW level output from A Input			100	ns	$C_{I} = 15 \text{ pF, } R_{I} = 4.0 \text{ k}\Omega$
^t PLH	Propagation delay time, LOW-to- HIGH level output from A Input		4	100	ns	o_ 10 p1, n_ 4.0 k2
^t PHL	Propagation delay time, HIGH-to- LOW level output from RBI Input			100	ns	$C_{I} = 15 \text{ pF, } R_{I} = 6.0 \text{ k}\Omega$
^t PLH	Propagation delay time, LOW-to- HIGH level output from RBI Input			100	ns	CL = 13 pr, nL = 6.0 kt2

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
Voн	Output Voltage — High	54,74			5.5	V
lOL	Output Current — Low	54 74			4.0 8.0	mA

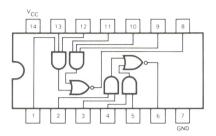
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMETED			LIMITS		LINUTO	TECT COMPITIONS
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
		54			0.7	V	0
VIL	Input LOW Voltage	74			0.8	V	Guarantee Input LOW Voltage
VIK	Input Clamp Diode Volta	ige			-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
ГОН	Output HIGH Current				250	μΑ	$V_{CC} = MIN, V_{IH} = 2.0 V$ $V_{IL} = V_{IL} MAX, V_{OH} = 5.5 V$
		54,74			0.4	V	I _{OL} = 4.0 mA V _{CC} = MIN, V _{IH} = 2.0 V
VOL	Output LOW Voltage	74			0.5	V	I _{OL} = 8.0 mA V _{IL} = V _{IL} MAX
lн Пн	Input Current HIGH				20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$
'IH	Input current riidri				0.1	mA	$V_{CC} = MAX, V_{IN} = 7.0 V$
IIL	Input Current LOW				-0.4	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$
lcc	Power Supply Current			8.0	15	mA	V _{CC} = MAX

AC CHARACTERISTICS: $V_{CC} = 5.0 \text{ V}$, $TA = 25^{\circ}$

SYMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS
STIVIBUL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
[†] PHL	Propagation delay time, HIGH-to- LOW level output from A Input			100	ns	C: = 15 -5 P: = 2010
^t PLH	Propagation delay time, LOW-to- HIGH level output from A Input			100	ns	$C_L = 15 \text{ pF}, R_L = 2.0 \text{ k}\Omega$
^t PHL	Propagation delay time, HIGH-to- LOW level output from RBI Input			100	ns	C. = 15 pc P. = 60k0
^t PLH	Propagation delay time, LOW-to- HIGH level output from RBI Input			100	ns	$C_L = 15 \text{ pF}, R_L = 6.0 \text{ k}\Omega$





J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

SN54LS51 SN74LS51

DUAL 2-WIDE 2-INPUT/ 3-INPUT AND-OR-INVERT GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
Vcc	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	٧
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
IOH	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

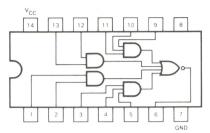
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST	ONDITIONS	
STIVIBUL	PARAMETER		MIN	TYP	MAX	UNITS	TEST	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
		54			0.7			ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA		
VoH	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{II}$		
VOH	Output High Voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
IL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V	
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$		
lcc	Power Supply Current Total, Output HIGH Total, Output LOW				1.6	- mA	V _{CC} = MAX		

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX	UNITS	TEST CONDITIONS
^t PLH	Turn Off Delay, Input to Output		12	20	ns	V _{CC} = 5.0 V
^t PHL	Turn On Delay, Input to Output		12.5	20	ns	C _L = 15 pF





J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

SN54LS54 SN74LS54

3-2-2-3-INPUT AND-OR-INVERT GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

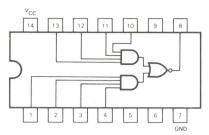
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST	ONDITIONS	
STIVIBUL	PARAMETER	1	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
		54			0.7	.,		ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA		
VOH	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN$, $I_{OH} = MAX$, $V_{IN} = V_{II}$		
VOH	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
V _{OL}	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
IIL	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_I$	N = 0.4 V	
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
Icc	Power Supply Current Total, Output HIGH				1.6	- mA	V _{CC} = MAX		
	Total, Output LOW				2.0		100		

AC CHARACTERISTICS: TA = 25°C

SYMBOL			LIMITS			TEGT COMPLETIONS
	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
tPLH	Turn Off Delay, Input to Output		12	20	ns	V _{CC} = 5.0 V
tPHL	Turn On Delay, Input to Output		12.5	20	ns	$C_L = 15 pF$

MOTOROLA



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

SN54LS55 SN74LS55

2-WIDE 4-INPUT AND - OR - INVERT GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMADOL	DL PARAMETER			LIMITS		LINUTC	TEST CONDITIONS		
SYMBOL	PARAIVIETER	ı	MIN	TYP	MAX	UNITS	IESTC	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
		54			0.7		Guaranteed Inp	ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN}$	=-18 mA	
Voн	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH}$		
VOH	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table	
		54,74		0.25	0.4	٧	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
IIL	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_I$	N = 0.4 V	
los	Short Circuit Current	Short Circuit Current			-100	mA	$V_{CC} = MAX$		
ICC	Power Supply Current Total, Output HIGH Total, Output LOW				0.8	mA	V _{CC} = MAX		

AC CHARACTERISTICS: T_A = 25°C

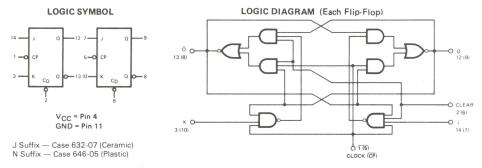
CVAADOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
tPLH	Turn Off Delay, Input to Output		12	20	ns	V _{CC} = 5.0 V	
^t PHL	Turn On Delay, Input to Output		12.5	20	ns	$C_L = 15 pF$	



DESCRIPTION — The SN54LS/74LS73A offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

SN54LS73A SN74LS73A

DUAL JK NEGATIVE
EDGE-TRIGGERED FLIP-FLOP
LOW POWER SCHOTTKY



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMET	- F.D.	LIMITS			LINITO	TECT	CONDITIONS	
SYMBOL	PARAMET	EK	MIN	TYP	MAX	UNITS	TEST	CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Ing All Inputs	out HIGH Voltage for	
		54			0.7	.,		out LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	ge		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
Voн	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{II}$ or V_{IL} per Truth Table		
VОН	Output man voltage	74	2.7	3.5		V			
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$		
OL Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA V _{IN} = V _{IL} or V _I per Truth Table			
lін	Input HIGH Current	J, K Clear Clock			20 60 80	μΑ	$V_{CC} = MAX, V_{IN} = 2.7 V$ $V_{CC} = MAX, V_{IN} = 7.0 V$		
ın	mpattingin darroit	J, K Clear Clock			0.1 0.3 0.4	mA			
l _{IL}	Input LOW Current	J, K Clear, Clock			-0.4 -0.8	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$		
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current				6.0	mA	$V_{CC} = MAX$		

MODE SELECT - TRUTH TABLE

OPERATING MODE		INPUTS		OUTPUTS		
OFENATING MODE	\overline{c}_D	J	K	Q	ā	
Reset (Clear)	L	X	Х	L	н	
Toggle	н	h	h	q	q	
Load "0" (Reset)	н	1	h	L	н	
Load "1" (Set)	н	h	1 .	Н	L	
Hold	н	1	1	q	q	

 $\begin{array}{l} {\rm H,\ h=HIGH\ Voltage\ Level} \\ {\rm L,\ I=LOW\ Voltage\ Level} \end{array}$

X = Don't Care

I, h(q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	٧
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

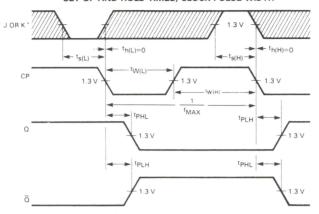
	/ 00							
CVMPOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS		
SYMBOL	PARAMETER	MIN	TYP	MAX	ONITS	TEST CONDITIONS		
fMAX	Maximum Clock Frequency	30	45		MHz	Fig. 1	$V_{CC} = 5.0 \text{ V}$	
tPLH	Propagation Delay,		15	20	ns	Fig. 1	$C_{\rm L} = 15 \rm pF$	
tPHL	Clock to Output		15	20	ns	1.19.1	OL 10 bi	

AC SETUP REQUIREMENTS: TA = 25°C

SYMBOL	PARAMETER		LIMITS			TEGT COMPLETIONS		
		MIN	TYP	MAX	UNITS	TEST CONDITIONS		
tw	Clock Pulse Width High	20			ns	Fig. 1		
tw	Set Pulse Width	25			ns	Fig. 2	V F 0 V	
t _S	Setup Time	20			ns	Fig. 1	$V_{CC} = 5.0 \text{ V}$	
th	Hold Time	0			ns	rig. i		

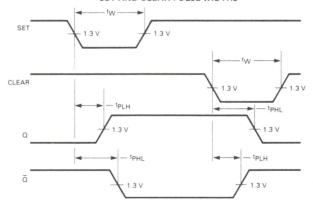
AC WAVEFORMS

Fig. 1 CLOCK TO OUTPUT DELAYS, DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH



^{*}The shaded areas indicate when the input is permitted to change for predicatable output performance.

Fig. 2 SET AND CLEAR TO OUTPUT DELAYS, SET AND CLEAR PULSE WIDTHS





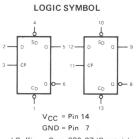
DESCRIPTION - The SN54LS/74LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and $\overline{\mathbf{Q}}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

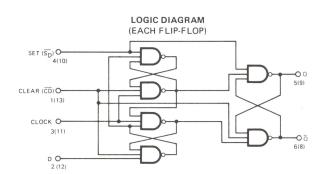
SN54LS74A SN54LS74A

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS		
STIVIBUL	PARAIVIETER		MIN	TYP	MAX	UNITS	TEST	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
		54			0.7	.,		ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	= -18 mA	
VOH	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$	
VOH	o stps:dii voitage	74	2.7	3.5		V	or V _{IL} per Truth	Table	
		54,74		0.25	0.4	V			
VOL	Output LOW Voltage	74		0.35	0.5	V		V _{IN} = V _{IL} or V _{IH} per Truth Table	
	Input High Current Data, Clock Set, Clear				20 40	μΑ	V _{CC} = MAX, V _I	N = 2.7 V	
lН	Data, Clock Set, Clear				0.1 0.2	mA	V _{CC} = MAX, V	N = 7.0 V	
ΊL	Input LOW Current Data, Clock Set, Clear				-0.4 -0.8	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$		
los	Output Short Circuit Cu	irrent	-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current				8.0	mA	V _{CC} = MAX		

MODE SELECT — TRUTH TABLE

		INPUTS	1 5 5	OUT	PUTS
OPERATING MODE	SD	CD	D	Q	ā
Set	L	Н	X	Н	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	Н	H
Load "1" (Set)	Н	Н	h	Н	L
Load "O" (Reset)	Н	Н	- 1	L	Н

*Both outputs will be HIGH while both \overline{S}_D and \overline{C}_D are LOW, but the output states are unpredictable if \overline{S}_D and \overline{C}_D go HIGH simultaneously.

 $\begin{array}{l} \text{H,h} = \text{HIGH Voltage Level} \\ \text{L,I} = \text{LOW Voltage Level} \\ \text{X} = \text{Don't Care} \end{array}$

I, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74	110000		4.0 8.0	mA.

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

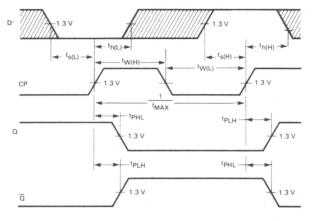
SYMBOL	PARAMETER		LIMITS		LINUTC		TEST CONDITIONS
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS		TEST CONDITIONS
fMAX	Maximum Clock Frequency	25	33		MHz	Fig. 1	Vac = 5.0 V
tPLH	Clock, Clear, Set to Output		13	25	ns	Fig. 1	$V_{CC} = 5.0 \text{ V},$ $C_{L} = 15 \text{ pF}$
^t PHL			25	40	ns		

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS		
	PARAMETER	MIN	TYP	MAX	UNITS			
t _W (H)	Clock	25			ns	Fig. 1		
tW(L)	Clear, Set	25			ns	Fig. 2		
ts	Data Setup Time — HIGH	20			ns	Eig 1	$V_{CC} = 5.0 \text{ V}$	
	LOW	20			ns	Fig. 1		
t _h	Hold Time	5.0			ns	Fig. 1		

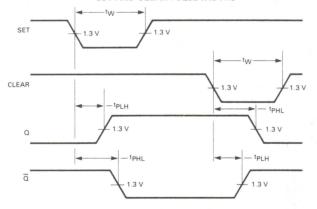
AC WAVEFORMS

Fig. 1 CLOCK TO OUTPUT DELAYS,
DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH



 $^{{}^{\}star}\mathsf{The}\,\mathsf{shaded}\,\mathsf{areas}\,\mathsf{indicate}\,\mathsf{when}\,\mathsf{the}\,\mathsf{input}\,\mathsf{is}\,\mathsf{permitted}\,\mathsf{to}\,\mathsf{change}\,\mathsf{for}\,\mathsf{predicatable}\,\mathsf{output}\,\mathsf{performance}.$

Fig. 2 SET AND CLEAR TO OUTPUT DELAYS, SET AND CLEAR PULSE WIDTHS





DESCRIPTION — The TTL/MSI SN54LS/74LS75 and SN54LS/74LS77 are latches used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the Enable is HIGH and the Q output will follow the data input as long as the Enable remains HIGH. When the Enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the Enable is permitted to go HIGH.

The SN54LS/74LS75 features complementary Ω and $\overline{\Omega}$ output from a 4-bit latch and is available in the 16-pin packages. For higher component density applications the SN54LS/74LS77 4-bit latch is available in the 14-pin package with $\overline{\Omega}$ outputs omitted.

SN54LS/74LS75 SN54LS/74LS77

4-BIT D LATCH

LOW POWER SCHOTTKY

LOADING (Note a)

PIN NAN	MES	HIGH	LOW
D_1-D_4	Data Inputs	0.5 U.L.	0.25 U.L.
E_{0-1}	Enable Input Latches 0, 1	2.0 U.L.	1.0 U.L.
E_{2-3}	Enable Input Latches 2, 3	2.0 U.L.	1.0 U.L.
Q_{1} Q_{4}	Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q_1}_{-}\overline{Q_4}$	Complimentary Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

Notes:

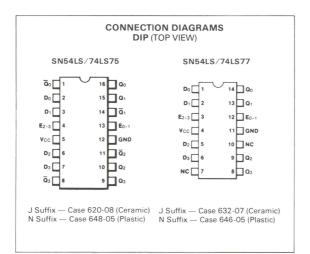
- a. 1 Unit Load (U.L.) = 40 μ A HIGH
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

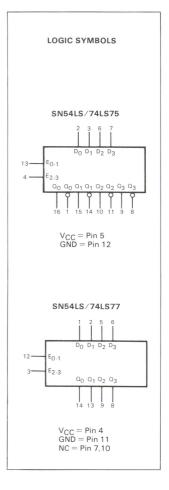
TRUTH TABLE

(=40	1 101011)
tn	t _{n+1}
D	Q
н	н
L	L

NOTES

 t_n = bit time before enable negative-going transition t_{n+1} = bit time after enable negative-going transition





DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS			TEST CONDITIONS		
STIVIBUL	PARAIVIET	=N	MIN	TYP	MAX	UNITS	TEST C	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	Guaranteed Input HIGH Voltage for All Inputs	
	1	54			0.7			ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	ge		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA		
Voн	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _O	$H = MAX, V_{IN} = V_{IH}$	
VОН	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table	
VOL	Output LOW Voltage	54,74		0.25	0.4	V	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN$, $V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table	
VOL	Output LOVV Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$		
I _I H	Input HIGH Current	D Input E Input			20 80	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
-111		D Input E Input			0.1 0.4	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
IIL	Input LOW Current	D Input E Input			-0.4 -1.6	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$		
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current				12	mA	$V_{CC} = MAX$		

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS
STIVIBUL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
^t PLH ^t PHL	Propagation Delay, Data to Ω		15 9.0	27 17	ns	
^t PLH ^t PHL	Propagation Delay, Data to $\overline{\mathbb{Q}}$		12 7.0	20 15	ns	V _{CC} = 5.0 V
^t PLH ^t PHL	Propagation Delay, Enable to Q		15 14	27 25	ns	C _L = 15 pF
^t PLH ^t PHL	Propagation Delay, Enable to $\overline{\mathbb{Q}}$		16 7.0	30 15	ns	

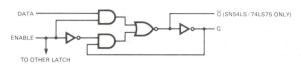
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMBOL	DADAMET	PARAMETER		LIMITS		UNITS	TEST CONDITIONS		
SYMBOL	PARAMET	=K	MIN	TYP	MAX	UNITS	IESI C	CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	Guaranteed Input HIGH Voltage for All Inputs	
	Innut I OW/ Valence	54			0.7	.,		out LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	ge		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = −18 mA		
V/0	Output HIGH Voltage	54	2.5	3.5		V		H = MAX, VIN = VIH	
VOH	Output High voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table	
VOL	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	VIN = VIL or VIH per Truth Table	
lн	Input HIGH Current	D Input E Input			20 80	μΑ	V _{CC} = MAX, V	IN = 2.7 V	
чн	par mon canon	D Input E Input			0.1 0.4	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$		
lıL	Input LOW Current	D Input E Input			-0.4 -1.6	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$		
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$		
lcc	Power Supply Current				13	mA	V _{CC} = MAX		

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER	LIMITS			UNITS	TECT COMPITIONS	
		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH ^t PHL	Propagation Delay, Data to Q		11 9.0	19 17	ns	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 15 \text{ pF}$	
tPLH tPHL	Propagation Delay, Enable to Q		10 10	18 18	ns		

LOGIC DIAGRAM



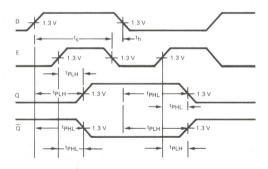
GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
Vcc	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lor	Output Current — Low	54 74			4.0 8.0	mA

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

CVMPOL	PARAMETER		LIMITS			TECT COMPLETIONS	
SYMBOL		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
tw	Enable Pulse Width High	20			ns		
t _S	Setup Time	20			ns	$V_{CC} = 5.0 \text{ V}$	
th	Hold Time	0			ns		

AC WAVE FORMS



DEFINITION OF TERMS:

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_{H}) — is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.



DESCRIPTION — The SN54LS/74LS76A offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW clock transitions.

SN54LS76A SN74LS76A

DUAL JK FLIP-FLOP WITH SET AND CLEAR

LOW POWER SCHOTTKY

MODE SELECT - TRUTH TABLE

OPERATING MODE		OUTPUTS				
	SD	¯c _D	J	К	Q	Q
Set Reset (Clear) *Undetermined Toggle Load "0" (Reset) Load "1" (Set) Hold		HLLHHH	X X h I h	X X A h	HLHIGHHG	L H A H L A

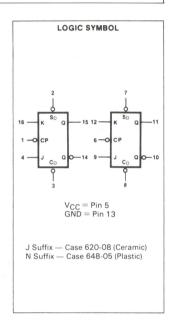
*Both outputs will be HIGH while both \overline{S}_D and \overline{C}_D are LOW, but the output states are unpredictable if \overline{S}_D and \overline{C}_D go HIGH simultaneously.

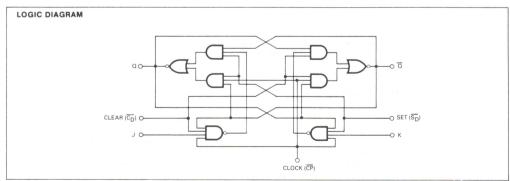
H,h = HIGH Voltage Level

L,I = LOW Voltage Level

X = Immaterial

I,h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.





GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	· V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54, 74			-0.4	mA
lOL	Output Current — Low	54 74		~	4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

				LIMITS			1	
SYMBOL	PARAMETER	2	MIN	TYP	MAX	UNITS	TEST C	ONDITIONS
VIH	Input HIGH Voltage		2.0	111	IVIAX	V	Guaranteed Inp All Inputs	ut HIGH Voltage for
		54			0.7		Guaranteed Input LOW Voltage All Inputs	
VIL	Input LOW Voltage	74			0.8	V		
VIK	Input Clamp Diode Volta	ge		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$	
Voн	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{OH}$ or V_{IL} per Truth Table	
VOH	Output man voltage	74	2.7	3.5		V		
		54,74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} =	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA V _{IN} = V _{IL} or V _I per Truth Table	
liн	Input HIGH Current	J, K Clear Clock			20 60 80	μΑ	V _{CC} = MAX, V _{IN} = 2.7 V	
чн	input man editent	J, K Clear Clock			0.1 0.3 0.4	mA	V _{CC} = MAX, V _I	N = 7.0 V
IIL	Input LOW Current	J, K Clear, Clock			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
lcc	Power Supply Current				6.0	mA	V _{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

CVMAROL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
SYMBOL		MIN	TYP	MAX	ONITS	TEST CONDITIONS	
fMAX	Maximum Clock Frequency	30	45		MHz		
tPLH	Clock, Clear, Set to Output		15	20	ns	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 15 \text{ pF}$	
^t PHL			15	20	ns		

AC SETUP REQUIREMENTS: $T_{\mbox{\scriptsize A}} = 25 \ensuremath{^{\circ}}\mbox{\scriptsize C}$, $V_{\mbox{\scriptsize CC}} = 5.0 \ \mbox{\scriptsize V}$

SYMBOL	PARAMETER		LIMITS			TEST CONDITIONS	
STIVIBUL		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
tw	Clock Pulse Width High	20			ns		
tw	Clear Set Pulse Width	25			ns	$V_{CC} = 5.0 \text{ V}$	
t _S	Setup Time	20			ns	100 515 1	
th	Hold Time	0			ns		



DESCRIPTION — The SN54LS/74LS78A offers individual J, K, and Direct Set inputs as well as common Clock Pulse and Common Direct Clear Inputs. These dual Fiip-Flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the HIGH-to-LOW Clock Transition.

J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

SN54LS78A SN74LS78A

DUAL JK FLIP-FLOP

LOW POWER SCHOTTKY

MODE SELECT - TRUTH TABLE

S _D L H L	TC _D	J X	K X X	OUT Q H L	PUTS
L		×	×		L
L H L	H	×	×	H	L H
H L	L			L	Н
L	1				
	_	X	×	Н	н
Н	н	h	h	q	q
Н	Н	1	h	L	Н
Н	Н	h	- 1	н	L
Н	н	1	1	q	q
	Н	н	H H h	H H h I	H H h I H

*Both outputs will be HIGH while both \overline{S}_D and \overline{C}_D are LOW, but the output states are unpredictable if \overline{S}_D and \overline{C}_D go HIGH simultaneously.

H, h = HIGH Voltage Level L, I = LOW Voltage Level

X = Immaterial

I, h(q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-

LOW clock transition.

LOGIC SYMBOL 3 J SD Q 13 10 J SD Q 8 14 K CD CP CP CD CP VCC = Pin 4 GND = Pin 11

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		LINUTC	TEST CONDITIONS		
STIVIBUL	PARAMETER		MIN	TYP	MAX	UNITS	TEST	CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
14		54			0.7	V		ut LOW Voltage for	
V _{IL}	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA		
Voн	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{OH}$ or V_{IL} per Truth Table		
•ОП	output morr voltage	74	2.7	3.5		V			
		54,74		0.25	0.4	V	$ \begin{array}{c c} I_{OL} = 4.0 \text{ mA} \\ \hline I_{OL} = 8.0 \text{ mA} \\ \end{array} \begin{array}{c} V_{CC} = V_{CC} \text{ MI} \\ V_{IN} = V_{IL} \text{ or } V_{IC} \\ \text{per Truth Table} \\ \end{array} $		
VOL	Output LOW Voltage	74		0.35	0.5	V			
	Input HIGH Current J, K Clear Set Clock				20 120 60 160	μΑ	$V_{CC} = MAX, V_{IN} = 2.7 \text{ V}$ $V_{CC} = MAX, V_{IN} = 7.0 \text{ V}$		
liн	J, K Clear Set Clock				0.1 0.6 0.3 0.8	mA			
lIL	Input LOW Current J, K Set Clock, Clear				-0.4 -0.8 -1.6	mA	$V_{CC} = MAX, V_{IN} = 0.4 V$		
los	Output Short Circuit Cu	ırrent	-20		-100	mA	V _{CC} = MAX, V _C	OUT = 0 V	
СС	Power Supply Current			4.0	6.0	mA	$V_{CC} = MAX, V_{CC}$	CP = 0 V	

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
STIVIBUL		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
fMAX	Maximum Clock Frequency	30	45		MHz	V	
tPLH	Clear, Clock, Set to Output		15	20	ns	$V_{CC} = 5.0 \text{ V}$ $C_{I} = 15 \text{ pF}$	
^t PHL			15	20	ns		

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	0.00.045750		LIMITS		UNITS	TEST CONDITIONS		
	PARAMETER	MIN	TYP	MAX	UNITS			
tw	Clock Pulse Width High	20			ns			
tw	Clear Set Pulse Width	25			ns	V _{CC} = 5.0 V		
t _S	Setup Time	20			ns	VCC = 3.5 V		
th	Hold Time	0			ns			



DESCRIPTION — The SN54LS/74LS83A is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A₁ — A₄, B₁ — B₄)and a Carry Input (C₀).It generates the binary Sum outputs Σ_1 — Σ_4) and the Carry Output (C₄) from the most significant bit. The LS83A operates with either active HIGH or active LOW operands (positive or negative logic). The SN54LS/74LS283 is recommended for new designs since it is identical in function with this device and features standard corner power pins.

PIN NAMES

		HIGH	LOW
A ₁ — A ₄ B ₁ — B ₄	Operand A Inputs Operand B Inputs	1.0 U.L.	0.5 U.L.
C ₀	Carry Input	1.0 U.L. 0.5 U.L.	0.5 U.L. 0.25 U.L.
Σ 1 $ \Sigma$ 4	Sum Outputs (Note b)	10 U.L.	5(2.5) U.L.
C4	Carry Output (Note b)	10 U.L.	5(2.5) U.L.

LOADING (Note a)

NOTES:

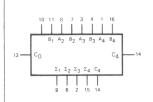
- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for commercial (74) Temperature Ranges.

SN54LS83A SN74LS83A

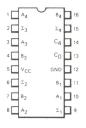
4-BIT BINARY FULL ADDER WITH FAST CARRY

LOW POWER SCHOTTKY





CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

NOTE:

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS83A adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C₄) outputs.

$$C_0 + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_4$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS83A can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH Inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Example:

	CO	Α1	A ₂	Аз	A4	В1	B ₂	В3	В4	Σ1	Σ_2	Σ3	Σ4	C4	
Logic Levels	L	L	Н	L	Н	Н	L	L	Н	Н	Н	L	L	Н	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9 = 19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6 = 12)

Interchanging inputs of equal weight does not affect the operation, thus C₀, A₁, B₁, can be arbitrarily assigned to pins 10, 11, 13, etc.

FUNCTIONAL TRUTH TABLE

C(n-1)	An	Bn	Σ_{n}	Cn
L	L	L	L	L
L	L	Н	Н	L
L	Н	L	Н	L
L	Н	Н	L	Н
Н	L	L	Н	L
Н	L	Н	L	Н
Н	Н	L	L	Н
Н	Н	Н	Н	Н

 ${\it C}_1-{\it C}_3$ are generated internally ${\it C}_0-{\it is}$ an external input

C₄ — is an output generated internally

GUARANTEED OPERATING RANGES

COMIDAITIE	D OI EIGHING IDAIGEO					
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ЮН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DADAMETER	PARAMETER		LIMITS			TEST CONDITIONS		
STIVIBUL	PARAIVIETER		MIN	TYP	MAX	UNITS	TEST	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage All Inputs		
V	Input LOW Voltage	54			0.7	V		ut LOW Voltage for	
VIL	input LOVV Voitage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN}$	=-18 mA	
VoH	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} =		
TOR	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	$V_{IN} = V_{IL}$ or V_{IH} per Truth Table	
IIH	Input HIGH Current C _O A or B				20 40	μΑ	V _{CC} = MAX, V _{IN} = 2.7 V		
111	C _O A or B				0.1 0.2	mA	V _{CC} = MAX, V _I	N = 7.0 V	
I _{IL}	Input LOW Current C _O A or B				-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V		
los	Output Short Circuit Cu	rrent	-20		-100	mA	$V_{CC} = MAX$		
lcc	Power Supply Current All Inputs Grounded All Inputs at 4.5 V, Ex All Inputs at 4.5 V	cept B			39 34 34	mA	V _{CC} = MAX		

AC CHARACTERISTICS: $T_A = 25$ °C

CVMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS		
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
^t PLH ^t PHL	Propagation Delay, C_0 Input to any Σ Output		16 15	24 24	ns			
^t PLH ^t PHL	Propagation Delay, Any A or B Input to Σ Outputs		15 15	24 24	ns	$V_{CC} = 5.0 V$ $C_{L} = 15 pF$		
^t PLH ^t PHL	Propagation Delay, Co Input to C4 Output		11 15	17 22	ns	Figures 1 and 2		
^t PLH ^t PHL	Propagation Delay, Any A or B Input to C ₄ Output		11 12	17 17	ns			

AC WAVEFORMS

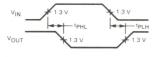


Fig. 1

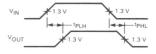


Fig. 2



DESCRIPTION — The SN54LS/74LS85 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A₀-A₃, B₀-B₃); A₃, B₃ being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" (O_A > B), "A less than B" (O_A < B), "A equal to B" (O_A = B). Three Expander Inputs, I_A > B, I_A < B, I_A = B, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: I_A < B = I_A > B = L, I_A = B = H. For serial (ripple) expansion, the O_A > B, O_A < B and O_A = B Outputs are connected respectively to the I_A > B, I_A < B, and I_A = B inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the SN54LS/74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

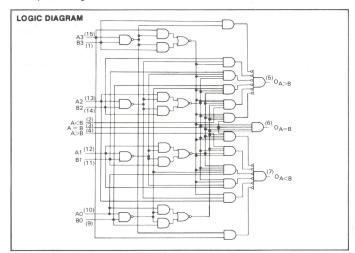
• EASILY EXPANDABLE

BINARY OR BCD COMPARISON
 OA > B. OA > B. AND OA - B. OUTPUTS AVAILABI

• O _{A >B} , O _{A<b< sub=""></b<>}	$_{A}$, AND $O_{A} = B$ OUTPUTS AVAILABLE	LOADIN	G (Note a)
PIN NAMES		HIGH	LOW
A_0-A_3 , B_0-B_3	Parallel Inputs	1.5 U.L.	0.75 U.L.
$I_A = B$	A = B Expander Inputs	1.5 U.L.	0.75 U.L.
$I_{A < B}, I_{A > B}$	A < B, $A > B$, Expander Inputs	0.5 U.L.	0.25 U.L.
$O_{A > B}$	A Greater Than B Output (Note b)	10 U.L.	5 (2.5) U.L.
O _A < _B	B Greater Than A Output (Note b)	10 U.L.	5 (2.5) U.L.
$O_A = B$	A Equal to B Output (Note b)	10 U.L.	5 (2.5) U.L.

Notes: a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW

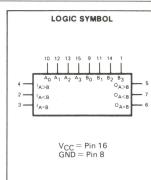
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

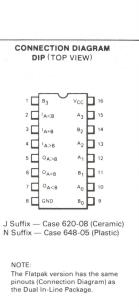


SN54LS85 SN74LS85

4-BIT MAGNITUDE COMPARATOR

LOW POWER SCHOTTKY





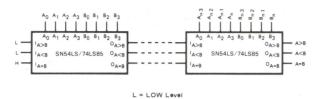
TRUTH TABLE

co	COMPARING INPUTS				ASCADIN	IG	OUTPUTS			
A3,B3	A ₂ ,B ₂	A ₁ ,B ₁	A ₀ ,B ₀	I _{A>B}	I _{A<b< sub=""></b<>}	I _{A=B}	O _{A>B}	o _{A<b< sub=""></b<>}	O _{A=B}	
A ₃ >B ₃	Х	Х	X	X	Х	Х	Н	L	L	
A3 <b3< td=""><td>X</td><td>X</td><td>×</td><td>X</td><td>×</td><td>X</td><td>L</td><td>Н</td><td>L</td></b3<>	X	X	×	X	×	X	L	Н	L	
A3=B3	A ₂ >B ₂	×	×	X	×	X	н	L	L	
A3=B3	$A_2{<}B_2$	×	×	X	×	Х	L	н	L	
A3=B3	A2=B2	$A_1 > B_1$	×	X	×	Х	н	L	L	
A3=B3	A2=B2	$A_1 < B_1$	×	X	×	X	L	Н	L	
A3=B3	A2=B2	A1=B1	$A_0 > B_0$	×	×	Х	н	L	L	
A3=B3	A2=B2	A1=B1	$A_0{<}B_0$	X	×	X	L	Н	L	
A3=B3	A2=B2	A1=B1	$A_0 = B_0$	н	L	L	н	L	L	
A3=B3	A2=B2	A1=B1	A ₀ =B ₀	L	н	L	L	Н	L	
A3=B3	A2=B2	A ₁ =B ₁	$A_0 = B_0$	X	X	Н	L	L	Н	
A3=B3	A2=B2	A1=B1	A ₀ =B ₀	н	Н	L	L	L	L	
A3=B3	A2=B2	A ₁ =B ₁	A ₀ =B ₀	L	L	L	н	Н	L	

H = HIGH Level L = LOW Level X = IMMATERIAL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN ·	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	٧
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA



H = HIGH Level
Fig. 1. COMPARING TWO n-BIT WORDS

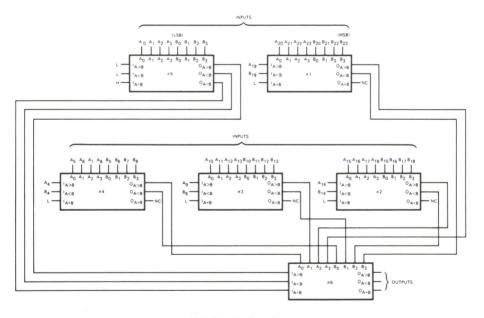
APPLICATIONS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table 1,

TABLE I

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2 - 6
25-120 Bits	8 - 31

NOTE:
The SN54LS/74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A_O-A_O and B_O-B_O inputs of another SN54LS/74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.



MSB = Most Significant Bit LSB = Least Significant Bit

L = LOW Level H = HIGH Level

NC = No Connection

Fig. 2. COMPARISON OF TWO 24-BIT WORDS

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	PARAMETE	'D		LIMITS		UNITS	TEST CONDITIONS		
SYMBOL	PARAMETE	R	MIN	TYP	MAX	UNITS	IEST	CONDITIONS	
VIH	Input HIGH Voltage	C 60 110	2.0			٧	Guaranteed Input HIGH Voltage fo All Inputs		
	181 121	54			0.7		Guaranteed Inp	out LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	ı = −18 mA	
VoH	Output HIGH Voltage	54	2.5	3.5	100	V		$H = MAX, V_{IN} = V_{IH}$	
VОН	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Truth	n Table	
VOL	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table	
VOL	Output Lovy Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$		
lн	Input HIGH Current A < B, A > B Other Inputs A < B, A > B Other Inputs				20 60	μΑ	$V_{CC} = MAX, V_{IN} = 2.7 V$		
					0.1 0.3	mA	V _{CC} = MAX, V	1 _{IN} = 7.0 V	
	Input LOW Current								
IL A < B, A > B Other Inputs		,			-0.4 -1.2	mA	V _{CC} = MAX, V	$I_{1N} = 0.4 \text{ V}$	
los	Output Short Circuit: Current		-20		-100	mA	V _{CC} = MAX		
Icc	Power Supply Current				20	mA	V _{CC} = MAX		

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

CVMAROL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS		
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS			
^t PLH ^t PHL	Any A or B to A $<$ B, A $>$ B		24 20	36 30	ns			
^t PLH ^t PHL	Any A or B to A = B		27	45 45	ns	V _{CC} = 5.0 V		
^t PLH ^t PHL	A < B or A = B to A > B		14 11	22 17	ns	$C_L = 15 \text{ pF}$		
tPLH tPHL	A = B to A = B		13 13	20 26	ns			
tPLH tPHL	A > B or $A = B$ to $A < B$		14 11	22 17	ns			

AC WAVEFORMS

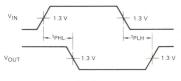
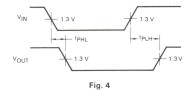
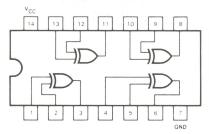


Fig. 3



MOTOROLA SCHOTTKY TTL DEVICES





TRUTH TABLE

	N	OUT
1		
A	В	Z
L	L	L
L	Н	н
• н	L	н
Н	Н	L

SN54LS86 SN74LS86

QUAD 2-INPUT EXCLUSIVE OR GATE LOW POWER SCHOTTKY

J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

GUARANTEED OPERATING RANGES

	0. 1.0					
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ЮН	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS		
STIVIBUL	FARAIVIETER		MIN	TYP	MAX	UNITS	IESI	CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
	54			0.7			put LOW Voltage for		
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Voltag	е		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
		54	2.5	3.5		V		$_{OH} = MAX, V_{IN} = V_{IH}$	
VOH	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	h Table	
.,		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA V _{IN} = V _{IL} or V _{IH} per Truth Table		
					40	μΑ	V _{CC} = MAX, \	/ _{IN} = 2.7 V	
lН	Input HIGH Current				0.2	mA	V _{CC} = MAX, \	/ _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V		
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
ICC	Power Supply Current				10	mA	V _{CC} = MAX	21	

AC CHARACTERISTICS: $T_A = 25$ °C

CVMBOL	DADAMETED	LIMITS			UNITS	TEST CONDITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t _{PLH}	Propagation Delay, Other Input LOW		12 10	23 17	ns	V _{CC} = 5.0 V	
^t PLH ^t PHL	Propagation Delay, Other Input HIGH		20 13	30 22	ns	C _L = 15 pF	



DESCRIPTION — The SN54LS/74LS90, SN54LS/74LS92 and SN54LS/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggerd by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to \overline{CP}) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

- LOW POWER CONSUMPTION . . . TYPICALLY 45 mW
- HIGH COUNT RATES . . . TYPICALLY 42 MHz
- CHOICE OF COUNTING MODES . . . BCD, BI-QUINARY, DIVIDE-BY-TWELVE, BINARY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION **EFFECTS**

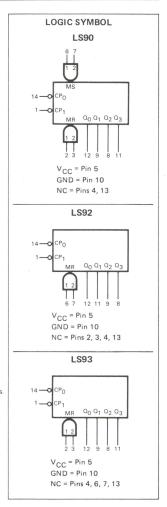
PIN NAMES LOADING (Note a) HIGH LOW 0.5 U.L. CPn Clock (Active LOW going edge) Input to 1.5 U.L. ÷2 Section CP₁ 2.0 U.L. Clock (Active LOW going edge) Input to 0.5 U.I. ÷5 Section (LS90), ÷6 Section (LS92) CP₁ Clock (Active LOW going edge) Input to 0.5 U.L. 1.0 U.L. ÷8 Section (LS93) MR_1, MR_2 Master Reset (Clear) Inputs 0.5 U.L. 0.25 U.L. 0.25 U.L. MS₁, MS₂ Master Set (Preset-9, LS90) Inputs 0.5 U.L. Output from ÷2 Section (Notes b & c) 10 U.L. 5(2.5) U.L. Q_1, Q_2, Q_3 Outputs from ÷5 (LS90), ÷6 (LS92), 10 U.L. 5(2.5) U.L. ÷8 (LS93) Sections (Note b)

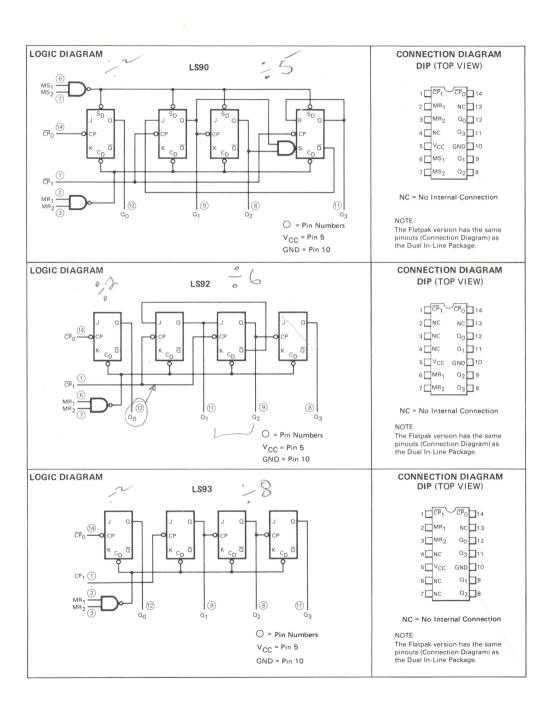
- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges c. The Ω_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{\text{CP}}_1$ input of the device.
- d. To insure proper operation the rise (tr) and fall time (tf) of the clock must be less than 100 ns.

SN54LS/74LS90 SN54LS/74LS92 SN54LS/74LS93

DECADE COUNTER: **DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER**

LOW POWER SCHOTTKY





FUNCTIONAL DESCRIPTION — The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q₀ output of each device is designed and specified to drive the rated fan-out plus the $\overline{\mathbb{CP}}_1$ input of the device.

A gated AND asynchronous Master Reset (MR₁ \bullet MR₂) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set (MS₁ \bullet MS₂) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

LS90

- A. BCD Decade (8421) Counter The $\overline{\text{CP}}_1$ input must be externally connected to the Q_O output. The $\overline{\text{CP}}_0$ input receives the incoming count and a BCD count sequence is produced.
- B. Symmetrical Bi-quinary Divide-By-Ten Counter The Q₃ output must be externally connected to the $\overline{\text{CP}}_0$ input. The input count is then applied to the $\overline{\text{CP}}_1$ input and a divide-by-ten square wave is obtained at output Q₀.
- C. Divide-By-Two and Divide-By-Five Counter No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (\overline{CP}_0 as the input and Q_0 as the output). The \overline{CP}_1 input is used to obtain binary divide-by-five operation at the Q_3 output.

LS92

- A. Modulo 12, Divide-By-Twelve Counter The $\overline{\text{CP}}_1$ input must be externally connected to the Q₀ output. The $\overline{\text{CP}}_0$ input receives the incoming count and Q₃ produces a symmetrical divide-by-twelve square wave output.
- B. Divide-By-Two and Divide-By-Six Counter No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{\text{CP}}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

LS93

- A. 4-Bit Ripple Counter The output Q_0 must be externally connected to input $\overline{\mathbb{CP}}_1$. The input count pulses are applied to input $\overline{\mathbb{CP}}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0 , Q_1 , Q_2 , and Q_3 outputs as shown in the truth table.
- B. 3-Bit Ripple Counter The input count pulses are applied to input $\overline{\mathbb{CP}}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1 , Q_2 , and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS90 MODE SELECTION

SN54LS/74LS90 • SN54LS/74LS92 • SN54LS/74LS93

RE			OUT	PUTS						
MR ₁	MR ₂	MS ₁	MS ₂		α ₀	Q ₁	02	α3		
Н	Н	L	X	11	L	L	L	L		
Н	. н	X	L		L	L	L	L		
X	X	Н	Н		Н	L	L	Н		
L	X	L	X			Co	unt			
X	L	X	L		Count					
L	X	X	L		Count					
X	L	L	X			Co	unt			

H = HIGH Voltage Level
L = LOW Voltage Level

X = Don't Care

LS92	AND	LS93
MODE	SELE	CTION

RESET INPUTS			OUTI	PUTS			
MR ₁	MR ₂	ο ₀	Q ₁	Q_2	Ω3		
Н	Н	L	L	L	L		
L	Н		Cou	int			
Н	L	Count					
L	L		Cou	int			

H = HIGH Voltage Level
L = LOW Voltage Level

X = Don't Care

LS90 BCD COUNT SEQUENCE

COLINIT	1	OUT	PUT				
COUNT	. Q ₀	Q ₁	02	Ο3			
0	L	L	Ŀ	L			
1	Н	L	L	L			
2	L	Н	L	L			
3	H	Н	L	L			
4	L	L	Н	L			
5	- H	L	Н	L			
6	L	Н	Н	L			
7	Н	Н	Н	L			
8	L	L	L	ч Н ч			
9	Н	L	L	Н			

NOTE: Output Q_0 is connected to Input \overline{CP}_1 for BCD count.

LS92 TRUTH TABLE

COUNT		OUT	PUT						
COONT	α ₀	α ₁	02	α3					
0	L	L	L	L					
. 1	Н	L	L	L					
2 3	L	Н	L	L					
3	Н	Н	L	L					
4	L	L	Н	L					
5	Н	L	H	L					
6	L	L	L	Н					
7	Н	L	L	Н					
8	L	Н	L	Н					
9	Н	Н	L)	Н					
10	L	L	Н	H					
11	Н	L	н	Н					

Note: Output Q₀ connected to input $\overline{\text{CP}}_1$

LS93 TRUTH TABLE

COUNT		OUT	PUT	
COONT	α ₀	01	Q_2	σ_3
0	L	L	L	L
1	H	L	L	L
2	L	Н	L	L
3	Н	Н	L	L
4	L	L	Н	L
5	Н	L	Н	L
6	L	Н	Н	L
7	Н	Н	Н	L
8	L	L	L	Н
9	Н	L	L	Н
10	L	H	L	Н
11	Н	Н	L	Н
12	L	L	Н	Н
13	H	L	Н	Н
14	L	Н	Н	Н
15	Н	Н	Н	Н

Note: Output Q_0 connected to input \overline{CP}_1 .

GUARANTEED OPERATING RANGES

						*
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lor	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS		
STIVIBUL	FARAIVIETER	`	MIN	TYP	MAX	UNITS	TEST	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
		54			0.7	.,		at LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
√IK	Input Clamp Diode Volt	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
Voн	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{OH}$		
*OH	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth	h Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	VCC = VCC MIN,	
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA	VIN = VIL or VIH per Truth Table	
					20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$		
IH	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_{IN} = 7.0 \text{ V}$		
liL	Input LOW Current MS, MR CP ₀ CP ₁ (LS90, LS92) CP ₁ (LS93)				-0.4 -2.4 -3.2 -1.6	mA	V _{CC} = MAX, V _{IN} = 0.4 V		
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current				15	mA	V _{CC} = MAX	-	

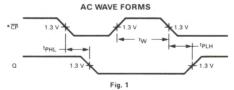
AC CHARACTERISTICS: $T_A = 25^{\circ}C$, $V_{CC} = 5.0 \text{ V}$, $C_L = 15 \text{ pF}$

	PARAMETER	LIMITS									
SYMBOL		LS90			LS92			LS93			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
fMAX	CPO Input Clock Frequency	32			32			32		,	MHz
fMAX	CP₁ Input Clock Frequency	16			16			16			MHz
tPLH tPHL	Propagation Delay, CP _O Input to Q _O Output		10 12	16 18		10 12	16 18		10 12	16 18	ns
^t PLH ^t PHL	CP ₀ Input to Q₃ Output		32 34	48 50		32 34	48 50		46 46	70 70	ns
tPLH tPHL	\overline{CP}_1 Input to Q ₁ Output		10 14	16 21		10 14	16 21		10 14	16 21	ns
tPLH tPHL	$\overline{\text{CP}}_1$ Input to Q₂ Output		21 23	32 35	,	10 14	16 21		21 23	32 35	ns
^t PLH ^t PHL	CP₁ Input to Q₃ Output		21 23	32 35		21 23	32 35		34 34	51 51	ns
^t PLH	MS Input to Q ₀ and Q ₃ Outputs		20	30							ns
^t PHL	MS Input to Q ₁ and Q ₂ Outputs		26	40							ns
^t PHL	MR Input to Any Output		26	40		26	40		26	40	ns

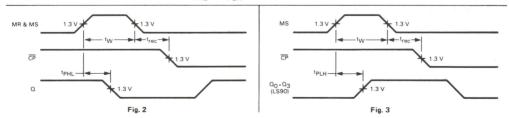
AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

			LIMITS						
SYMBOL	PARAMETER	LS	LS90		LS92		93	UNITS	
		MIN	MAX	MIN	MAX	MIN	MAX		
tw	CP _O Pulse Width	15		15		15		ns	
tw	CP₁ Pulse Width	30		30		30		ns	
tw	MS Pulse Width	15						ns	
tw	MR Pulse Width	15		15		15		ns	
t _{rec}	Recovery Time MR to CP	25		25		25		ns	

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.



*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.





DESCRIPTION — The SN54LS/74LS91 is an 8-Bit Serial-In/Serial Out Shift Register. This device features eight R-S master-slave flip-flops, input gating and a clock driver. By gating single-rail data and input control thru inputs A, B, and an internal inverter, complementary inputs to the first bit of the shift register are formed. An inverting clock driver provides the drive for the internal common clock line. The clock pulse inverter driver causes this circuitry to shift information one-bit on the positive edge of the input clock pulse.

FUNCTION TABLE

	UTS	OUTPUTS				
AI	tn	AT t _{n+8}				
Α	В	QH	ΦH			
Н	Н	Н	L			
L	X *	L	H			
X	L	L	Н			

H = HIGH, L = LOW

X = Irrelevant

 $t_{n} = Reference bit time$

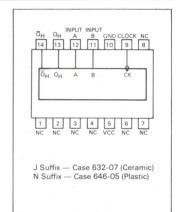
t_{n+8} = Bit time after 8 LOW to High Clock

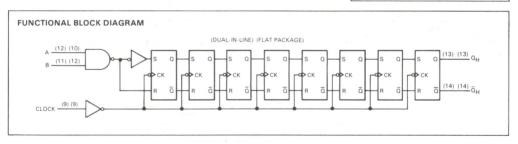
transition

SN54LS91 SN74LS91

8-BIT SHIFT REGISTERS

LOW POWER SCHOTTKY





GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
Vcc	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
IOL	Output Current — Low	54 74	-7-		4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS		
STIVIBUL	PARAIVIETER	1	MIN	TYP	MAX	UNITS	TEST	CNDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	out HIGH Voltage for	
		54			0.7	.,	Guaranteed Inp	out LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = −18 mA		
VOH	Output HIGH Voltage 54 74		2.5	3.5		V	$V_{CC} = MIN$, $I_{OH} = MAX$, $V_{IN} = V_{II}$		
			2.7	3.5		V	or V _{IL} per Truth Table		
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
			1,		20	μΑ	$V_{CC} = MAX, V_I$	IN = 2.7 V	
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
ll I	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	V _{CC} = MAX, V _{IN} = 0.4 V	
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current				20	mA	V _{CC} = MAX		

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	DADAMETED	LIMITS			LINUTO	TEGT COMPLETIONS	
	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
fMAX	Maximum Clock Frequency	10	18		MHz		
t _{PLH} t _{PHL}	Propagation Delay LOW to HIGH Propagation Delay HIGH to LOW		24 27	40 40	ns	$V_{CC} = 5.0 V$ $C_L = 15 pF$	

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER	LIMITS			UNITS	, TEST COMPLICATE		
	PARAMETER	MIN	TYP	MAX	UNITS	* TEST CONDITIONS		
t₩	Clock Pulse Width Low	25			ns	2 - 2 - 2		
t _S	Setup Time	25			ns	V _{CC} = 5.0 V		
th	Hold Time	0			ns			



DESCRIPTION — The SN54LS/74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The LS95B is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- SYNCHRONOUS, EXPANDABLE SHIFT RIGHT
- SYNCHRONOUS SHIFT LEFT CAPABILITY
- SYNCHRONOUS PARALLEL LOAD
- SEPARATE SHIFT AND LOAD CLOCK INPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

PIN NAMES

LOADING (Note a)

		HIGH	LOW
S	Mode Control Input	0.5 U.L.	0.25 U.L.
DS	Serial Data Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
P ₀ — P ₃ CP ₁	Serial Clock (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
CP ₂	Parallel Clock (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
$0^{0} - 0^{3}$	Parallel Outputs (Note b)	10 U.L.	5(2.5)U.L.

NOTES:

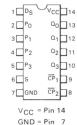
- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54LS95B SN74LS95B

4-BIT SHIFT REGISTER

LOW POWER SCHOTTKY

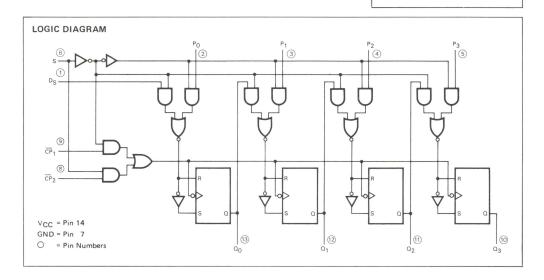
CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

NOTE

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



FUNCTIONAL DESCRIPTION — The LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P₀ — P₃) Data inputs and four Parallel Data outputs (Q₀ — Q₃). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock Inputs ($\overline{\mathbb{CP}}_1$) and ($\overline{\mathbb{CP}}_2$). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, $\overline{\text{CP}}_2$ is enabled. A HIGH to LOW transition on enabled $\overline{\text{CP}}_2$ transfers parallel data from the P $_0$ — P $_3$ inputs to the Q $_0$ — Q $_3$ outputs.

When the Mode Control input (S) is LOW, \overline{CP}_1 is enabled. A HIGH to LOW transition on enabled \overline{CP}_1 transfers the data from Serial input (DS) to Q₀ and shifts the data in Q₀ to Q₁, Q₁ to Q₂, and Q₂ to Q₃ respectively (right-shift). A left-shift is accomplished by externally connecting Q₃ to P₂, Q₂ to P₁, and Q₁ to P₀, and operating the LS95B in the parallel mode (S = HIGH).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while $\overline{\text{CP}}_2$ is HIGH, or changing S from HIGH to LOW while $\overline{\text{CP}}_1$ is HIGH and $\overline{\text{CP}}_2$ is LOW will not cause any changes on the register outputs.

MODE SELECT - TRUTH TABLE

OPERATING MODE			INPUTS				OUTPL	TS	
OPENATING MODE	S	CP ₁	CP ₂	DS	Pn	α ₀	Q ₁	02	ο3
Ch://	L	L	×	1.	x	L	q ₀	q ₁	q ₂
Shift	L	1	×	h	X	н	90	91	92
Parallel Load	Н	Х	1	Х	Pn	P ₀	P ₁	p ₂	p ₃
	L	L	L	Х	X	No Change			
	7	L	L	Х	X	No Change			
	l	Н	L	X	Х		No C	hange	
Mode Change	7	Н	L	Х	Х		Undete	rmined	
Wode Change	l	L	н	X	X		Undete	rmined	
	7	L	Н	×	Х		No C	hange	
	L	н	Н	Х	X	Undetermined			
	1	Н	Н	X	X		No C	nange	

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

I = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.

h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

 p_{Π} = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
Vcc	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

CVAADOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS		
SYMBOL	PARAMETER	(MIN	TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
		54			0.7			ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA		
Vон	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN$, $I_{OH} = MAX$, $V_{IN} = V_{I}$		
	Output more voltage	74	2.7	3.5	8	V	or V _{IL} per Truth Table		
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
IH	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
IL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	$V_{CC} = MAX$, $V_{IN} = 0.4 V$	
os	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current				21	mA	V _{CC} = MAX	* *	

AC CHARACTERISTICS: TA = 25°C, VCC = 5.0 V

SYMBOL	PARAMETER	LIMITS			UNITS	TEST COMPITIONS	
STIVIBUL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
fMAX	Maximum Clock Frequency	25	36		MHz	V _{CC} = 5.0 V	
^t PLH	CP to Output		18	27	ns	$C_{\rm L} = 15 \rm pF$	
^t PHL			21	32	ns		

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

0)/440.01			LIMITS			TEST CONDITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS		
tw	CP Pulse Width	20			ns		
t _S	Data Setup Time	20			ns		
th	Data Hold Time	20			ns	V _{CC} = 5.0 V	
t _S	Mode Control Setup Time	20			ns		
th	Mode Control Hold Time	20			ns		

DESCRIPTIONS OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) —is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

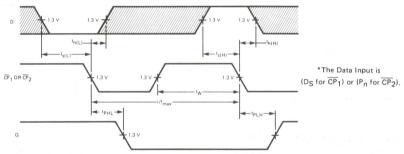
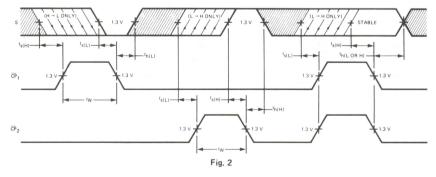


Fig. 1





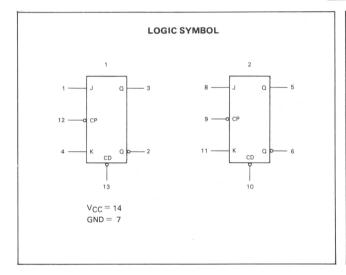
SN54LS107A SN74LS107A

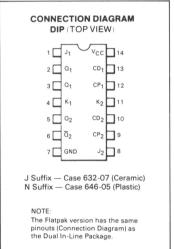
DESCRIPTION — The SN54LS/74LS107A is a Dual JK Flip-Flop with individual J, K, Direct Clear and Clock Pulse inputs. Output changes are initiated by the HIGH-to-LOW transition of the clock. A LOW signal on CD input overrides the other inputs and makes the Q output LOW.

The SN54LS/74LS107A is the same as the SN54LS/74LS73A but has corner power pins.

DUAL JK FLIP-FLOP

LOW POWER SCHOTTKY





GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DADA	PARAMETER			LIMITS		UNITS	TEST CONDITIONS	
STIVIBUL	PARA	IVIETER		MIN	TYP	MAX	UNITS	TEST	CONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	out HIGH Voltage for	
.,			54			0.7	.,	Guaranteed Inp	out LOW Voltage for
VIL	Input LOW Voltage		74			0.8	V	All Inputs	
VIK	Input Clamp Diode	Voltage			-0.65	-1.5	. V	V _{CC} = MIN, I _{IN}	j = −18 mA
Voh	Output HIGH Voltage	10	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$
VОН	Output man voitag	ic.	74	2.7	3.5		V	or V _{IL} per Truth	Table .
			54,74		0.25	0.4	V		V _{CC} = V _{CC} MIN,
VOL	Output LOW Voltag	е	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	$V_{IN} = V_{IL}$ or V_{IH} per Truth Table
I	Input HIGH Current	J, K Clear Clock				20 60 80	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 \text{ V}$ $V_{CC} = MAX$, $V_{IN} = 7.0 \text{ V}$	
lін		J, K Clear Clock				0.1 0.3 0.4	mA		
IIL	Input LOW Current	J, K Clear a	nd Clock			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
los	Short Circuit Currer	nt		-20		-100	mA	V _{CC} = MAX	
lcc	Power Supply Curre	ent			-	6.0	mA	$V_{CC} = MAX$	

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

	7					
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
fMAX	Maximum Clock Frequency	30	45		MHz	$V_{CC} = 5.0 \text{ V}$
^t PLH	Propagation Delay,		15	20	ns	$C_{\rm I} = 15 \rm pF$
^t PHL	Clock to Output		15	20	ns	S_ 10 pi

AC SETUP REQUIREMENTS: $T_A = 25^{\circ}C$, $V_{CC} = 5.0 \text{ V}$

CVAADOL	PARAMETER	LIMITS			UNITS	TEST COMPITIONS	
SYMBOL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
tw	Clock Pulse Width	20			ns		
tw	Set Pulse Width	25			ns	V _{CC} = 5.0 V	
t _S	Setup Time	20			ns]	
th	Hold Time	0			ns		



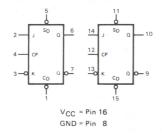
DESCRIPTION — The SN54LS/74LS109A consists of two high speed completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and \overline{K} pins together.

SN54LS109A SN74LS109A

DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY





J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

LOGIC DIAGRAM SET(Sp) 5(11) CLEAR (CD) 1(16) CLOCK 4(12) Z(14) R 3(13)

CVAADOL	DADAMETER			LIMITS		LINUTC	TECT	CNDITIONS	
SYMBOL	PARAMETER	1	MIN	TYP	MAX	UNITS	TEST	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp	ut HIGH Voltage for	
		54			0.7			ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA	
Voн	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$	
VOH.	Output mon voltage	74	2.7	3.5		V	or V _{IL} per Truth Table		
.,		54,74		0.25	0.4	V	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN$, $V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$		
	Input HIGH Current J, K, Clock Set, Clear				20 40	μΑ	V _{CC} = MAX, V _{IN} = 2.7 V		
Ін	J, K, Clock Set, Clear				0.1 0.2	mA	VCC = MAX, V	N = 7.0 V	
lıL	Input LOW Current J, K, Clock Set, Clear				-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V		
los	Output Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
СС	Power Supply Current			8.0	mA	V _{CC} = MAX			

MODE SELECT - TRUTH TABLE

00504711041005	1	NPUTS		OUTPUTS		
OPERATING MODE	s _D	\overline{c}_{D}	J	ĸ	Q	ā
Set	L	н	×	X	н.	L
Reset (Clear)	н	L	×	X	L	н
*Undetermined	L	L	×	×	н	н
Load "1" (Set)	н	н	h	h	н	L
Hold	н	н	1	h	q	q
Toggle	н	н	h	- 1	q	q
Load "0" (Reset)	н	н	1	- 1	L	Н

*Both outputs will be HIGH while both $\overline{S}_{\overline{D}}$ and $\overline{C}_{\overline{D}}$ are LOW, but the output states are unpredictable if $\overline{S}_{\overline{D}}$ and $\overline{C}_{\overline{D}}$ go HIGH simultaneously.

H,h = HIGH Voltage Level

L,I = LOW Voltage Level X = Don't Care

I, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
IOL	Output Current — Low	54 74	,		4.0 8.0	mA

AC CHARACTERISTICS: TA = 25°C, VCC = 5.0 V

CVMPOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS			
SYMBOL	FARAIVIETER	MIN	TYP	MAX	ONTO	TEST CONDITIONS			
fMAX	Maximum Clock Frequency	25	33		MHz	V _{CC} = 5.0 V			
tPLH	Clock, Clear, Set to Output		13	25	ns	$C_L = 15 \text{ pF}$			
tPHL .			25	40	ns				

AC SET UP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	DADAMETER	LIMITS			UNITS	TEST CONDITIONS
	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
tw	Clock High Clear, Set Pulse Width	25			ns	
ts	Data Setup Time — HIGH	35			ns	$V_{CC} = 5.0 \text{ V}$
o .	LOW	25			ns	
th	Hold Time	5.0			ns	

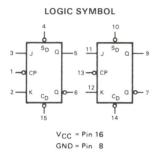


DESCRIPTION — The SN54LS/74LS112A dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

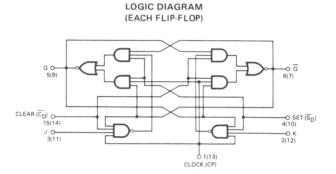
SN54LS112A SN74LS112A

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)



CVMAROL	PARAMETER			LIMITS		LINUTC	TEST CONDITIONS	
SYMBOL	PARAME	IEK	MIN	TYP	MAX	UNITS	IEST	ONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
		54			0.7		Guaranteed Inp	ut LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode V	oltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA
Voн	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$
VOH	Output more voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
1	Input HIGH Current	J, K Set, Clear Clock			20 60 80	μĄ	V _{CC} = MAX, V _I	N = 2.7 V
lін	input nigh current	J, K Set, Clear Clock			0.1 0.3 0.4	mA	V _{CC} = MAX, V _I	N = 7.0 V
I _{IL}	Input LOW Current	J, K Clear,Set,Clk			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
los	Short Circuit Curren	t	-20		-100	mA	V _{CC} = MAX	
lcc	Power Supply Curre	nt			6.0	mA	V _{CC} = MAX	

MODE SELECT - TRUTH TABLE

OPERATING MODE		INPUTS			OUT	PUTS
OPERATING MODE	\overline{s}_D	_CD	J	К	Q	ā
Set	L	Н	×	×	Н	L
Reset (Clear)	н	L	X	×	L	н
*Undetermined	L	L	X	×	н	Н
Toggle	н	н	h	h	q	q
Load "0" (Reset)	н	н	1	h	L	н
Load "1" (Set)	н	н	h	, 1	н	L
Hold	н	н	- 1	1	q	q

^{*}Both outputs will be HIGH while both \overline{s}_D and \overline{c}_D are LOW, but the output states are unpredictable if \overline{s}_D and \overline{c}_D go HIGH simultaneously.

H,h = HIGH Voltage Level L,I = LOW Voltage Level X = Don't Care

I, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

00/11011111	0. 2.0					
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	DARAMETER		LIMITS			TEST COMPLITIONS
	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
fMAX	Maximum Clock Frequency	30	45		MHz	Vac = 5 0 V
tPLH	PLH Propagation Delay, Clock		15	20	ns	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 15 \text{ pF}$
^t PHL	Clear, Set to Output		15	20	ns]

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

CVMAROL	DADAMETER		LIMITS		UNITS	TEST CONDITIONS		
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
tw	Clock Pulse Width High	20			ns			
tw	Clear, Set Pulse Width	25			ns	V _{CC} = 5.0 V		
t _S	Setup Time	20			ns	VCC = 5.0 V		
th	Hold Time	0			ns	*		

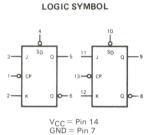


DESCRIPTION — The SN54LS/74LS113A offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

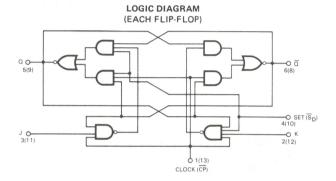
SN54LS113A SN74LS113A

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)



CVAAROL	DADAMETE	D		LIMITS		UNITS	TECT	ONDITIONS	
SYMBOL	PARAMETE	н	MIN	TYP	MAX	UNITS	TEST C	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
		54			0.7	.,		ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Vol	tage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA	
Voн	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$	
VОН	Output High Voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table	
		54,74		0.25	0.4	V	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN$, $V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table	
VOL	Output LOW Voltage	74		0.35	0.5	V			
Iн	Input HIGH Current	J, K Set Clock			20 60 80	μΑ	V _{CC} = MAX, V _I	N = 2.7 V	
	input high current	J, K Set Clock			0:1 0:3 0:4	mA	V _{CC} = MAX, V _I	N = 7.0 V	
lıL	Input LOW Current	J, K Set, Clock			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V		
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current	Power Supply Current			6.0	mA	V _{CC} = MAX		

MODE SELECT - TRUTH TABLE

OPERATING MODE		INPUTS		OUTPUTS		
OPERATING MODE	\overline{S} _D	J	K	Q	ā	
Set	L	×	Х	Н	L	
Toggle	н	h	h	q	q	
Load "0" (Reset)	н	1	h	L	Н	
Load ''1'' (Set)	н	h	1	н	L	
Hold	Н	1	. 1	q	\overline{q}	
	1	I				

H,h = HIGH Voltage Level

L,I = LOW Voltage Level
X = Don't Care

I, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	٧
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

CVMPOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
fMAX	Maximum Clock Frequency	30	45		MHz	V	
^t PLH	Propagation Delay, Clock		15	20	ns	$V_{CC} = 5.0 \text{ V}$ $C_{I} = 15 \text{ pF}$	
^t PHL	Set to Output		15	20	ns		

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	DADAMETED		LIMITS		UNITS	TEST CONDITIONS	
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t₩	Clock Pulse Width High	20			ns		
tW	Set Pulse Width	25			ns	Vac = 5.0 V	
t _S	Setup Time	20			ns	$V_{CC} = 5.0 \text{ V}$	
th	Hold Time	0		:	ns		



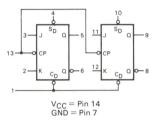
DESCRIPTION — The SN54LS/74LS114A offers common clock and common clear inputs and individual J, K, and set inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

SN54LS114A SN74LS114A

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

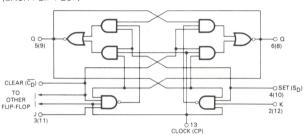
LOW POWER SCHOTTKY





J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

LOGIC DIAGRAM (EACH FLIP-FLOP)



SYMBOL	PARAMET	ED		LIMITS		UNITS	TEST CONDITIONS	
STIVIBUL	PARAIVIET	EK	MIN	TYP	MAX	UNITS	TEST C	ONDITIONS
VIH	Input HIGH Voltage		2.0			٧	Guaranteed Inp All Inputs	ut HIGH Voltage for
16.	t O\M\\/- t	54			0.7	V		ut LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode V	oltage		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN}$	=-18 mA
Voн	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$
•ОП	Output Filed Folloge	74	2.7	3.5		V	or V _{IL} per Truth	Table
1/-	0	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
	Input HIGH Current	J, K Set Clear Clock			20 60 120 160	μΑ	V _{CC} = MAX, V _{IN} = 2.7 V	
liн	Input nigh current	J, K Set Clear Clock			0.1 0.3 0.6 0.8	mA	VCC = MAX, VI	_N = 7.0 V
IIL	Input LOW Current	J, K Set Clear, Clock			-0.4 -0.8 -1.6	mA	V _{CC} = MAX, V _I	N = 0.4 V
los	Output Short Circuit Current		-20		-100	mA	V _{CC} = MAX	
Icc	Power Supply Current				6.0	mA	V _{CC} = MAX	

MODE SELECT - TRUTH TABLE

	,						
		INPUTS			OUTPUTS		
OPERATING MODE	\bar{s}_D	¯c _D	J	К	Q	ā	
Set	L	Н	×	×	Н	L	
Reset (Clear)	н	L	X	×	L	Н	
*Undetermined	L	L	×	X	н	Н	
Toggle	н	н	h	h	q	q	
Load "0" (Reset)	н	н	1	h	L	Н	
Load "1" (Set)	н	н	h	1	н	L	
Hold	н	н	1	- 1	q	q	

^{*}Both outputs will be HIGH while both \overline{s}_D and \overline{c}_D are LOW, but the output states are unpredictable if \overline{s}_D and \overline{c}_D go HIGH simultaneously.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ЮН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER	LIMITS			LINUTC	TECT COMPLTIONS	
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
fMAX	Maximum Clock Frequency	30	45		MHz		
^t PLH	Propagation Delay, Clock,		15	20	ns	$V_{CC} = 5.0 \text{ V}$ $C_{I} = 15 \text{ pF}$	
^t PHL	Clear, Set to Output		15	20	ns	5 - 15 μι	

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	DADAMETER		LIMITS			TEST CONDITIONS	
	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
tw	Clock Pulse Width High	20			ns		
tw	Clear, Set Pulse Width	25			ns	$V_{CC} = 5.0 \text{ V}$	
t _S	Setup Time	20			ns] VCC = 5.0 V	
th	Hold Time	0			ns		

H,h = HIGH Voltage Level

L,I = LOW Voltage Level X = Don't Care

I, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.



DESCRIPTION — These d-c triggered multivibrators feature pulse width control by three methods. The basic pulse width is programmed by selection of external resistance and capacitance values. The LS122 has an internal timing resistor that allows the circuits to be used with only an external capacitor. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-levelactive (B) inputs, or be reduced by use of the overriding clear.

The LS122 and LS123 have Schmitt trigger inputs to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

- OVERRIDING CLEAR TERMINATES OUTPUT PULSE
- COMPENSATED FOR VCC AND TEMPERATURE VARIATIONS
- D-C TRIGGERED FROM ACTIVE-HIGH OR ACTIVE-LOW GATED LOGIC INPUTS
- RETRIGGERABLE FOR VERY LONG OUTPUT PULSES, UP TO 100% DUTY CYCLE
- INTERNAL TIMING RESISTORS ON LS122

I S122 FUNCTIONAL TABLE

	IN	PUTS			OUT	PUTS
CLEAR	Α1	A2	В1	В2	Q	ā
L	X	X	X	X	L	Н
X	н	H	X	X	L	н
X	X	X	L	X	L	Н
X	X	X	X	L	L	Н
.H	L	X	1	. Н	Л	T
Н	L	X	Н	1	Л	T.
H	X	L	1	Н	л	: 1
Н	X	L	H	1	л	ъ
Н	Н	1	Н	Н	л	ъ
н	1	1	Н	Н	л	ъ
Н	1	Н	Н	Н	л	U
1	L	X	Н	Н	л	U
1	X	L	Н	Н	Л	П

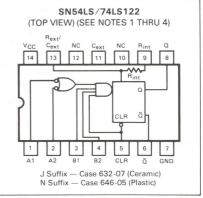
LS123 FUNCTIONAL TABLE

INP	UTS		OUTPUTS		
CLEAR	Α	В	Q	ā	
L	X	Х	L	Н	
X	н	Х	L	Н	
X	X	L	L	Н	
Н	L	1	л	T	
Н	1	Н	л	T	
-, †	L	Н	Л	T	

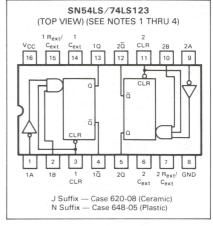
SN54LS/74LS122 SN54LS/74LS123

RETRIGGERABLE MONOSTABLE **MULTIVIBRATORS**

LOW POWER SCHOTTKY



NC - NO internal connection



NOTES:

- 1. An external timing capacitor may be connected between C_{ext} and $R_{\text{ext}'}/C_{\text{ext}}$ (positive). 2. To use the internal timing resistor of the LS122, connect R_{int} to V_{CC} . 3. For improved pulse width accuracy connect an external resistor between $R_{\text{ext}'}/C_{\text{ext}}$ and V_{CC} . with Rint open-circuited.
- 4. To obtain variable pulse widths, connect an external variable resistance between R_{int}/C_{ext} and V_{CC} .

TYPICAL APPLICATION DATA

The output pulse t_W is a function of the external components, C_{ext} and R_{ext} or C_{ext} and R_{int} on the LS122. For values of C_{ext} \geqslant 1000 pF, the output pulse at $V_{CC} = 5.0 \text{ V}$ and $V_{RC} = 5.0 \text{ V}$ (see Figures 1, 2, and 3) is given by

tW = K Rext Cext where K is nominally 0.45

If C_{ext} is on pF and R_{ext} is in $k\Omega$ then t_W is in nanoseconds.

The C_{ext} terminal of the LS122 and LS123 is an internal connection to ground, however for the best system performance C_{ext} should be hard-wired to ground.

Care should be taken to keep R_{ext} and C_{ext} as close to the monostable as possible with a minimum amount of inductance between the R_{ext}/C_{ext} junction and the R_{ext}/C_{ext} pin. Good groundplane and adequate bypassing should be designed into the system for optimum performance to insure that no false triggering occurs.

It should be noted that the C_{ext} pin is internally connected to ground on the LS122 and LS123, but not on the LS221. Therefore, if C_{ext} is hard-wired externally to ground, substitution of a LS221 onto a LS123 socket will cause the LS221 to become non-functional.

The switching diode is not needed for electrolytic capacitance application and should not be used on the LS122 and LS123.

To find the value of K for $C_{\text{ext}} \geqslant 1000 \, \text{pF}$, refer to Figure 4. Variations on V_{CC} or V_{RC} can cause the value of K to change, as can the temperature of the LS123, LS122. Figures 5 and 6 show the behaviour of the circuit shown in Figures 1 and 2 if separate power supplies are used for V_{CC} and V_{RC} . If V_{CC} is tied to V_{RC} , Figure 7 shows how K will vary with V_{CC} and temperature. Remember, the changes in R_{ext} and C_{ext} with temperature are not calculated and included in the graph.

As long as $C_{ext} \ge 1000$ pF and $5K \le R_{ext} \le 260$ K (SN74LS122/123) or $5K \le R_{ext} \le 160$ K (SN54LS122/123), the change in K with respect to R_{ext} is negligable.

If $C_{ext} \le 1000$ pF the graph shown on Figure 8 can be used to determine the output pulse width. Figure 9 shows how K will change for $C_{ext} \le 1000$ pF if V_{CC} and V_{RC} are connected to the same power supply. The pulse width two in nanoseconds is approximated by

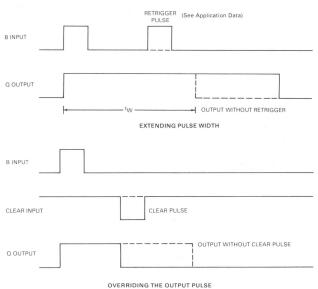
$$t_W = 6 + 0.05 C_{ext} (pF) + 0.45 R_{ext} (k\Omega) C_{ext} + 11.6 R_{ext}$$

In order to trim the output pulse width, it is necessary to include a variable resistor between V_{CC} and the R_{ext}/C_{ext} pin or between V_{CC} and the R_{ext} pin of the LS122. Figure 10, 11, and 12 show how this can be done. R_{ext} remote should be kept as close to the monostable as possible.

Retriggering of the part, as shown in Figure 3, must not occur before C_{ext} is discharged or the retrigger pulse will not have any effect. The discharge time of C_{ext} in nanoseconds is guaranteed to be less than 0.22 C_{ext} (pF) and is typically 0.05 C_{ext} (pF).

For the smallest possible deviation in output pulse widths from various devices, it is suggested that C_{ext} be kept ≥ 1000 pF.

WAVEFORMS



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	
Vcc	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA
R _{ext}	External Timing Resistance	54 74	5.0 5.0		180 260	kΩ
C _{ext}	External Capacitance	54,74		No Restric	tion	
R _{ext} /C _{ext}	Wiring Capacitance at Rext/Cext Terminal	54,74			50	pF

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

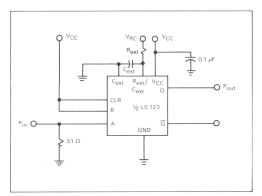
SYMBOL	PARAMETER	,		LIMITS		UNITS	TEST	ONDITIONS
STIVIBUL	PARAIVIETER	1	MIN	TYP	MAX	UNITS	TEST	CNDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
		54			0.7	.,		ut LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA
Voн	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$
VOH	Output mon voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN},$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V
ΙΗ	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V
ll.	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_I$	N = 0.4 V
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
Icc	Power Supply Current	LS122			11	mA	V _{CC} = MAX	
		LS123			20			

AC CHARACTERISTICS: $T_A = 25^{\circ}C$, $V_{CC} = 5.0 \text{ V}$

CVMAROL	DADAMETED		LIMITS		LINUTC	TEST COMPITIONS
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
^t PLH	Propagation Delay, A to Q		23	33	ns	
^t PHL	Propagation Delay, A to $\overline{\mathbb{Q}}$		32	45	113	$C_{\text{ext}} = 0$
^t PLH	Propagation Delay, B to Q		23	44	ns	C _L = 15 pF
^t PHL	Propagation Delay, B to $\overline{\mathbf{Q}}$		34	56	113	$R_{\text{ext}} = 5.0 \text{ k}\Omega$
^t PLH	Propagation Delay, Clear to $\overline{\Omega}$		28	45	ns	$R_L = 2.0 \text{ k}\Omega$
^t PHL	Propagation Delay, Clear to Q		20	27	113	
^t W min	A or B to Q		116	200	ns	
t _W Q	A to B to Q	4.0	4.5	5.0	μs	$C_{\text{ext}} = 1000 \text{ pF}, R_{\text{ext}} = 10 \text{ k}\Omega,$ $C_{\text{L}} = 15 \text{ pF}, R_{\text{L}} = 2.0 \text{ k}\Omega$

AC SETUP REQUIREMENTS: $T_A = 25^{\circ}C$, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER		LIMITS		UNITS
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS
tw	Pulse Width	40			ns



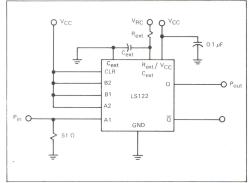


Fig. 1

Fig. 2

32

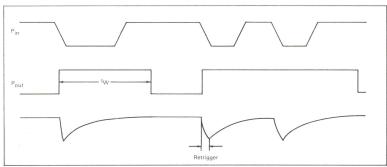
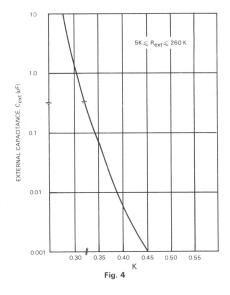
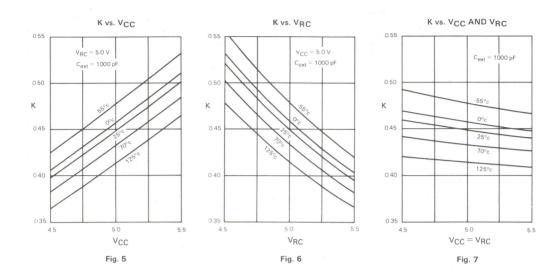
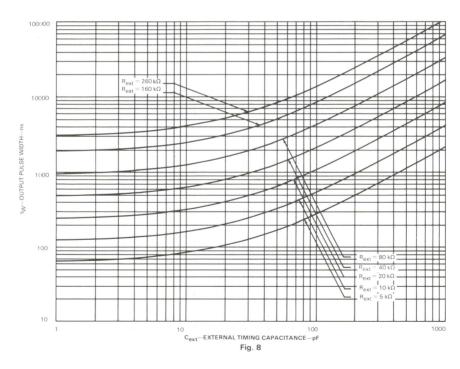


Fig. 3







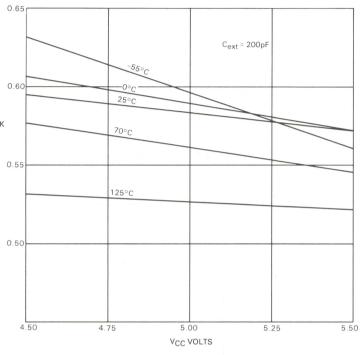


Fig. 9

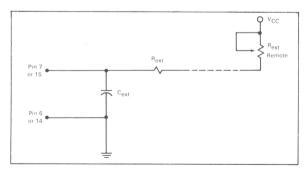


Fig. 10 - LS123 REMOTE TRIMMING CIRCUIT

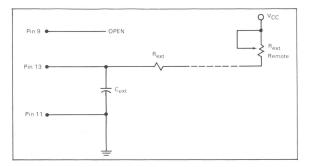


Fig. 11—LS122 REMOTE TRIMMING CIRCUIT WITHOUT Rext

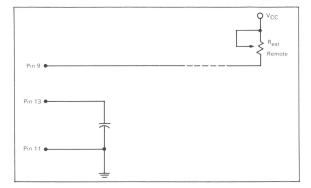


Fig. 12—LS122 REMOTE TRIMMING CIRCUIT WITH Rint



TRUTH TABLES

LS125A

	LS	1	2	6/
-	, 7	Г		

INP	UTS	OUTPUT
E	D	001701
L	L	L
L	Н	Н
Н	X	(Z)

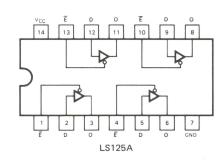
INP	UTS	ОИТРИТ
Е	D	001101
Н	L	L
Н	Н	Н
L	X	(Z)

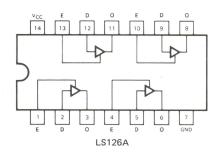
L = LOW Voltage Level

H = HIGH Voltage Level
X = Don't Care

(Z) = High Impedance (off)

J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)





SN54LS/74LS125A SN54LS/74LS126A

QUAD 3-STATE BUFFERS LOW POWER SCHOTTKY

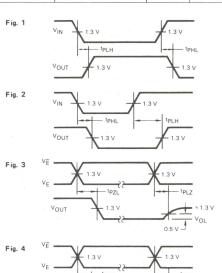
SYMBOL	PARAMETER			LIMITS		LINITC	TECT	CONDITIONS	
STIVIBUL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for	
		54			0.7			put LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	ige		-0.65	-1.5	V	V _{CC} = MIN, III	N =−18 mA	
Voн	Output HIGH Voltage	54	2.4			V	V _{CC} = MIN, I _C	$O_H = MAX, V_{IN} = V_{IH}$	
VOH	Output man voltage	74	2.4			V	or V _{IL} per Truth Table		
		54,74		0.25	0.4	V	I _{OL} = 12 mA V _{CC} = V _{CC} MIN,	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 24 mA	VIN = VIL or VIH per Truth Table	
lozh	Output Off Current HIG	Н			20	μΑ	VCC = MAX, V	/ _{OUT} = 2.4 V	
lozL	Output Off Current LOV	V			-20	μΑ	V _{CC} = MAX, \	/ _{OUT} = 0.4 V	
l	Input HIGH Current				20	μΑ	V _{CC} = MAX, \	/ _{IN} = 2.7 V	
lн	input nigh current				0.1	mA	V _{CC} = MAX, \	/ _{IN} = 7.0 V	
IIL	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_{IN} = 0.4V$		
los	Short Circuit Current		-40		-225	mA	V _{CC} = MAX	V _{CC} = MAX	
lcc	Power Supply Current	LS125A			20	mA	Vcc = MAX	$V_{IN} = 0 \text{ V}, V_E = 4.5 \text{ V}$	
.00	Tower Supply Current	LS126A			22	IIIA	VCC - WIAX,	$V_{IN} = 0 \text{ V}, V_E = 4.5 \text{ V}$ $V_{IN} = 0 \text{ V}, V_E = 0 \text{ V}$	

GUARANTEED OPERATING RANGES

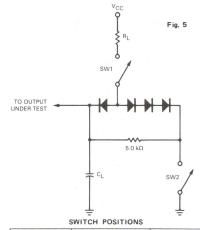
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
Тд	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ОН	Output Current — High	54 74			-1.0 -2.6	mA
lor	Output Current — Low	54 74			12 24	mA

AC CHARACTERISTICS: $T_A = 25$ °C

SYMBOL	DADAMETE	n		LIMITS		UNITS	TEST CONDITIONS		
STIMBOL	PARAMETE	н	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
^t PLH		LS125A		9.0	15				
tPLH	Propagation Delay,	LS126A		9.0	15	ns	Fig. 2		
^t PHL	Data to Output	LS125A		7.0	18		$V_{CC} = 5.0 \text{ V}$		
tPHL:		LS126A		8.0	18				
	Output Enable Time	LS125A		12	20		Figs. 4, 5	$C_L = 45 \text{ pF}$ $R_L = 667 \Omega$	
^t PZH	to HIGH Level	LS126A		16	25	ns			
4	Output Enable Time	LS125A		15	25		F: 2 F		
^t PZL	to LOW Level	LS126A		21	35	ns	Figs. 3, 5		
	Output Disable Time	LS125A			20		F: 4 F		
[†] PHZ	from HIGH Level	LS126A			25	ns	Figs. 4, 5	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 5.0 \text{ pF}$	
	Output Disable Time	LS125A			20	ns	Figs 2 F	$R_L = 667 \Omega$	
^t PLZ	from LOW Level	LS126A			25		Figs. 3, 5		



 v_{OUT}



SYMBOL	SW1	SW2
tPZH	Open	Closed
tPZL	Closed	Open
tPLZ	Closed	Closed
tPHZ	Closed	Closed

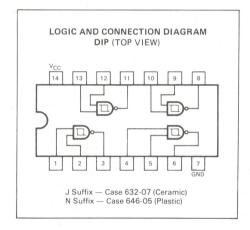


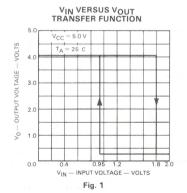
DESCRIPTION — The SN54LS/74LS132 contains four 2-Input NAND Gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional NAND Gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than $V_{\rm T+}$ (MAX), the gate will respond to the transitions of the other input as shown in Figure 1.

SN54LS132 SN74LS132

QUAD 2-INPUT
SCHMITT TRIGGER NAND GATE
LOW POWER SCHOTTKY





GUARANTEED OPERATING RANGES

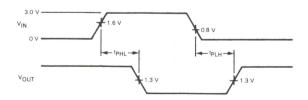
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	· V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ЮН	Output Current — High	54,74			-0.4	mA
OL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMADOL	DADAMETER			LIMITS		LINUTO	TECT CONDITIONS
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{T+}	Positive-Going Thresho	ld Voltage	1.5		2.0	V	V _{CC} = 5.0 V
V_{T-}	Negative-Going Threshold Voltage		0.6		1.1	V	V _{CC} = 5.0 V
V _T +-V _T _	Hysteresis		0.4	0.8		V	V _{CC} = 5.0 V
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} =- 18 mA
Vou	Output HIGH Voltage	54	2.5	3.4		V	$V_{CC} = MIN, I_{OH} = -400 \mu A, V_{IN} = V_{II}$
Voн	Output HIGH Voltage	74	2.7	3.4	8.1		$\sqrt{CC} = 101101, 10H = -400 \mu A, \sqrt{N} = \sqrt{C}$
VOL	Output LOW Voltage	54,74		0.25	0.4	V	$V_{CC} = MIN, I_{OL} = 4.0 \text{ mA}, V_{IN} = 2.0 \text{ V}$
OL	o atput 2011 voltago	74		0.35	0.5	V	$V_{CC} = MIN, I_{OL} = 8.0 \text{ mA}, V_{IN} = 2.0 \text{ V}$
I _{T+}	Input Current at			-0.14		mA	V00 - 5 0 V V - V
'1+	Positive-Going Thresho	ld		-0.14		IIIA	$VCC = 5.0 \text{ V}, V_{IN} = V_{T+}$
IT-	Input Current at			-0.18		mA	Voc. 50000
11-	Negative-Going Thresh	old		-0.18		IIIA .	$V_{CC} = 5.0 \text{ V}, V_{IN} = V_{T-}$
IIH	Input HIGH Current				20	μΑ	$V_{CC} = MAX, V_{IN} = 2.7 V$
'IH	Imput man current				0.1	mA	$V_{CC} = MAX, V_{IN} = 7.0 V$
IIL	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_{IN} = 0.4 V$
los	Output Short Circuit Current		-20		-100	mA	V _{CC} = MAX, V _{OUT} = 0 V
	Power Supply Current			1.5	-		
ICC	Total, Output HIGH			5.9	11	mA	$V_{CC} = MAX, V_{IN} = 0 V$
	Total, Output LOW			8.2	14	mA	$V_{CC} = MAX$, $V_{IN} = 4.5 V$

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	DADAMETER	LIMITS			UNITS	TEST COMPITIONS	
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH	Turn Off Delay, Input to Output			22	ns	V _{CC} = 5.0 V	
^t PHL	Turn On Delay, Input to Output			22	ns	C _L = 15 pF	



THRESHOLD VOLTAGE AND HYSTERESIS VERSUS POWER SUPPLY VOLTAGE

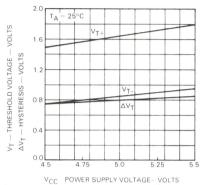


Fig. 2

THRESHOLD VOLTAGE AND HYSTERESIS VERSUS TEMPERATURE

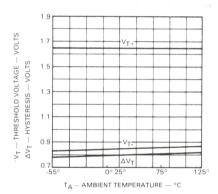
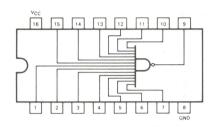


Fig. 3





J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

SN54LS133 SN74LS133

13-INPUT NAND GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

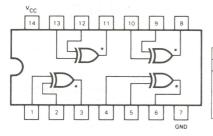
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMADOL	DADAMETE			LIMITS		UNITS	TEST CONDITIONS		
SYMBOL	PARAMETER	1	MIN	TYP	MAX	UNITS	TEST	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage f All Inputs		
		54			0.7	.,		ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA	
Voн	Output HIGH Voltage	54	2.5	3.5	Х.	V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = $ or V_{IL} per Truth Table		
VOH	Output man voltage	74	2.7	3.5		V			
		54,74	-	0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	VIN = VIL or VIH per Truth Table	
					20	μΑ	V _{CC} = MAX, V _I	N = 2.7 V	
lн	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _I	N = 7.0 V	
IIL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V	
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$		
Power Supply Curren Total, Output HIGH					0.5	mA	V _{CC} = MAX		
	Total, Output LOW				1.1	mA	ACC — INIMA		

AC CHARACTERISTICS: $T_A = 25$ °C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
STIVIBUL		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH	Turn Off Delay, Input to Output		10	15	ns	V _{CC} = 5.0 V	
tPHL	Turn On Delay, Input to Output		40	59	ns	$C_L = 15 pF$	





TRUTH TABLE

11	V	OUT
A	В	Z
L	L	L
L	н	н
Н	L	н
Н	н	L

SN54LS136 SN74LS136

QUAD 2-INPUT EXCLUSIVE OR GATE

LOW POWER SCHOTTKY

*OPEN COLLECTOR OUTPUTS

J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
VOH	Output Voltage — High	54,74			5.5	V
lor	Output Current — Low	54 74			4.0 8.0	mA

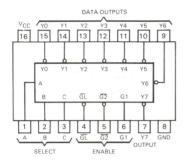
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMAROL	DADAMETED			LIMITS		LINUTC	TEST CONDITIONS	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS		
VIH	Input HIGH Voltage	nput HIGH Voltage				V	Guaranteed Inp All Inputs	ut HIGH Voltage for
		54			0.7	.,	Guaranteed Input LOW Voltage for	
V _{IL}	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	ige		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$	
ЮН	Output HIGH Current	54,74			100	μΑ	$V_{CC} = MIN, V_{OH} = MAX$	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
					40	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V
IH	Input HIGH Current				0.2	mA	$V_{CC} = MAX, V_{IN} = 7.0 \text{ V}$	
lıL	Input LOW Current			- 5	-0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
cc	Power Supply Current				10	mA	V _{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST COMPLITIONS
		MIN	TYP	MAX	OWITS	TEST CONDITIONS
^t PLH ^t PHL	Propagation Delay, Other Input LOW		18 18	30 30	ns	V _{CC} = 5.0 V
^t PLH ^t PHL	Propagation Delay, Other Input HIGH		18 18	30 30	ns	$C_L = 15 \text{ pF}, R_L = 2.0 \text{ k}\Omega$





J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

SN54LS137 SN74LS137

3-LINE TO 8-LINE
DECODERS/DEMULTIPLEXERS
WITH ADDRESS LATCHES

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

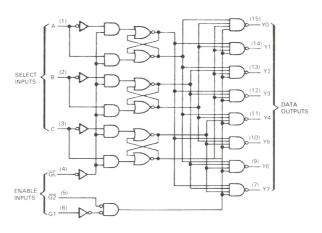
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lor	Output Current — Low	54 74			4.0 8.0	mA

CVAADOL	DADAMETER			LIMITS		LINUTC	TECT	ONDITIONS
SYMBOL	PARAMETER	1	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
		54			0.7		Guaranteed Inp	ut LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA
Vон	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$
VОН	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
V _{OL}	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V
lн	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _I	N = 7.0 V
lıL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V
os	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
lcc	Power Supply Current				18	mA	V _{CC} = MAX	

FI	INCTI	TIME	ARI	F

		INP	UTS			OUTPUTS							
E	ENABLE			SELECT					OUT	PUTS			
GL	G1	G2	С	В	А	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X L	H X	X	×	X	H	H H	H	H H	Н	Н	H	H
L L L	H H H	L L L	L L L	L L H	L H L	H H H	H L H	H L H	H H L	H H H	H	H H H	H H H
L L L	H H H	L L L	H H H	L H H	L H L	H H H	Н Н Н	Н Н Н	H H H	H H H	H H H	H H L	H H L
Н	Н	L	Х	X	X	Output corresponding to stored address, L; all others, H							

 $\mathsf{H} = \mathsf{high} \; \mathsf{level}, \, \mathsf{L} = \mathsf{low} \; \mathsf{level}, \, \mathsf{X} = \mathsf{irrelevant}$



AC CHARACTERISTICS: $V_{CC} = 5.0 \text{ V}, T_A = 25^{\circ}\text{C}$

CVMBOL	DADAMETER	LEVELS OF		LIMITS		LINUT	TEST
SYMBOL	PARAMETER	DELAY	MIN	TYP	MAX	UNIT	CONDITIONS
^t PLH ^t PHL	Propagation Delay Time, A,B,C to Y	2 4		11 25	17 38	ns	
^t PLH ^t PHL	Propagation Delay Time, A,B,C to Y	3 3		16 19	24 29	ns	
tPLH tPHL	Propagation Delay Time, Enable \$\overline{G2}\$ to Y	2 2		13 16	21 27	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
tPLH tPHL	Propagation Delay Time, Enable G1 to Y	3 3		14 18	21 27	ns	С[— 15 рг
^t PLH ^t PHL	Propagation Delay Time, Enable GL to Y	3 4		18 25	27 38	ns	

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER		LIMITS			TEST CONDITIONS		
	PARAIVIETER	MIN	TYP	MAX	UNITS	1231 CONDITIONS		
tw	Pulse Width — Enable at GL	15			ns			
t _S	Setup Time, A,B,C	10			ns	$V_{CC} = 5.0 V$		
t _h	Hold Time, A,B,C	10	10		ns			



DESCRIPTION — The LSTTL/MSI SN54LS/74LS138 is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138s and one inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- DEMULTIPLEXING CAPABILITY
- MULTIPLE INPUT ENABLE FOR EASY EXPANSION
- TYPICAL POWER DISSIPATION OF 32 mW
- ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION **EFFECTS**

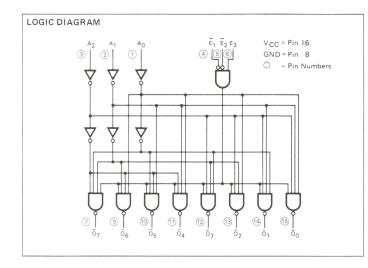
PIN NAMES

LOADING	(Note a)

		HIGH	LOW
$ \begin{array}{c} A_0 - A_2 \\ \overline{E}_1, \overline{E}_2 \\ E_3 \\ \overline{O}_0 - \overline{O}_7 \end{array} $	Address Inputs Enable (Active LOW) Inputs Enable (Active HIGH) Input Active LOW Outputs (Note b)	0.5 U.L. 0.5 U.L. 0.5 U.L. 10 U.L.	0.25 U.L. 0.25 U.L. 0.25 U.L. 5(2.5) U.L.

NOTES:

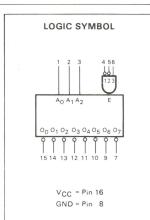
- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.



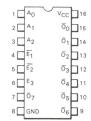
SN54LS138 SN74LS138

1-OF-8-DECODER/ **DEMULTIPLEXER**

LOW POWER SCHOTTKY



CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs $(\overline{O}_0 \cdot \overline{O}_7)$. The LS138 features three Enable inputs, two active LOW $(\overline{E}_1, \overline{E}_2)$ and one active HIGH (E_3) . All outputs will be HIGH unless \overline{E}_1 and \overline{E}_2 are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LS138s and one inverter. (See Figure a.)

The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRI	ITH	TA	RI	E

		INP	UTS						OUT	PUTS			
Ē ₁	\overline{E}_2	E ₃	A ₀	Α1	A ₂	\bar{o}_0	\overline{o}_1	\overline{o}_2	\overline{o}_3	04	\bar{o}_5	\overline{o}_6	\overline{o}_7
Н	X	X	×	×	X	Н	Н	Н	Н	Н	Н	Н	Н
×	Н	×	×	X	X	н	Н	Н	Н	Н	Н .	Н	Н
×	×	L	×	×	X	Н	Н	Н	Н	Н	Н	Н	Н
L	L	н	- L	L	L	L	Н	Н	Н	Н	H	H	Н
L	L	H	н	· L	L	н	L	Н	Н	Н	Н	Н	н
L	L	Н	L	Н	L	н	Н	L	Н	Н	Н	Н	Н
L	L	Н	Н	Н	L	н	Н	Н	L	Н	Н	Н	Н
L	L	Н	L	L	Н	Н	•н	Н	Н	L	Н	. Н	Н
L	L	Н	Н	L	Н	н	Н	Н	Н	Н	L	Н	Н
L	L	Н	T.	Н	Н	н	Н	Н	Н	Н	Н	L	Н
L	L	Н	н	Н	Н	н	Н	Н	Н	Н	Н	Н	L

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Don't Care

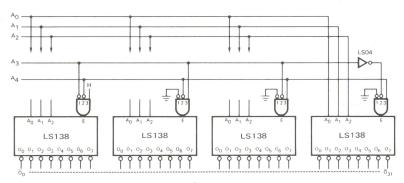


Fig. a.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	٧
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	R .	MIN TYP MA		MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage	8	2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
.,	1	54			0.7	.,		ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age	7	-0.65	-1.5	V	V _{CC} = MIN, I _{IN} =-18 mA		
Vон	Output HIGH Voltage	54	2.5	3.5		V		$=$ MAX, $V_{IN} = V_{IH}$	
∨ОН	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth Table		
.,		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
IH	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_{IN} = 7.0 \text{ V}$		
IL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V	
os	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
cc	Power Supply Current				10	mA	V _{CC} = MAX		

AC CHARACTERISTICS: $T_A = 25$ °C

SYMBOL	PARAMETER	LEVEL OF		LIMITS		LINUTC	TEST
STIVIBOL	PANAIVIETEN	DELAY	MIN	TYP	MAX	UNITS	CONDITIONS
^t PLH ^t PHL	Propagation Delay Address to Output	2 2		13 27	20 41	ns	
^t PLH ^t PHL	Propagation Delay Address to Output	3 3		18 26	27 39	ns	V _{CC} = 5.0 V
tPLH tPHL	Propagation Delay Enable to Output	2 2		12 21	18 32	ns	$C_L = 15 pF$
^t PLH ^t PHL	Propagation Delay Enable to Output	3		17 25	26 38	ns	

AC WAVEFORMS

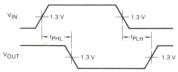


Fig. 1

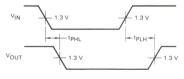


Fig. 2



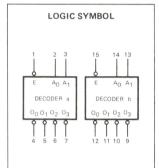
DESCRIPTION — The LSTTL/MSI SN54LS/74LS139 is a high speed Dual 1-of-4 Decoder/Demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW Outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the LS139 can be used as a function generator providing all four minterms of two variables. The LS139 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- TWO COMPLETELY INDEPENDENT 1-OF- 4 DECODERS
- ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION **EFFECTS**

SN54LS139 SN74LS139

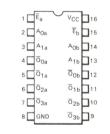
DUAL 1-OF-4-DECODER/ DEMULTIPLEXER

LOW POWER SCHOTTKY



V_{CC} = Pin 16 GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

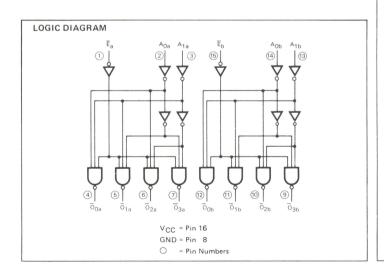
PIN NAMES

A₀, A₁ Address Inputs Enable (Active LOW) Input $\overline{O}_0 - \overline{O}_3$

Active LOW Outputs (Note b)

1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges



LOADING (Note a)

LOW

0.25 U.L.

0.25 U.L.

5 (2.5) U.L.

HIGH

0.5 U.L.

0.5 U.L.

10 U.L.

FUNCTIONAL DESCRIPTION — The LS139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A₀, A₁) and provide four mutually exclusive active LOW outputs $(\overline{O}_0 - \overline{O}_3)$. Each decoder has an active LOW Enable (\overline{E}) . When \overline{E} is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application.

Each half of the LS139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

		INPUTS		OUTPUTS							
	Ē	A ₀	Α1	\overline{o}_0	\overline{o}_1	\overline{o}_2	\overline{o}_3				
	Н	×	×	Н	Н	Н	Н				
	L	L	L	L	Н	Н	Н				
	L	Н	L	н	L	Н	Н				
100	L	L	Н	н	H	L	Н				
	L	Н	Н	н	Н	Н	L				

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

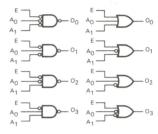


Fig. a

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

SYMBOL	PARAMETER			LIMITS		UNITS	TECT	ONDITIONS		
STIVIBUL	PARAIVIETER	1	MIN	TYP	MAX	UNITS	TEST	ONDITIONS		
VIH	Input HIGH Voltage		2.0			٧	Guaranteed Inp All Inputs	ut HIGH Voltage for		
	1	54			0.7	.,		ut LOW Voltage for		
VIL	Input LOW Voltage	74			0.8	V	All Inputs	All Inputs		
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	= MIN, I _{IN} =-18 mA		
Voн	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$		
*OH	Output High Voltage	74	2.7	3.5		V	or V _{IL} per Truth Table			
	Output LOW Voltage	54,74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} M			
VOL		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table		
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V		
ΙΗ	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V		
ll	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V			
os	Short Circuit Current		-20		-100	mA	V _{CC} = MAX			
lcc	Power Supply Current				11	mA	$V_{CC} = MAX$			

AC CHARACTERISTICS: $T_A = 25$ °C

CVMBOL	DADAMETER	LEVEL OF	LIMITS			LINUTC	TEST	
SYMBOL tplh tphl tplh tphl tphl	PARAMETER	DELAY	MIN	TYP MAX		UNITS	CONDITIONS	
	Propagation Delay Address to Output	2 2		13 22	20 33	ns		
	Propagation Delay Address to Output	3 3		18 25	29 38	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$	
^t PLH ^t PHL	Propagation Delay Enable to Output	2 2		16 21	24 32	ns		

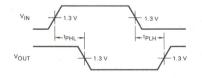


Fig. 1

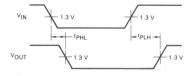


Fig. 2



DESCRIPTION — The SN54LS/74LS145, 1-of-10 Decoder/Driver, is designed to accept BCD inputs and provide appropriate outputs to drive 10-digit incandescent displays. All outputs remain off for all invalid binary input conditions. It is designed for use as indicator/relay drivers or as an open-collector logic circuit driver. Each of the high breakdown output transistors will sink up to 80 mA of current. Typical power dissipation is 35 mW. This device is fully compatible with all TTL families

SN54LS145 SN74LS145

1-OF-10 DECODER/DRIVER OPEN-COLLECTOR

LOW POWER SCHOTTKY

- LOW POWER VERSION OF 54/74145
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

LOADING (Note a)

PIN NAMES

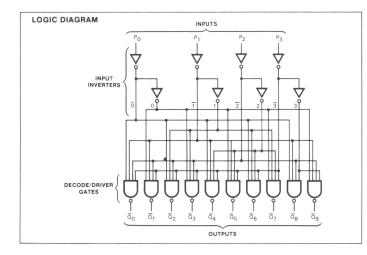
 P_0 , P_1 , P_2 , P_3 BCD Inputs Q_0 to Q_9 Outputs (Note b)

HIGH	LOW
0.5 U.L.	0.25 U.L.
Open Collector	15 (7.5) U.L.

NOTES

a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

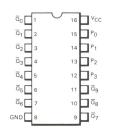
b. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges



Po P1 P2 P3 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 1 2 3 4 5 6 7 9 10 11 VCC = Pin 16 GND = Pin 8

LOGIC SYMBOL

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

TRUTH TABLE

	INP	UTS						OUT	PUTS				
P ₃	P ₂	P ₁	P ₀	\bar{a}_0	\overline{Q}_1	\overline{Q}_2	\overline{Q}_3	<u>0</u> 4	\bar{a}_5	ō ₆	ā ₇	ā ₈	ā ₉
L	L	L.	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н
L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н
L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н
L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н
L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
L	H	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н
Н	L	L	L	Н	Н	Н	Н	Н	Н	H	Н	L	Н
H	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
H	L	H	L	Н	Н	Н	Н	Н	Н	H	Н	Н	H
Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Н	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	H
H	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н

H = HIGH Voltage Level L = LOW Voltage Level

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
Vcc	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
Voн	Output Voltage — High	54,74			15	V
lOL	Output Current — Low	54 74			12 24	mA

0.440.01	DADAMETE			LIMITS		LINITO	TEST COMPITIONS
SYMBOL	PARAMETER	{	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
		54			0.7	.,	Guaranteed Input LOW Voltage for
VIL	Input LOW Voltage	74		1	0.8	V	All Inputs
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$
ГОН	Output HIGH Current	54,74			250	μΑ	$V_{CC} = MIN, V_{OH} = MAX$
		54,74		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN},$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 24 \text{ mA} \mid V_{IN} = V_{IL} \text{ or } V_{IH}$
		54,74		2.3	3.0	V	I _{OL} = 80 mA per Truth Table
					20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$
lн	Input HIGH Current				0.1	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$
IIL	Input LOW Current				-0.4	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$
lcc	Power Supply Current				13	mA	V _{CC} = MAX, V _{IN} = GND

AC CHARACTERISTICS: $T_A = 25$ °C

SYMBOL	DADAMETER	LIMITS			LIMITO	TECT COMPITIONS
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
tPHL tPLH	Propagation Delay Pn Input to Qn Output			50 50	ns	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 45 \text{ pF}$

AC WAVEFORMS

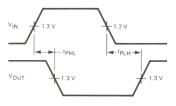


Fig. 1

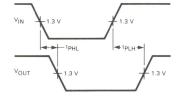


Fig. 2



DESCRIPTION — The SN54LS/74LS147 and the SN54LS/74LS148 are Priority Encoders. They provide priority decoding of the inputs to ensure that only the highest order data line is encoded. Both devices have data inputs and outputs which are active at the low logic level.

The LS147 encodes nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition does not require an input condition because zero is encoded when all nine data lines are at a high logic level.

The LS148 encodes eight data lines to three-line (4-2-1) binary (octal). By providing cascading circuitry (Enable Input El and Enable Output EO) octal expansion is allowed without needing external circuitry.

The SN54LS/74LS748 is a proprietary Motorola part incorporating a built-in deglitcher network which minimizes glitches on the GS output. The glitch occurs on the negative going transition of the El input when data inputs 0-7 are at logical ones.

The only dc parameter differences between the LS148 and the LS748 are that (1) Pin 10 (input 0) has a fan-in of 2 on the LS748 versus a fan-in of 1 on the LS148; (2) Pins 1, 2, 3, 4, 11, 12 and 13 (inputs 1, 2, 3, 4, 5, 6, 7) have a fan-in of 3 on the LS748 versus a fan-in of 2 on the LS148.

The only ac difference is that tpHL from EI to EO is changed from 40 to 45 $\,$ ns.

SN54LS/74LS147
FUNCTION TABLE

	TOTOTION TABLE													
			IN	IPU	rs				(UTI	PUT	s		
1	2	3	4	5	6	7	8	9	D	С	В	Α		
Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н		
X	X	X	X	X	X	X	X	L	L	Н	Н	L		
X	X	X	X	X	X	X	L	Н	L	Н	Н	Н		
X	X	X	X	X	X	L	Н	Н	Н	L	L	L		
X	X	X	X	X	L	Н	Н	Н	Н	L	L	Н		
X	X	X	X	L	Н	Н	H	H	Н	L	Н	L		
X	X	X	L	Н	Н	Н	Н	Н	Н	L	Н	Н		
X	X	L	Н	Н	Н	Н	Н	Н	Н	Н	L	.L		
X	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н		
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L		

SN54LS/74LS148 SN54LS/74LS748 FUNCTION TABLE

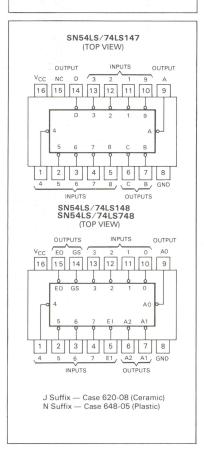
			11	NPL	JTS					0	UTF	UTS	3
ΕI	0	1	2	3	4	5	6	7	Α2	Α1	A0	GS	EO
Н	Χ	Χ	Χ	X	X	X	X	X	Н	Н	Н	Н	Н
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	X	X	X	Χ	X	X	X	L	L	L	L	L	Н
L	X	X	X	Χ	Χ	X	L	Н	L	L	Н	L	Н
L	Χ	X	Χ	X	Χ	L	Н	Н	L	Н	L	L	Н
L	Χ	Χ	Χ	X	L	Н	Н	Н	L	Н	Н	L	Н
L	X	X	Χ	L	Н	Н	Н	Н	Н	L	L	L	Н
L	Χ	Χ	L	Н	Н	Н	Н	Н	Н	L	Н	L	Н
L	X	L	Н	Н	Н	Н	Н	Н	Н	Н	L	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н

H = high logic level, L = low logic level, X = irrelevant

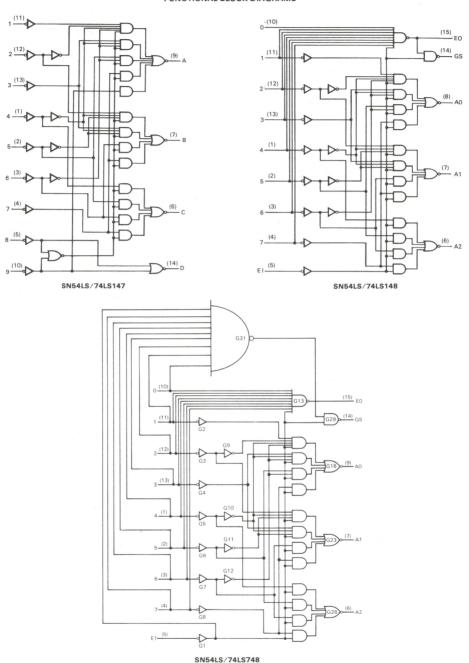
SN54LS/74LS147 SN54LS/74LS148 SN54LS/74LS748

10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

LOW POWER SCHOTTKY



FUNCTIONAL BLOCK DIAGRAMS



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ЮН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST	CONDITIONS
OTIVIDOL	FARAIVIETER		MIN	TYP	MAX	UNITS	TEST	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for
.,		54			0.7	.,		put LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = MIN, I_{II}$	$_{N} = -18 \text{ mA}$
Vон	Output HIGH Voltage	54	2.5	3.5		V		$_{H} = MAX, V_{IN} = V_{IH}$
VOH	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	$V_{IN} = V_{IL}$ or V_{IH} per Truth Table
I _I н	Input HIGH Current All Others Input 0 (LS748) Inputs 1-7 (LS148) Inputs 1-7 (LS748)				20 40 40 60	μΑ	V _{CC} = MAX, V	1 _{IN} = 2.7 V
1111	All Others Input 0 (LS748) Inputs 1-7 (LS148) Inputs 1-7 (LS748)				0.1 0.2 0.2 0.3	mA	V _{CC} = MAX, V	γ _{IN} = 7.0 V
IIL	Input LOW Current All others Input 0 (LS748) Inputs 1-7 (LS148) Inputs 1-7 (LS748)				-0.4 -0.8 -0.8 -1.2	mA	V _{CC} = MAX, V	$\gamma_{\rm IN}=0.4~{\rm V}$
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX	
lcc	Power Supply Current				20	mA	V _{CC} = MAX, II Open	nputs 7, EI, GND, Others
					17	mA	V _{CC} = MAX, A	All open

AC CHARACTERISTICS: $V_{CC} = 5.0 \text{ V}$, $T_A = 25^{\circ}\text{C}$

SN54LS/74LS147

	FROM	ТО		LIMITS				1 - 2 - 11 - 1 - 1	
SYMBOL	(INPUT)	(OUTPUT)	WAVEFORM	MIN	N TYP MAX		UNIT	TEST CONDITIONS	
t _{PLH}	Anv	Any	In-phase		12	18	ns		
^t PHL	Ally	Ally	output		12	18	113	CL = 15 pF,	
^t PLH	Any	Any	Out-of-phase		21	33	ns	$R_L = 2 k\Omega$	
^t PHL	7.1.7	7,	output		15	23	110		

SN54LS/74LS148 SN54LS/74LS748

CVAAROL	FROM	TO	WAVEFORM	I	IMIT	S	UNIT	TEST CONDITIONS	
SYMBOL	(INPUT)	(OUTPUT)	VVAVEFORIVI	MIN	TYP	MAX	UNIT		
^t PLH	1 thru 7	A0, A1, or A2	In-phase		14	18	ns		
^t PHL	T till d /	70, 71, 01 72	output		15	25	110		
^t PLH	1 thru 7	A0, A1, or A2	Out-of-phase		20	36	ns		
^t PHL	T till d 7	A0, A1, 01 A2	output		16	29	113		
^t PLH	Othru 7	EO	Out-of-phase		7.0	18	ns		
^t PHL	O tilla 7	Ľ.O	output		25	40	113	$C_L = 15 pF$,	
^t PLH	0 thru 7	GS	In-phase		35	55	ns	$R_L = 2 k\Omega$,	
tPHL	O tilla 7	43	output		9.0	21	113		
^t PLH	EI	A0, A1, or A2	In-phase		16	25	ns		
^t PHL	Li	A0, A1, 01 A2	output		12	25	113		
^t PLH	EI	GS	In-phase		12	17	ns		
^t PHL	LI	33	output		14	36	113		
^t PLH	EI	EO	In-phase		12	21	ns		
^t PHL		20	output		28 30	40 45	115	(LS148) (LS748)	



DESCRIPTION — The TTL/MSI SN54LS/74LS151 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- FULLY BUFFERED COMPLEMENTARY OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

SN54LS151 SN74LS151

8-INPUT MULTIPLEXER

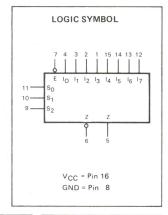
LOW POWER SCHOTTKY

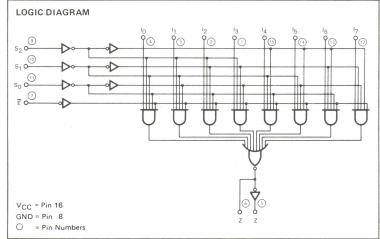
PIN NAMES		LOADIN	IG (Note a)
		HIGH	LOW
$\frac{S_0 - S_2}{\overline{E}}$	Select Inputs	0.5 U.L.	0.25 U.L.
Ē	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
10 - 17	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.
Z	Complementary Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.
NOTES			

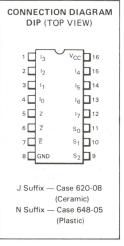
NOTES:

a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.







FUNCTIONAL DESCRIPTION — The LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S₀, S₁, S₂. Both assertion and negation outputs are provided. The Enable input (E) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$\begin{split} Z &= \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + \\ & I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2). \end{split}$$

The LS151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the LS151 can provide any logic function of four variables and its negation.

TRUTH TABLE

Ē	S ₂	S ₁	s ₀	10	11	12	13	14	15	16	17	Ž	Z
Н	X	×	X	X	×	X	X	X	X	X	X	Н	L
L	L	L	L	L	×	×	X	X	X	×	X	Н	L
L	L	L	L	Н	×	X	×	×	X	×	×	L	н
L	L	L	Н	×	L	×	×	×	X	×	X	н	L
L	L	L	Н	×	Н	X	×	X	X	X	X	L	н
L	L	Н	L	X	×	L	X	×	X	×	×	Н	L
L	L	Н	L	X	×	Н	X	×	×	×	×	L	Н
L	L	. Н	Н	×	×	X	L	×	X	X	×	Н	L
L	L	Н	Н	×	×	×	Н	×	X	×	X	L	н
L	н	L	L	×	×	×	×	L	X	×	X	Н	L
L	н	L	L	×	X	×	X	Н	×	×	X	L	н
L	н	L	Н	×	X	X	×	X	L	X	X	Н	L
L	н	L	Н	X	×	×	X	×	Н	×	×	·L	н
L	Н	Н	L	×	X	X	X	X	×	L	×	н	L
L	н	Н	L	X	×	×	×	×	×	н	×	L	н
L	н	Н	Н	×	×	X	×	X	×	×	L	Н	L
L	Н	Н	Н	×	X	X	X	X	X	X	Н	L	Н

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
Vcc	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

CVMBOL	DADAMETER	,		LIMITS		LINITO	TEST	ONDITIONS	
SYMBOL	PARAMETER	TANAMETER		TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
		54			0.7		Guaranteed Inp	ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} =-18 mA		
Voн	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$	
VOH	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth Table		
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
IH	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
İIL	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_I$	N = 0.4 V	
os	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$		
lcc	Power Supply Current				10	mA	V _{CC} = MAX		

AC CHARACTERISTICS: TA = 25°C

0)/14001	DADAMETED		LIMITS		LINUTC	TEST CONDITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH ^t PHL	Propagation Delay Select to Output Z		27 18	43 30	ns		
^t PLH ^t PHL	Propagation Delay Select to Output Z		14 20	23 32	ns	*	
^t PLH ^t PHL	Propagation Delay Enable to Output Z		26 20	42 32	ns	V _{CC} = 5.0 V	
tPLH tPHL	Propagation Delay Enable to Output Z		15 18	24 30	ns	$C_L = 15 pF$	
^t PLH ^t PHL	Propagation Delay Data to Output Z		20 16	32 26	ns		
^t PLH ^t PHL	Propagation Delay Data to Output Z		13 12	21 20	ns		

AC WAVEFORMS

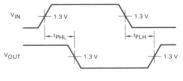


Fig. 1

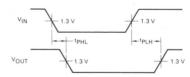


Fig. 2



DESCRIPTION — The LSTTL/MSI SN54LS/74LS153 is a very high speed Dual 4-Input Multiplexer with common select inputs and individual enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the LS153 can generate any two functions of three variables. The LS153 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- MULTIFUNCTION CAPABILITY
- NON-INVERTING OUTPUTS
- SEPARATE ENABLE FOR EACH MULTIPLEXER
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION **EFFECTS**

SN54LS153 SN74LS153

DUAL 4-INPUT MULTIPLEXER

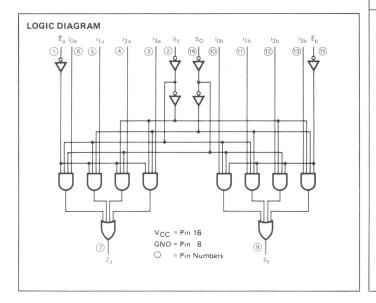
LOW POWER SCHOTTKY

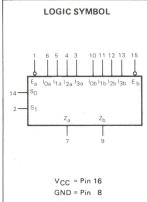
PIN NAMES		LOADIN	G (Note a)
		HIGH	LOW
s_0	Common Select Input	0.5 U.L.	0.25 U.L.
S ₀ E	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
10, 11	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

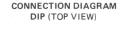
NOTES:

a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.









J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS153 is a Dual 4-Input Multiplexer fabricated with Low Power, Schottky barrier diode process for high speed. It can select two bits of data from up to four sources under the control of the common Select Inputs (S_0 , S_1). The two 4-input multiplexer circuits have individual active LOW Enables (\overline{E}_a , \overline{E}_b) which can be used to strobe the outputs independently. When the Enables (\overline{E}_a , \overline{E}_b) are HIGH, the corresponding outputs (Z_a , Z_b) are forced LOW.

The LS153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below.

$$\begin{split} Z_a &= \overline{\mathsf{E}}_a \cdot (\mathsf{I}_{0a} \cdot \overline{\mathsf{S}}_1 \cdot \overline{\mathsf{S}}_0 + \mathsf{I}_{1a} \cdot \overline{\mathsf{S}}_1 \cdot \mathsf{S}_0 + \mathsf{I}_{2a} \cdot \mathsf{S}_1 \cdot \overline{\mathsf{S}}_0 + \mathsf{I}_{3a} \cdot \mathsf{S}_1 \cdot \mathsf{S}_0) \\ Z_b &= \overline{\mathsf{E}}_b \cdot (\mathsf{I}_{0b} \cdot \overline{\mathsf{S}}_1 \cdot \overline{\mathsf{S}}_0 + \mathsf{I}_{1b} \cdot \overline{\mathsf{S}}_1 \cdot \mathsf{S}_0 + \mathsf{I}_{2b} \cdot \mathsf{S}_1 \cdot \overline{\mathsf{S}}_0 + \mathsf{I}_{3b} \cdot \mathsf{S}_1 \cdot \mathsf{S}_0) \end{split}$$

The LS153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The LS153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT	INPUTS		INPUTS (a or b)							
s ₀	s ₁	Ē	10	11	12	13	Z			
×	X	Н	X	X	×	Х	L			
L	L	L	L	×	×	×	L			
L	L	L	Н	×	×	×	Н			
H	L	L	×	L	×	×	L			
Н	L	L	×	Н	×	×	Н			
L	Н	L	X	×	L	X	L			
L	Н	L	X	×	Н	×	Н			
Н	Н	L	X	×	×	L	L			
Н	Н	L	×	X	×	Н	Н			

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

COMIDATE	or Electrical Database					
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	٧
ТА	Operating Ambient Temperature Range	54 74	-55 O	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

CVMBOL	DADAMETER	PARAMETER		LIMITS		UNITS	TEST	ONDITIONS	
SYMBOL	PARAIVIETER	1	MIN	TYP	MAX	UNITS	1531 0	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
		54			0.7	.,,		ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA		
Voн	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$	
VOH	74		2.7	3.5		V	or V _{IL} per Truth	Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	V _{CC} = MAX, V _I	N = 2.7 V	
IH	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
IIL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V	
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
Icc	Power Supply Current				10	mA	V _{CC} = MAX		

AC CHARACTERISTICS: T_A = 25°C

CVMADOL	DADAMETER		LIMITS			TEGT COMPITIONS		
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS		TEST CONDITIONS	
^t PLH ^t PHL	Propagation Delay Data to Output		10 17	15 26	ns	Fig. 2		
^t PLH ^t PHL	Propagation Delay Select to Output		19 25	29 38	ns	Fig. 1	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$	
^t PLH ^t PHL	Propagation Delay Enable to Output		16 21	24 32	ns	Fig. 2		

AC WAVEFORMS

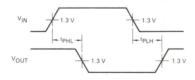


Fig. 1

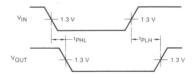


Fig. 2



DESCRIPTION — The SN54LS/74LS155 and SN54LS/74LS156 are high speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The LS155 and LS156 are fabricated with the Schottky barrier diode process for high speed and are completely compatible with all Motorola TTL families.

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- COMMON ADDRESS INPUTS
- TRUE OR COMPLEMENT DATA DEMULTIPLEXING
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION **EFFECTS**

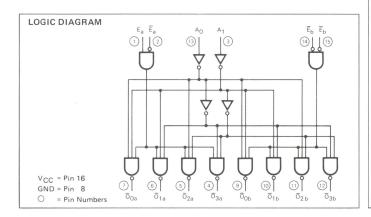
PIN NAMES

		HIGH	LOW
A ₀ , A ₁	Address Inputs	0.5 U.L.	0.25 U.L.
\overline{E}_a , \overline{E}_b	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
Ea	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{\overline{O}}_{0}^{a} - \overline{O}_{3}$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES

a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

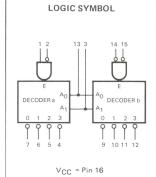
The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The HIGH level drive for the LS156 must be established by an external resistor.



SN54LS/74LS155 SN54LS/74LS156

DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

LS156-OPEN-COLLECTOR LOW POWER SCHOTTKY



GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix - Case 648-05

(Plastic)

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOADING (Note a)

FUNCTIONAL DESCRIPTION — The LS155 and LS156 are Dual 1-of-4 Decoder/Demultiplexers with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A₀, A₁) and provides four mutually exclusive active LOW outputs $(\overline{O}_0 - \overline{O}_3)$. If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input $(E_a \circ \overline{E}_a)$. In demultiplexing applications, Decoder "a" can accept either true or complemented data by using the \overline{E}_a or E_a inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs $(\overline{E}_b \circ \overline{E}_b)$. The LS155 or LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying E_a to \overline{E}_b and relabeling the common connection as (A₂). The other \overline{E}_b and \overline{E}_a are connected together to form the common enable.

The LS155 and LS156 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in Fig. a. The LS156 has the further advantage of being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$\begin{split} & \text{f = (E + A_0 + A_1) \cdot (E + \overline{A}_0 + A_1) \cdot (E + A_0 + \overline{A}_1) \cdot (E + \overline{A}_0 + \overline{A}_1)} \\ & \text{where } E = E_a + \overline{E}_a \\ \vdots & E = E_b + E_b \end{split}$$

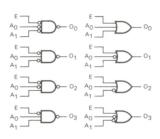


Fig. a

TRUTH TABLE

ADD	RESS	ENAB	LE "a"	OUTPUT "a"		ENAB	LE "b"	OUTPUT "b"					
A ₀	A ₁	Ea	Ēa	ō ₀	\bar{o}_1	\bar{o}_2	ō ₃	Ēb	\overline{E}_b	ō ₀	\bar{o}_1	\bar{o}_2	ō ₃
X	Х	L	Х	Н	Н	Н	Н	Н	X	Н	Н	Н	Н
×	Х	X	Н	Н	Н	Н	Н	X	Н	Н	Н	Н	Н
L	L	Н	L	L	Н	Н	Н	L	L	L	Н	Н	Н
Н	L	Н	L	Н	L	Н	Н	L	L	Н	L	Н	Н
L	Н	Н	L	Н	Н	L	Н	L	L	Н	Н	L	Н
Н	Н	Н	L	Н	Н	Н	L	L	L	Н	Н	Н	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74		1 1 1 1	4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

				LIMITS					
SYMBOL	PARAMETER	R	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
		54			0.7	.,		ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
Voн	Output HIGH Voltage 54 74	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$	
*OH		2.7	3.5		V	or V _{IL} per Truth	Table		
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
IH	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
IL	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_I$	N = 0.4 V	
OS	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$		
cc	Power Supply Current				10	mA	$V_{CC} = MAX$		

AC CHARACTERISTICS $T_{\mbox{\scriptsize A}} = 25^{\circ} \mbox{\scriptsize C}$

SYMBOL	PARAMETER	LIMI	TS MAX	UNITS		TEST CONDITIONS
t _{PLH}	Propagation Delay Address, \overline{E}_a or \overline{E}_b to Output	10 19	15 30	ns	Fig. 1	
t _{PLH}	Propagation Delay Address to Output	17 19	26 30	ns	Fig. 2	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 15 \text{ pF}$
^t PLH ^t PHL	Propagation Delay E _a to Output	18 18	27 27	ns	Fig. 1	

AC WAVEFORMS

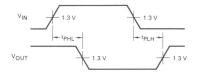


Fig. 1

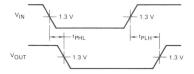


Fig. 2

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
Vон	Output Voltage — High	54,74			5.5	V
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS		
STIVIBUL	PARAMETER		MIN	TYP	MAX	UNITS			
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
		54			0.7	.,	Guaranteed Input LOW Voltage for		
V _{IL}	Input LOW Voltage 74				0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
ГОН	Output HIGH Current	54,74			100	μΑ	$V_{CC} = MIN, V_{OH} = MAX$		
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$v_{CC} = v_{CC} MIN$,	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
lН	Input HIGH Current	Input HIGH Current			0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
l _{IL}	Input LOW Current				-0.4	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$		
lcc	Power Supply Current	*			10	mA	V _{CC} = MAX		

AC CHARACTERISTICS $T_A = 25^{\circ}C$

SYMBOL	PARAMETER	LIMITS		LINUTO	TEGT COMPLETIONS		
STIVIBUL	PARAMETER	TYP	MAX	UNITS	TEST CONDITIONS		
^t PLH ^t PHL	Propagation Delay Address, \bar{E}_a or \bar{E}_b to Output	25 34	40 51	ns	Fig. 1	V _{CC} = 5.0 V	
^t PLH ^t PHL	Propagation Delay Address to Output	31 34	46 51	ns	Fig. 2	$C_L = 15 \text{ pF}$ $R_L = 2 \text{ k}\Omega$	
^t PLH ^t PHL	Propagation Delay E _a to Output	32 32	48 48	ns	Fig. 1	_	

AC WAVEFORMS

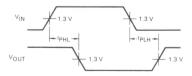


Fig. 1

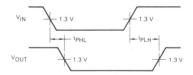


Fig. 2



DESCRIPTION — The LSTTL/MSI SN54LS/74LS157 is a high speed Quad 2-Input Multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The LS157 can also be used to generate any four of the 16 different functions of two variables. The LS157 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- NON-INVERTING OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION FEFFCTS

SN54LS157 SN74LS157

QUAD 2-INPUT MULTIPLEXER

LOW POWER SCHOTTKY

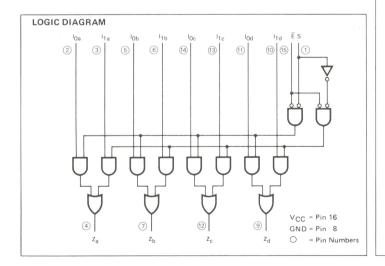
PIN NAMES

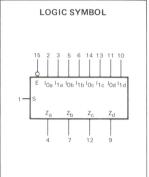
		HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
Ē	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$Z_a - Z_d$	Multiplexer Outputs (Note b)	10 U.L.	5 (2.5) U.L.

LOADING (Note a)

NOTES

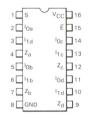
- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.





V_{CC} = Pin 16 GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05

(Plastic)

NOTE

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS157 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S). The Enable Input (\overline{E}) is active LOW. When \overline{E} is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs.

The LS157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$\begin{split} Z_a &= \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \\ Z_c &= \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \end{split} \qquad Z_b &= \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S}) \\ Z_d &= \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S}) \end{split}$$

A common use of the LS157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		ОИТРИТ
Ē	S	10	11	Z
Н	×	×	×	L
L	н	×	L	L
L	Н	×	Н	Н
L	L	L	X	L
L	L	Н	X	н

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

GOANAITIE	D OF LINATING NAMES					
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lor	Output Current — Low	54 74			4.0 8.0	mA

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS			
STIVIBUL	PARAMETER	1	MIN	TYP	MAX	UNITS	TEST C	ONDITIONS		
VIH	Input HIGH Voltage		2.0			٧	Guaranteed Inp All Inputs	Guaranteed Input HIGH Voltage fo All Inputs		
		54			0.7	.,		ut LOW Voltage for		
VIL	Input LOW Voltage	74			0.8	V	All Inputs			
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA			
VoH	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$		
VOH	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth	1 Table		
V _{OL}		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$		
	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table		
lıн	Input HIGH Current IO,I1 E,S				20 40	μΑ	$V_{CC} = MAX, V_{IN} = 2.7 V$			
	I _O ,I ₁ Ē,S				0.1 0.2	mA	V _{CC} = MAX, V _I	N = 7.0 V		
I _{IL}	Input LOW Current IO.I1 E,S				-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V			
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX			
lcc	Power Supply Current	Power Supply Current			16	mA	V _{CC} = MAX			

AC CHARACTERISTICS: T_A = 25°C

CVAADOL	DARAMETER	LIMITS			LINITO	TEST CONDITIONS		
SYMBOL	PARAMETER	MIN	TYP MAX UNITS			TEST CONDITIONS		
t _{PLH} t _{PHL}	Propagation Delay Data to Output		9.0 9.0	14 14	ns	Fig. 2		
^t PLH ^t PHL	Propagation Delay Enable to Output		13 14	20 21	ns	Fig. 1	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 15 \text{ pF}$	
^t PLH ^t PHL	Propagation Delay Select to Output		15 18	23 27	ns	Fig. 2		

AC WAVEFORMS

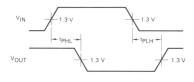


Fig. 1

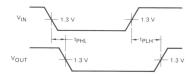


Fig. 2



DESCRIPTION — The LSTTL/MSI SN54LS/74LS158 is a high speed Quad 2-Input Multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The LS158 can also generate any four of the 16 different functions of two variables. The LS158 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- INVERTED OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

SN54LS158 SN74LS158

QUAD 2-INPUT MULTIPLEXER

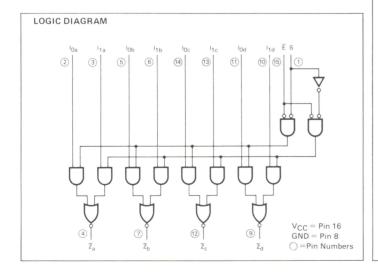
LOW POWER SCHOTTKY

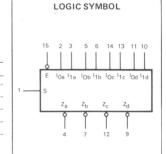
PIN NA	MAEC

		HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
E	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
<u>l</u> 1a - <u>l</u> 1d	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$\overline{Z}_a - \overline{Z}_d$	Inverted Outputs (Note b)	10 U.L.	5 (2.5) U.L.

LOADING (Note a)

- NOTES: a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.





V_{CC} = Pin 16 GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

NOTE

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS158 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S) and presents the data in inverted form at the four outputs. The Enable Input (\overline{E}) is active LOW. When \overline{E} is HIGH, all of the outputs (\overline{Z}) are forced HIGH regardless of all other inputs.

The LS158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input.

A common use of the LS158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE

ENABLE	SELECT INPUT	INP	UTS	OUTPUT							
Ē	S	10	11	Z							
Н	X	X	Х	Н							
L	L	L	X	Н							
L	L	Н	×	L							
L	Н	X	L	Н							
L	Н	×	Н	L							

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

CVMAROL	DARAMETER		LIMITS			UNITS	TEST CONDITIONS		
SYMBOL	PARAMETER	1	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0		×	V	Guaranteed Input HIGH Voltage f All Inputs		
		54			0.7			put LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
√он	Output HIGH Voltage	54	2.5	3.5		V		$_{OH} = MAX, V_{IN} = V_{IH}$	
VOH	Output High voltage	74	2.7	3.5		V	or V _{IL} per Truth Table		
V _{OL}	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN$,	
		74		0.35	0.5	V	I _{OL} = 8.0 mA V _{CC} = V _{CC} in V _{IN} = V _{IL} or V _I per Truth Table		
IH	Input HIGH Current IO,I1 E,S				20 40	μΑ	V _{CC} = MAX, V	′ _{IN} = 2.7 V	
	1 ₀ ,1 ₁ Ē,S				0.1	mA	V _{CC} = MAX, V	′ _{IN} = 7.0 V	
IL	Input LOW Current IO.I1 E.S				-0.4 -0.8	mA	V _{CC} = MAX, V	′ _{IN} = 0.4 ∨	
os	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$		
СС	Power Supply Current				8.0	mA	V _{CC} = MAX		

AC CHARACTERISTICS: $T_A = 25^{\circ}C$

SYMBOL	PARAMETER	LIMITS		LINITO	TEST COMPITIONS			
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
^t PLH ^t PHL	Propagation Delay Data to Output		7.0 10	12 15	ns	Fig. 2		
t _{PLH} t _{PHL}	Propagation Delay Enable to Output		11 18	17 24	ns -	Fig. 1	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$	
tPLH tPHL	Propagation Delay Select to Output		13 16	20 24	ns	Fig. 2		

AC WAVEFORMS

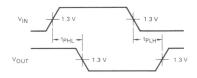


Fig. 1

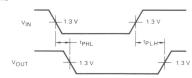


Fig. 2



DESCRIPTION — The LS160A/161A/162A/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The LS160A and LS162A count modulo 10 (BCD). The LS161A and LS163A count modulo 16 (binary.)

The LS160A and LS161A have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS162A and LS163A have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	BCD (Modulo 10)	Binary (Modulo 16)
Asynchronous Reset	LS160A	LS161A
Synchronous Reset	LS162A	LS163A

- SYNCHRONOUS COUNTING AND LOADING
- TWO COUNT ENABLE INPUTS FOR HIGH SPEED SYNCHRONOUS EXPANSION
- TERMINAL COUNT FULLY DECODED
- EDGE-TRIGGERED OPERATION
- TYPICAL COUNT RATE OF 35 MHz

LOADING (Note a)

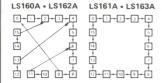
PIN NAN	IES	HIGH	LOW
PE	Parallel Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
Po-P3	Parallel Inputs	0.5 U.L.	0.25 U.L.
CEP	Count Enable Parallel Input	0.5 U.L.	0.25 U.L.
CET	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
SR	Synchronous Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
00-03	Parallel Outputs (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:

PIN NAMES

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges

STATE DIAGRAM



LOGIC EQUATIONS

Count Enable = CEP • CET • PE TC for LS160A & LS162A = CET \circ Q₀ \circ $\overline{Q_1}$ \circ $\overline{Q_2}$ \circ Q₃ TC for LS161A & LS163A = CET • Q₀ • Q₁ • Q₂ • Q₃ Preset = PE • CP + (rising clock edge) Reset = MR (LS160A & LS161A)

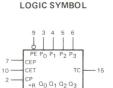
Reset = SR • CP + (rising clock edge) (LS162A & LS163A)

The LS160A and LS162A can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses

SN54LS/74LS160A SN54LS/74LS161A SN54LS/74LS162A SN54LS/74LS163A

BCD DECADE COUNTERS/ 4-BIT BINARY COUNTERS

LOW POWER SCHOTTKY



V_{CC} = Pin 16 GND = Pin 8

1 14 13 12 11

*MR for LS160A and LS161A *SR for LS162A and LS163A

CONNECTION DIAGRAMS DIP (TOP VIEW)



*MR for LS160A and LS161A *SR for LS162A and LS163A

J Suffix — Case 620-08 (Ceramic) N Suffix - Case 648-05 (Plastic)

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS160A/161A/162A/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. These counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS160A and LS161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs — Parallel Enable (\overline{PE}) , Count Enable Parallel (CEP) and Count Enable Trickle (CET) — select the mode of operation as shown in the tables below. The Count Mode is enabled when the CEP, CET, and \overline{PE} inputs are HIGH. When the \overline{PE} is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit the count sequence. With the \overline{PE} held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET•CEP) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

The LS160A and LS162A count modulo 10 following a binary coded decimal (BCD) sequence. They generate a TC output when the CET input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do not generate a TC output.

The LS161A and LS163A count modulo 16 following a binary sequence. They generate a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset (\overline{MR}) of the LS160A and LS161A is asynchronous. When the \overline{MR} is LOW, it overrides all other input conditions and sets the outputs LOW. The \overline{MR} pin should never be left open. If not used, the \overline{MR} pin should be tied through a resistor to VCC, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset $\overline{(SR)}$ input of the LS162A and LS163A acts as an edge-triggered control input, overriding CET, CEP and \overline{PE} , and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*SR	PE	CET	CEP	Action on the Rising Clock Edge (🖵)		
L	X	×	×	RESET (Clear)		
н	L	×	×	$LOAD (P_n \rightarrow Q_n)$		
Н	Н	Н	н	COUNT (Increment)		
Н	Н	L	×	NO CHANGE (Hold)		
Н	Н	X	L	NO CHANGE (Hold)		

*For the LS162A and LS163A only.

X = Don't Care

H = HIGH Voltage Level L = LOW Voltage Level

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
IOL Output Current — Low		54 74			4.0 8.0	mA

SYMBOL	PARAMETER		LIMITS			LINUTC	TEST CONDITIONS	
STIMBUL	PARAMETER	1	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
V _{IL}		54			0.7		Guaranteed Inp	ut LOW Voltage for
	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA	
Voн	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$
·Un	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
V _{OL}	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN$,
		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	VIN = VIL or VIH per Truth Table
I _I H	Input HIGH Current MR, Data, CEP, Cloc PE, CET			20 40	μΑ	V _{CC} = MAX, V _I	N = 2.7 V	
	MR, Data, CEP, Clock PE, CET			0.1 0.2	mA	V _{CC} = MAX, V _I	N = 7.0 V	
ΊL	Input LOW Current MR, Data, CEP, Cloc PE, CET			-0.4 -0.8	mA	V _{CC} = MAX, V _I	N = 0.4 V	
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
Icc	Power Supply Current Total, Output HIGH Total, Output LOW			31 32	mA	V _{CC} = MAX		

CVAAROL	BARAMETER		LIMITS			UNITS	TEST CONDITIONS	
SYMBOL	PARAMETER	(MIN	TYP	MAX	UNITS	TEST	CNDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
V _{IL}		54			0.7	.,		ut LOW Voltage for
	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA	
Voh	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OI}	$H = MAX, V_{IN} = V_{IH}$
• ОН	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
VOL	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN$
		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
Iн	Input HIGH Current Data, CEP, Clock PE, CET, SR				20 40	μΑ	$V_{CC} = MAX, V_{IN} = 2.7 \text{ V}$ $V_{CC} = MAX, V_{IN} = 7.0 \text{ V}$	
	Data, CEP, Clock PE, CET, SR			,	0.1 0.2	mA		
IIL	Input LOW Current Data, CEP, Clock PE, CET, SR				-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
lcc	Power Supply Current Total, Output HIGH Total, Output LOW				31 32	mA	V _{CC} = MAX	

AC CHARACTERISTICS: TA = 25°C

SYMBOL	DARAMETER	LIMITS			UNITS	TEST CONDITIONS	
	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
fMAX	Maximum Clock Frequency	25	32		MHz		
^t PLH ^t PHL	Propagation Delay Clock to TC		20 18	35 35	ns		
^t PLH ^t PHL	Propagation Delay Clock to Q		13 18	24 27	ns	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 15 \text{ pF}$	
^t PLH ^t PHL	Propagation Delay CET to TC		9.0 9.0	14 14	ns		
^t PHL	MR or SR to Q		20	28	ns		

AC SETUP REQUIREMENTS: TA = 25°C

SYMBOL	DADAMETED		LIMITS		UNITS	TEST CONDITIONS		
	PARAMETER	MIN	TYP	MAX	UNITS			
t _W CP	Clock Pulse Width Low	25			ns			
tW	MR or SR Pulse Width	20			ns	$V_{CC} = 5.0 \text{ V}$		
t _s	Setup Time, other*	20			ns	VCC = 5.0 V		
s	Setup Time PE or SR	25			ns			
t _h	Hold Time, Any Input	0			ns			

^{*}CEP, CET or DATA

DEFINITION OF TERMS:

SETUP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY, AND CLOCK PULSE WIDTH.

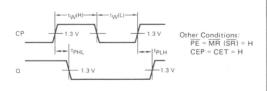
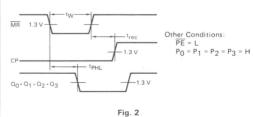


Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME.



AC WAVEFORMS (Cont'd)

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

The positive TC pulse occurs when the outputs are in the $(Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3)$ state for the LS160 and LS162 and the $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$ state for the LS161 and LS163.

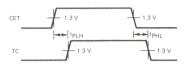


Fig. 3

Other Conditions: $CP = \overline{PE} = CEP = \overline{MR} = H$

CLOCK TO TERMINAL COUNT DELAYS.

The positive TC pulse is coincident with the output state ($Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3$) for the LS161 and LS163 and ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) for the LS161 and LS163.

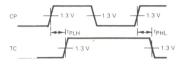


Fig. 4

Other Conditions: $\overline{PE} = CEP = CET = \overline{MR} = H$

SETUP TIME (t_s) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

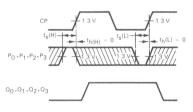


Fig. 5

Other Conditions: $\overline{PE} = L$, $\overline{MR} = H$

SETUP TIME (t_s) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE (\overline{PE}) INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

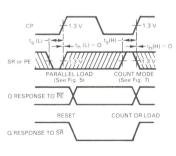


Fig. 6

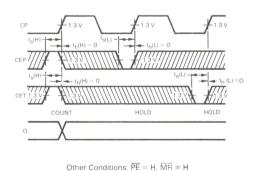


Fig. 7



DESCRIPTION — The SN54LS/74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

SN54LS164 SN74LS164

SERIAL-IN PARALLEL-OUT SHIFT REGISTER

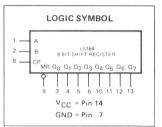
LOW POWER SCHOTTKY

- TYPICAL SHIFT FREQUENCY OF 35 MHz
- ASYNCHRONOUS MASTER RESET
- GATED SERIAL DATA INPUT
- FULLY SYNCHRONOUS DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

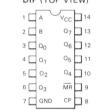
PIN NAMES		LOADING (Note a)				
		HIGH	LOW			
A, B	Data Inputs	0.5 U.L.	0.25 U.L.			
CP	Clock (Active HIGH Going	0.5 U.L.	0.25 U.L.			
	Edge) Input					
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.			
$Q_0 - Q_7$	Outputs (Note b)	10 U.L.	5(2.5) U.L.			

NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.



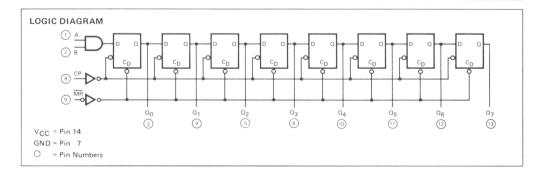
CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

NOTE:

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



FUNCTIONAL DESCRIPTION — The LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A•B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{\text{MR}}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

MODE SELECT - TRUTH TABLE

OPERATING		INPUTS	OUTPUTS		
MODE	MR	А	В	α ₀	$Q_1 - Q_7$
Reset (Clear)	L	×	X	L	L – L
	Н	1	ı	L	q ₀ – q ₆
Shift	Н	1	h	L	q ₀ – q ₆
Silit	Н	h	1	L,	q ₀ – q ₆
	Н	h	h	Н	q ₀ – q ₆

L (I) = LOW Voltage Levels

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

H (h) = HIGH Voltage Levels

X = Don't Care

q_n = Lower case letters indicate the state of the referenced input or output one set-up time prior to the LOW to HIGH clock transition.

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS		
STIVIBUL	PARAIVIETER	FARAIVIETER			MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
VIL		54			0.7	.,		ut LOW Voltage for	
	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
Vон	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN$, $I_{OH} = MAX$, $V_{IN} = V_{I}$		
		74	2.7	3.5		V	or V _{IL} per Truth	Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA V _{IN} = V _{IL} or V per Truth Table		
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V	
IH	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V	
İIL	Input LOW Current	Input LOW Current			-0.4	mA	$V_{CC} = MAX, V_I$	V _{CC} = MAX, V _{IN} = 0.4 V	
os	Short Circuit Current	Short Circuit Current			-100	mA	V _{CC} = MAX		
lcc	Power Supply Current			27	mA	$V_{CC} = MAX$			

AC CHARACTERISTICS: $T_A = 25$ °C

SYMBOL	DADAMETER		LIMITS		UNITS	TEST CONDITIONS	
	PARAMETER	MIN	TYP	MAX	UNITS		
fMAX	Maximum Clock Frequency	25	36		MHz		
^t PHL	Propagation Delay MR to Output Q		24	36	ns	$V_{CC} = 5 V$ $C_L = 15 pF$	
tPLH tPHL	Propagation Delay Clock to Output Q		17 21	27 32	ns		

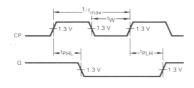
AC SETUP REQUIREMENTS: TA = 25°C

SYMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS	
	PARAMETER	MIN	TYP	MAX	UNITS		
tw	CP, MR Pulse Width	20			ns		
t _S	Data Setup Time	15			ns	$V_{CC} = 5 V$	
th	Data Hold Time				ns		

AC WAVEFORMS

*The shaded areas indicate when the input is permitted to change for predictable output performance.

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



CONDITIONS: $\overline{MR} = H$

Fig. 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

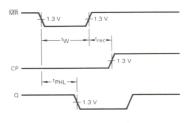


Fig. 2

DATA SETUP AND HOLD TIMES

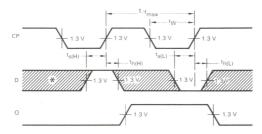


Fig. 3



DESCRIPTION — The SN54LS/74LS165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputing occurs asynchronously when the Parallel Load (PL) input is LOW. With PL HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (DS) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

SN54LS165 SN74LS165

8-BIT PARALIFI-TO-SERIAL CONVERTER

LOW POWER SCHOTTKY

PIN NAMES

CP₁, CP₂ Clock (LOW-to-HIGH Going Edge) Inputs 0.5 U.L. 0.25 U.L. Serial Data Input 0.5 U.L. 0.25 U.L. Asynchronous Parallel Load (Active LOW) 1.5 U.L. 0.75 U.L. Input Parallel Data Inputs

Q, Serial Output from Last State (Note b) Complementary Output (Note b)

HIGH LOW 0.5 U.L 0.25 U.L. 10 U.L. 5 (2.5) U.L.

5 (2.5) U.L.

10 U.L.

LOADING (Note a)

NOTES

DS

PL

Po-P

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges

TRUTH TABLE

PL	_ CP CONTENTS								CP		CONTENTS								RESPONSE
PL	1	2	Qo	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q,	RESPONSE								
L H H H	X L H \	× \ \ \ L	Po Ds Qo Ds	P ₁ Q ₀ Q ₁ Q ₀	P ₂ Q ₁ Q ₂ Q ₁ Q ₂	P ₃ Q ₂ Q ₃ Q ₂ Q ₃	P ₄ Q ₃ Q ₄ Q ₃ Q ₄	P ₅ Q ₄ Q ₅ Q ₄ Q ₅	P ₆ Q ₅ Q ₆ Q ₅ Q ₆	P ₇ Q ₆ Q ₇ Q ₆ Q ₇	Parallel Entry Right Shift No Change Right Shift No Change								

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

PoP1P2P3P4P5P6 Q-V_{CC} = Pin 16 GND = Pin 8 CONNECTION DIAGRAM DIP (TOP VIEW) 16 Vcc CP₁ 2 15 CP₂ P4 1 3 P₃ 14 13 P₂

LOGIC SYMBOL

11121314 3 4 5 6

GND 9 J Suffix — Case 620-08 (Ceramic) N Suffix - Case 648-05 (Plastic)

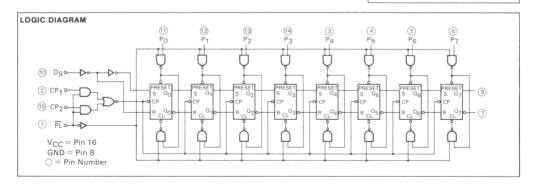
12 P1 Po

10 DS

P₆ 5

P7 6 Q7 07

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



FUNCTIONAL DESCRIPTION — The SN54LS/74LS165 contains eight clocked master/slave RS flip-flops connected as a shift register, with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the $\overline{\text{PL}}$ signal is LOW. The parallel data can change while $\overline{\text{PL}}$ is LOW, provided that the recommended setup and hold times are observed.

For clock operation, PL must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

SYMBOL	PARAMETER			LIMITS		UNITS	TECT	ST CONDITIONS	
STIVIBUL	PARAIVIETER	FANAIVIETEN		TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
		54			0.7		Guaranteed Inp	ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA	
Voн	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$	
VOH	Output mon voltage	74	2.7	3.5		V	or V _{IL} per Truth Table		
		54,74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN		
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
I _{IH}	Input HIGH Current Other Inputs PL Input				20 60	μΑ	V _{CC} = MAX, V _{IN} = 2.7 V		
	Other Inputs PL Input				0.1 0.3	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$		
I _{IL}	Input LOW Current Other Inputs PL Input				-0.4 -1.2	mA	V _{CC} = MAX, V _{IN} = 0.4 V		
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current				36	mA	V _{CC} = MAX		

AC CHARACTERISTICS: TA = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TECT CONDITIONS	
	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
fMAX	Maximum Input Clock Frequency	25	35		MHz		
^t PLH ^t PHL	Propagation Delay PL to Output		22 22	35 35	ns		
^t PLH ^t PHL	Propagation Delay Clock to Output		27 28	40 40	ns	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 15 \text{ pF}$	
t _{PLH}	Propagation Delay P7 to Q7		14 21	25 30	ns	3 <u>L</u> = 13 μι	
t _{PLH}	Propagation Delay P_7 to \overline{Q}_7		21 16	30 25	ns		

AC SETUP REQUIREMENTS: $T_{\Delta} = 25^{\circ}C$

CVMBOL	DADAMETER		LIMITS			TEST CONDITIONS
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
tw	CP Clock Pulse Width	25			ns	
t₩	PL Pulse Width	15			ns	
t _S	Parallel Data Setup Time	10			ns	
ts	Serial Data Setup Time	20			ns	V _{CC} = 5.0 V
t _S	CP ₁ to CP ₂ Setup Time ¹	30			ns	
th	Hold Time	0			ns	
t _{rec}	Recovery Time, PL to CP	45			ns	

① The role of CP₁, and CP₂ in an application may be interchanged

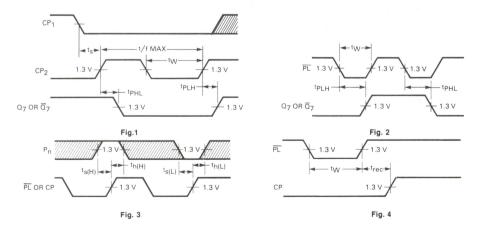
DEFINITION OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

 $HOLD\ TIME\ (t_h)$ — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative hold time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec})—is defined as the minimum time required between the end of the \overline{PL} pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer loaded Data to the Q outputs.

AC WAVEFORMS





DESCRIPTION — The SN54LS/74LS166 is an 8-Bit Shift Register. Designed with all inputs buffered, the drive requirements are lowered to one 54LS/74LS standard load. By utilizing input clamping diodes, switching transients are minimized and system design simplified.

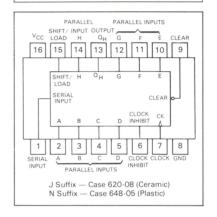
The LS166 is a parallel-in or serial-in, serial-out shift register and has a complexity of 77 equivalent gates with gated clock inputs and an overriding clear input. The shift/load input establishes the parallel-in or serial-in mode. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. Synchronous loading occurs on the next clock pulse when this is low and the parallel data inputs are enabled. Serial data flow is inhibited during parallel loading. Clocking is done on the low-to-high level edge of the clock pulse via a two input positive NOR gate, which permits one input to be used as a clock enable or clock inhibit function. Clocking is inhibited when either of the clock inputs are held high, holding either input low enables the other clock input. This will allow the system clock to be free running and the register stopped on command with the other clock input. A change from low-to-high on the clock inhibit input should only be done when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero

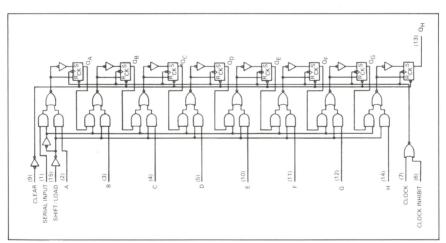
- SYNCHRONOUS LOAD
- DIRECT OVERRIDING CLEAR
- PARALLEL TO SERIAL CONVERSION

SN54LS166 SN74LS166

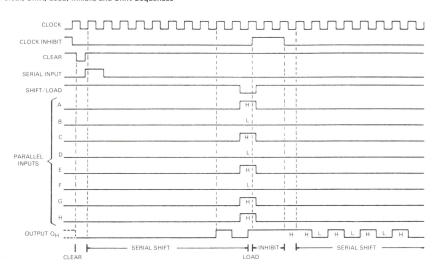
8-BIT SHIFT REGISTERS

LOW POWER SCHOTTKY





Typical Clear, Shift, Load, Inhibit, and Shift Sequences



FUNCTION TABLE

	INPUTS							OUTPUT						
CLEAR	SHIFT/	CLOCK	СГОСК	LOCK SERIAL PA		CLOCK SERIAL F		CLOCK SERIAL P		CLOCK SERIAL PARALLEL		OUTPUTS		QH
OLLANI	LOAD	INHIBIT	OLOOK	OLITIAL	A H	QΑ	QΒ	ФH						
L	X	X	X	X	X	L	L	L						
Н	X	L	L	X	X	Q_{AO}	Q_{BO}	QHO						
Н	L	L	1	X	ah	а	b	h						
Н	Н	L	Ť	Н	X	Н	Q_{An}	QGn						
Н	Н	L	t	L	X	L	Q_{An}	QGn						
Н	X	Н	t	X	X	Q _{AO}	QBO	QHO						

GUARANTEED OPERATING RANGES

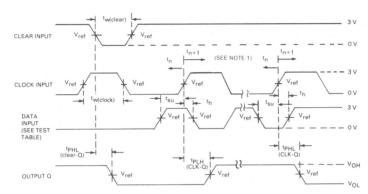
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

SYMBOL	DL PARAMETER			LIMITS		LIMITO	TECT	CONDITIONS	
STIVIBUL			MIN	TYP	MAX	UNITS	TEST	CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
		54			0.7			put LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Voltag	ge		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
Vон	Output HIGH Voltage	54	2.5	3.5		V		$_{DH} = MAX, V_{IN} = V_{IH}$	
VOH	Output man voltage	74	2.7	3.5		V	or V _{IL} per Trut	or V _{IL} per Truth Table	
		54,74		0.25	0.4	V		$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	V _{CC} = MAX, V	$I_{1N} = 2.7 \text{ V}$	
lн	Input HIGH Current				0.1	mA	V _{CC} = MAX, V	$v_{1N} = 7.0 \text{ V}$	
ΊL	Input LOW Current				-0.4	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$		
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current				38	mA	$V_{CC} = MAX$		

AC WAVEFORMS

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED
Н	0 V	Q _H at t _{n+1}
Serial Input	4.5 V	Q _H at t _{n+8}



Note 1. $t_n=$ bit time before clocking transition $t_{n+1}=$ bit time after one clocking transition $t_{n+8}=$ bit time after eight clocking transitions LS166 $V_{ref}=1.3~V_c$

AC CHARACTERISTICS: $T_A = 25 \, ^{\circ} C$

	, ,					
SYMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
fMAX	Maximum Clock Frequency	25	35		MHz	
tPHL	Clear to Output		19	30	ns	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 15 \text{ pF}$
^t PLH ^t PHL	Clock to Output		23 24	35 35	ns	CL = 13 βF

AC SETUP REQUIREMENTS: $T_A = 25^{\circ}C$

SYMBOL	PARAMETER		LIMITS		LINITO	TEST CONDITIONS
	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
tw	Clock Clear Pulse Width	30			ns	
t _S	Mode Control Setup Time	30			ns	$V_{CC} = 5.0 \text{ V}$
t _S	Data Setup Time	20			ns	
th	Hold Time, Any Input	15		_	ns	



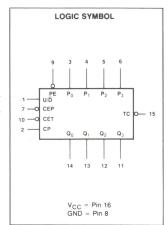
DESCRIPTION — The SN54LS/74LS168A and SN54LS/74LS169A are fully synchronous 4-stage up/down counters featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/\bar{D} input to control the direction of counting. The SN54LS/74LS168A counts in a BCD decade (8, 4, 2, 1) sequence, while the SN54LS/74LS169A operates in a Modulo 16 binary sequence. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

- LOW POWER DISSIPATION 100 mW TYPICAL
- HIGH-SPEED COUNT FREQUENCY 30 MHz TYPICAL
- FULLY SYNCHRONOUS OPERATION
- FULL CARRY LOOKAHEAD FOR EASY CASCADING
- SINGLE UP/DOWN CONTROL INPUT POSITIVE EDGE-TRIGGER OPERATION
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION **FFFFCTS**

SN54LS/74LS168A SN54LS/74LS169A

BCD DECADE/MODULO **16 BINARY SYNCHRONOUS** BI-DIRECTIONAL COUNTERS

LOW POWER SCHOTTKY



CONNECTION DIAGRAM DIP (TOP VIEW)

1 U/D	V _{cc}	16
2 CP	TC	15
3 🔲 P ₀	Q ₀	14
4 🗌 P ₁	Q ₁	13
5 P ₂	Q ₂	12
6 P ₃	Q_3	11
7 CEP	CET	10
8 GND	PE	9
° L GIND	FE	H ³

J Suffix — Case 620-08 (Ceramic) N Suffix - Case 648-05 (Plastic)

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package

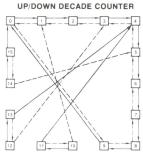
PIN NAMES

		HIGH	LOW
CEP	Count Enable Parallel (Active LOW) Input	0.5 U.L.	0.25 U.L.
CET	Count Enable Trickle (Active LOW) Input	1.0 U.L.	0.5 U.L.
CP PE	Clock Pulse (Active positive going edge) Input	0.5 U.L.	0.25 U.L.
PE	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
U/D	Up-Down Count Control Input	0.5 U.L.	0.25 U.L.
P ₀ -P ₃	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
$\frac{Q_0}{TC}$	Flip-Flop Outputs	10 U.L.	5 (2.5) U.L.
TC	Terminal Count (Active LOW) Output	10 U.L.	5 (2.5) U.L.

NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

STATE DIAGRAMS



SN54LS/74LS168A

SN54LS/74LS168A

UP: $TC = Q_0 \cdot Q_3 \cdot (U/\overline{D})$ DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (\overline{U/\overline{D}})$



- Count Up - - Count Down

10

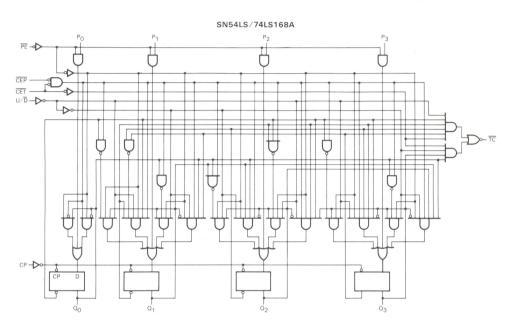
SN54LS/74LS169A

LOADING (Note a)

SN54LS/74LS169A

 $\begin{array}{ll} \text{UP:} & \text{TC} = \underline{Q_0} \bullet \underline{Q_1} \bullet \underline{Q_2} \bullet \underline{Q_3} \bullet (\underline{U/\overline{D}}) \\ \text{DOWN:} & \text{TC} = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet (\overline{U/\overline{D}}) \end{array}$

LOGIC DIAGRAMS



SN54LS/74LS169A PE OP OF CEP
GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

CVMBOL	DADAMETED		LIMITS			UNITS	TEST	ONDITIONS
SYMBOL	PARAMETER	{	MIN	TYP	MAX	UNITS	TEST	ONDITIONS
⁄ін	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
		54			0.7			ut LOW Voltage for
/IL	Input LOW Voltage	74			0.8	V	All Inputs	
/IK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA
′он	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN}$	
*OH	output man voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	Table
V _{OL}	Output LOW Voltage	54,74		0.25	0.4	٧ .	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
		74		0.35	0.5	V		VIN = VIL or VIH per Truth Table
IH.	Input HIGH Current Other Inputs CET Input				20 40	μΑ	V _{CC} = MAX, V _I	_N = 2.7 V
	Other Input CET Input			0.1 0.2	mA	V _{CC} = MAX, V _I	N = 7.0 V	
IL	Input LOW Current Other Input CET Input				-0.4 -0.8	mA	V _{CC} = MAX, V _I	N = 0.4 V
OS	Short Circuit Current		-20		-100	mA	V _{CC} = MAX	
CC	Power Supply Current				34	mA	V _{CC} = MAX	

FUNCTIONAL DESCRIPTION — The SN54LS/74LS168A and SN54LS/74LS169A use edge-triggered D-type flip-flops and that have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the clock and remain valid for the recommended hold time thereafter.

The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When \overline{PE} is LOW, the data on the Po-P3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both \overline{CEP} and \overline{CET} must be LOW and \overline{PE} must be HIGH. The U/\overline{D} input then determines the direction of counting.

The Terminal Count (\overline{TC}) output is normally HIGH and goes LOW, provided that \overline{CET} is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 15 (9 for the SN54LS/74LS168A) in the COUNT UP mode. The \overline{TC} output state is not a function of the Count Enable Parallel (\overline{CEP}) input level. The \overline{TC} output of the SN54LS/74LS168A decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the SN54LS/74LS168A will return to the legitimate sequence within two counts. Since the \overline{TC} signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on \overline{TC} . For this reason the use of \overline{TC} as a clock signal is not recommended.

MODE SELECT TABLE

PE	CEP	CET	U/D	Action on Rising Clock Edge						
L	X	X	X	Load (Pn-Qn)						
Н	L	L	Н	Count Up (increment)						
Н	L	L	L	Count Down (decrement)						
Н	Н	X	X	No Change (Hold)						
Н	X	Н	X	No Change (Hold)						

H = HIGH Voltage Level

L = LOW Voltage Level

X = immaterial

AC CHARACTERISTICS: $T_{\Delta} = 25^{\circ}C$, $V_{CC} = 5.0 \text{ V}$

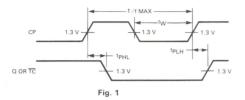
SYMBOL	PARAMETER		LIMITS			TECT COMPITIONS		
STIVIBUL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
fMAX	Maximum Clock Frequency	25	32		MHz			
^t PLH ^t PHL	Propagation Delay, Clock to TC		23 23	35 35	ns			
^t PLH ^t PHL	Propagation Delay, Clock to any Q		13 15	20 23	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$		
^t PLH ^t PHL	Propagation Delay, CET to TC		15 15	20 20	ns			
^t PLH ^t PHL	Propagation Delay, U/D to TC		17 19	25 29	ns			

AC SETUP REQUIREMENTS: $T_A = 25$ °C,

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
STIMBUL		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
tw	Clock Pulse Width	25			ns		
t _S	Setup Time, Data or Enable	20			ns		
t _S	Setup Time PE	25			ns	V _{CC} = 5.0 V	
t _S	Setup Time U/D	30			ns		
th	Hold Time Any Input	0			ns		

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY, AND CLOCK PULSE WIDTH.



CLOCK TO TERMINAL DELAYS

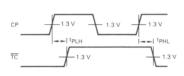
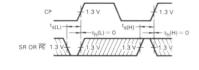
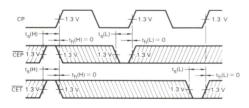


Fig. 3

SETUP TIME AND HOLD TIME FOR COUNT ENABLE AND PARALLEL ENABLE INPUTS, AND UP-DOWN CONTROL INPUTS

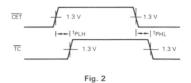




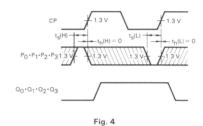
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 5

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS



SETUP TIME (t_S) AND HOLD (t_h) FOR PARALLEL DATA INPUTS.



UP-DOWN INPUT TO TERMINAL COUNT OUTPUT DELAYS

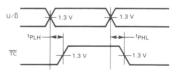


Fig. 6



DESCRIPTION — The TTL/MSI SN54LS/74LS170 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The SN54LS/74LS670 provides a similar function to this device but it features 3-state outputs.

- SIMULTANEOUS READ/WRITE OPERATION
- EXPANDABLE TO 512 WORDS OF n-BITS
- TYPICAL ACCESS TIME OF 20 ns
- LOW LEAKAGE OPEN-COLLECTOR OUTPUTS FOR EXPANSION
- TYPICAL POWER DISSIPATION OF 125 mW

PIN NAMES

		HIGH	LOW
D ₁ -D ₄	Data Inputs	0.5 U.L.	0.25 U.L.
WA, WB	Write Address Inputs	0.5 U.L.	0.25 U.L.
Ēw	Write Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
RA, RB	Read Address Inputs	0.5 U.L.	0.25 U.L.
ĒR	Read Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
Q ₁ -Q ₄	Outputs (Note b)	Open-Collector	5(2.5)U.L.

NOTES:

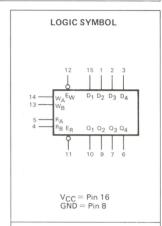
a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW

b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5.0 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive must be supplied by an external resistor to V_{CC}.

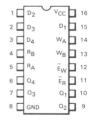
SN54LS170 SN74LS170

4 x 4 REGISTER FILE OPEN-COLLECTOR

LOW POWER SCHOTTKY



CONNECTION DIAGRAM DIP (TOP VIEW)



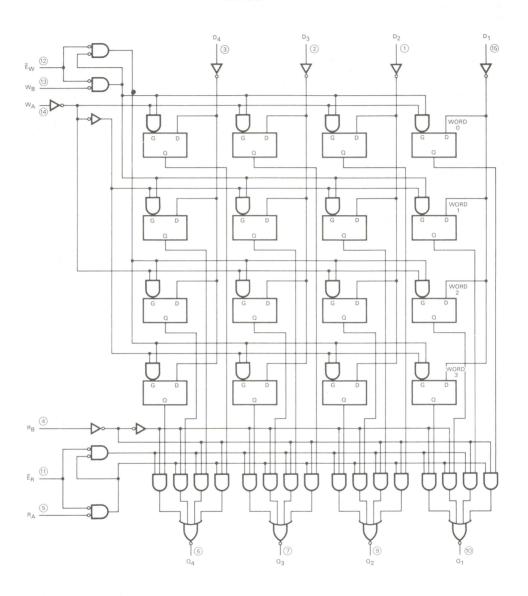
J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

NOTE

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOADING (Note a)

LOGIC DIAGRAM



V_{CC} = Pin 16 GND = Pin 8 ○=Pin Numbers

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WR	ITE INPL	JTS	WORD							
WB	WA	ĒW	0	1	2	3				
L	L	L	Q = D	00	00	00				
L	Н	L	α ₀	Q = D	00	a_0				
Н	L	L	α ₀	00	Q = D	Q_0				
Н	Н	L	α ₀	Q_0	Q_0	Q = D				
X	X	Н	α ₀	α_0	a_0	Q_0				

READ FUNCTION TABLE (SEE NOTES A AND D)

RE	READ INPUTS			OUTPUTS					
RB	RA	ĒR	Q1	Q2	Q3	Q4			
L	L	L	W0B1	W0B2	W0B3	W0B4			
L	Н	L	W1B1	W1B2	W1B3	W1B4			
Н	L	L	W2B1	W2B2	W2B3	W2B4			
Н	н	L	W3B1	W3B2	W3B3	W3B4			
×	×	Н	н	Н	Н	Н			

- NOTES: A. H = high level. L = low level, X = irreleveant.

 B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

 C. Q₀ = the level of Q before the indicated input conditions were established.

 D. WOB1 = The first bit of word 0, etc.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
Тд	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
VOH	Output Voltage — High	54,74			5.5	V
lOL	Output Current — Low	54 74			4.0 8.0	mA

CVMAROL	PARAMETER			LIMITS		LINITO	TECT	CONDITIONS
SYMBOL	PARAMETER	PANAMETER		TYP	MAX	UNITS	IESI	CONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage f	
		54			0.7	V		put LOW Voltage for
VIL	Input LOW Voltage	74			0.8		All Inputs	
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
IOH	Output High Current	54,74			100	μΑ	$V_{CC} = MIN, V_{OH} = MAX$	
V _{OL}	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC}MIN,$
		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
l	Input HIGH Current Any D, R, W E _R , E _W				20 40	μΑ	V _{CC} = MAX, \	/ _{IN} = 2.4 V
liH .	Any D, R, W E _R , E _W				0.1 0.2	mA	V _{CC} = MAX, \	/ _{IN} = 7.0 V
	Input LOW Current							
IIL	Any D, R, W E _R , E _W				-0.4 -0.8	mA	V _{CC} = MAX, \	/IN = 0.4 V
lcc	Power Supply Current				40	mA	V _{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25$ °C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
tPLH tPHL	Propagation Delay, Negative- Going ER to Q Outputs		20 20	30 30	ns	Fig. 1	
^t PLH ^t PHL	Propagation Delay, R _A or R _B to Q Outputs		25 24	40 40	ns	Fig. 2	$V_{CC} = 5 V$ $C_L = 15 pF$ $R_L = 2 k\Omega$
^t PLH ^t PHL	Propagation Delay, Negative- Going E _W to Q Outputs		30 26	45 40	ns	Fig. 1	n 2 Ki2
[†] PLH [†] PHL	Propagation Delay, Data Inputs to Q Outputs		30 22	45 35	ns	Fig. 1	

AC SETUP REQUIREMENTS: TA = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS		
STIVIBUL	FARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
t₩	Pulse Width, ER, EW	25			ns			
t _S	Setup Time, Data to \overline{E}_W	10			ns			
t _S	Setup Time, WA, WB to EW	15			ns	$V_{CC} = 5 V$ $R_L = 2 k\Omega$		
th	Hold Time, Data to E _W	15			ns			
th	Hold Time, W _A , W _B to E _W	5.0			ns			
^t LATCH	Latch Time	25			ns	,		

VOLTAGE WAVEFORMS

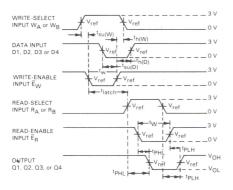


Fig. 1

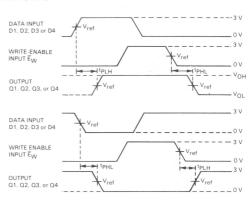


Fig. 2

MOTOROLA

DESCRIPTION — The SN54LS/74LS173A is a high-speed 4-Bit Register featuring 3-state outputs for use in bus-organized systems. The clock is fully edge-triggered allowing either a load from the D inputs or a hold (retain register contents) depending on the state of the Input Enable Lines ($\overline{\rm IE}_1$, $\overline{\rm IE}_2$). A HIGH on either Output Enable line ($\overline{\rm OE}_1$, $\overline{\rm OE}_2$) brings the output to a high impedence state without affecting the actual register contents. A HIGH on the Master Reset (MR) input resets the Register regardless of the state of the Clock (CP), the Output Enable ($\overline{\rm OE}_1$, $\overline{\rm OE}_2$) or the Input Enable ($\overline{\rm IE}_1$, $\overline{\rm IE}_2$) lines.

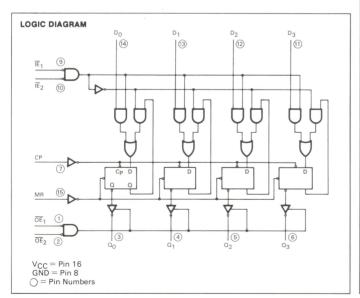
- FULLY EDGE-TRIGGERED
- 3-STATE OUTPUTS
- GATED INPUT AND OUTPUT ENABLES
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

PIN NAM	ES	LOADI	NG (Note a)
		HIGH	LOW
D_0-D_3	Data Inputs	0.5 U.L.	0.25 U.L.
IE ₁ -IE ₂	Input Enable (Active LOW)	0.5 U.L.	0.25 U.L.
$\overline{OE}_1 - \overline{OE}_2$	Output Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
CP	Clock Pulse (Active HIGH Going Edge)	0.5 U.L.	0.25 U.L.
	Input		
MR	Master Reset input (Active HIGH)	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Outputs (Note b)	65(25)U.L.	15(7.5)U.L.

NOTES:

a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

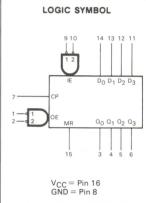
b. The Output LOW drive factor is 2.5 U.L. for Military $\,$ (54) and 5 U.L. for Commercial (74) Temperature Ranges.

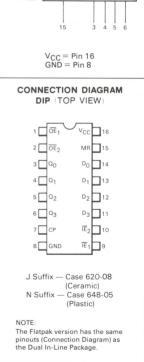


SN54LS173A SN74LS173A

4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY





GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54 74			-1.0 -2.6	mA
lOL	Output Current — Low	54 74			12 24	mA

TRUTH TABLE

MR	CP	ĪĒ ₁	ĪĒ ₂	Dn	Qn
Н	х	x	Х	х	L
L	L	x	X	x	Qn
L	5	Н	X	X	Qn
L	5	×	Н	X	Qn
L	5	L	L	L	L
L	5	L	L	Н	Н

When either \overline{OE}_1 or \overline{OE}_2 are HIGH, the output is in the off state (High Impedence); however this does not affect the contents or sequential operation of the register.

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

CVMADOL	PARAMETER			LIMITS		LINUTC	TEST CONDITIONS	
SYMBOL	PARAMETER	(MIN	TYP	MAX	UNITS	IEST	CONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp	out HIGH Voltage for
		54			0.7	.,		out LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
VOH	Output HIGH Voltage	54	2.4	3.4		V	$V_{CC} = MIN$, $I_{OH} = MAX$, $V_{IN} = V_{OT}$ or V_{IL} per Truth Table	
*OH	output man voltage	74	2.4	3.1		V		
		54,74		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	٧	I _{OL} = 24 mA	VIN = VIL or VIH per Truth Table
lozh	Output Off Current HIG	Н			20	μΑ	V _{CC} = MAX, V	0 = 2.4 V
lozL	Output Off Current LOV	V			-20	μΑ	V _{CC} = MAX, V	0 = 0.4 V
					20	μΑ	V _{CC} = MAX, V	IN = 2.7 V
lН	Input HIGH Current				0.1	mA .	V _{CC} = MAX, V	IN = 7.0 V
IIL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V	IN = 0.4 V
los	Short Circuit Current		-30		-130	. mA	V _{CC} = MAX	
lcc	Power Supply Current				30	mA	$V_{CC} = MAX$	

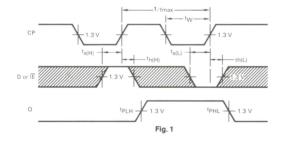
AC CHARACTERISTICS: $T_A = 25$ °C

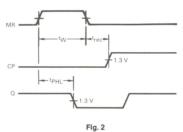
0)/44001	545445755	LIMITS		LINUTO	TEGT CONDITIONS		
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
fMAX	Maximum Input Clock Frequency	30	50		MHz		
^t PLH ^t PHL	Propagation Delay, Clock to Output	1,2	17 22	25 30	ns	V _{CC} = 5.0 V	
^t PHL	Propagation Delay, MR To Output		26	35	ns	$C_L = 45 \text{ pF},$	
^t PZH ^t PZL	Output Enable Time		15 18	23 27	ns	$R_L = 667 \Omega$	
^t PLZ ^t PHZ	Output Disable Time		11 11	17 17	ns	$C_L = 5.0 \text{ pF}$ $R_L = 667 \Omega$	

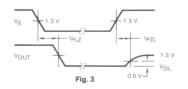
AC SETUP REQUIREMENTS: $T_A = 25$ °C

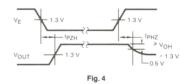
CVMPOL	PARAMETER		LIMITS			TEST COMPITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
tw	Clock or MR Pulse Width	20			ns		
t _S	Data Enable Setup Time,	35			ns		
t _S	Data Setup Time	17			ns	V _{CC} = 5.0 V	
th	Hold Time, Any Input	0			ns		
t _{rec}	Recovery Time	10			ns		

AC WAVEFORMS



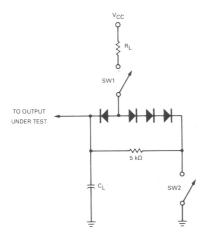






AC LOAD CIRCUIT

Fig. 5



*Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2		
tpzh	Open	Closed		
tpzL	Closed	Open		
tpLZ	Closed	Closed		
tpHZ	Closed	Closed		



DESCRIPTION — The LSTTL/MSI SN54LS/74LS174 is a high speed Hex D Flip-Flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW to HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops. The LS174 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED-POSITIVE EDGE-TRIGGERED CLOCK
- ASYNCHRONOUS COMMON RESET
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

SN54LS174 SN74LS174

HEX D FLIP-FLOP

LOW POWER SCHOTTKY

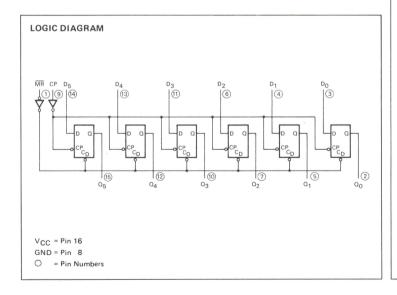
PIN NAMES

		HIGH	LOW
$D_0 - D_5$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_5$	Outputs (Note b)	10 U.L.	5 (2.5) U.L.

LOADING (Note a)

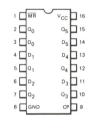
NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.



V_{CC} = Pin 16 GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05

(Plastic)

NOTE

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset $(\overline{\text{MR}})$ are common to all flip-flops.

Each D input's state is transferred to the corresponding flip-flop's output following the LOW to HIGH Clock (CP) transition.

A LOW input to the Master Reset $(\overline{\text{MR}})$ will force all outputs LOW independent of Clock or Data inputs. The LS174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

TRUTH TABLE

Inputs (t = n, MR = H)	Outputs (t = n+1) Note 1
D	Q
Н	Н
L	L

Note 1: t = n + 1 indicates conditions after next clock.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP .	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

OV/A A D. O. I	DADAMETE			LIMITS		LINUTO	TECT	ONDITIONS	
SYMBOL	PARAMETER	PARAMETER MIN TYP MAX		UNITS	TEST	ONDITIONS			
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for	
.,		54			0.7	.,		ut LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = - 18 mA		
√он	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$	
VOH	Output Fild i Voltage	74	2.7	3.5		V	or VIL per Truth	n Table	
		54,74		0.25	0.4	V ,	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	V _{CC} = MAX, V	N = 2.7 V	
IH	Input HIGH Current			×	0.1	mA	V _{CC} = MAX, V _I	N = 7.0 V	
IL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V		
OS	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	$V_{CC} = MAX$	
СС	Power Supply Current				26	mA	V _{CC} = MAX		

AC CHARACTERISTICS: TA = 25°C

SYMBOL	PARAMETER	LIMITS		LINUTC		TEST COMPITIONS		
	PARAMETER		TYP	MAX	UNITS	TEST CONDITIONS		
fMAX	Maximum Input Clock Frequency	30	40		MHz	*		
^t PHL	Propagation Delay, MR to Output		23	35	ns	$V_{CC} = 5.0 \text{ V}$		
tPLH tPHL	Propagation Delay, Clock to Output		20 21	30 30	ns	$C_L = 15 pF$		

AC SETUP REQUIREMENTS: $T_A = 25$ °C

SYMBOL	DADAMETER	LIMITS			LINITO	TEGT COMPLETIONS
	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
tw	Clock or MR Pulse Width	20			ns	
t _S	Data Setup Time	20			ns	$V_{CC} = 5.0 \text{ V}$
th	Data Hold Time	5.0			ns	VCC 3.5 V
t _{rec}	Recovery Time	25			ns	

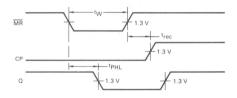
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SETUP AND HOLD TIMES DATA TO CLOCK

CP 1.3 V 1.3

*The shedden was indicate when the input is premitted to observe

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

Fig. 2

DEFINITIONS OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.



DESCRIPTION — The LSTTL/MSI SN54LS/74LS175 is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

The LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED-POSITIVE EDGE-TRIGGERED CLOCK
- CLOCK TO OUTPUT DELAYS OF 30 ns
- ASYNCHRONOUS COMMON RESET
- TRUE AND COMPLEMENT OUTPUT
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

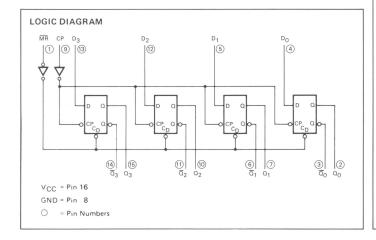
PIN NAMES

PIN NAIVIES		LUADIN	(Note a)
		HIGH	LOW
$D_0 - D_3$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\sigma^0 - \sigma^3$	True Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_0 - \overline{Q}_3$	Complemented Outputs (Note b)	10 U.L.	5(2.5) U.L.

LOADING (Note a)

NOTES:

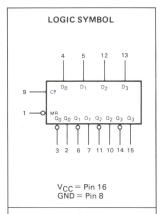
- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.



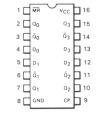
SN54LS175 SN74LS175

QUAD D FLIP-FLOP

LOW POWER SCHOTTKY



CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic)

N Suffix — Case 648-05 (Plastic)

NOTE:

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and \overline{Q} outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and \overline{Q} outputs to follow. A LOW input on the Master Reset (\overline{MR}) will force all Q outputs LOW and \overline{Q} outputs HIGH independent of Clock or Data inputs.

The LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

Outputs (t =	n+1) Note 1
Q	ā
L	Н
н	L
	Outputs (t = Q L H

Note 1: t = n + 1 indicates conditions after next clock.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

CVAADOL	PARAMETER		LIMITS			LINUTO	TEST CONDITIONS	
SYMBOL			MIN	TYP	MAX	UNITS	TEST CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
		54			0.7			ut LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} =-18 mA	
Vон	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IF}$
	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
					20	μΑ	V _{CC} = MAX, V _I	N = 2.7 V
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V
İIL	Input LOW Current	W Current			-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V
os	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
lcc	Power Supply Current				18	mA	$V_{CC} = MAX$	

AC CHARACTERISTICS: $T_A = 25$ °C

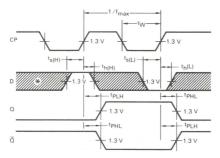
CVMAROL	B4844575B	LIMITS			LINUTO	TEST COMPITIONS
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
fMAX	Maximum Input Clock Frequency	30	40		MHz	
^t PLH ^t PHL	Propagation Delay, MR to Output		20 20	30 30	ns	$V_{CC} = 5.0 V$ $C_L = 15 pF$
^t PLH ^t PHL	Propagation Delay, Clock to Output		13 16	25 25	ns	

AC SETUP REQUIREMENTS: TA = 25°C

SYMBOL	DADAMETED		LIMITS			TECT COMPLETIONS	
	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t₩	Clock or MR Pulse Width	20			ns		
t _S	Data Setup Time	20			ns	$V_{CC} = 5.0 \text{ V}$	
th	Data Hold Time	5.0			ns	700 3.5 7	
trec	Recovery Time	25			ns		

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SETUP AND HOLD TIMES DATA TO CLOCK



^{*}The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

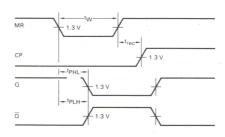


Fig. 2

DEFINITIONS OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.



DESCRIPTION — The SN54LS/74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic, operations on two variables and a variety of arithmetic operations.

- PROVIDES 16 ARITHMETIC OPERATIONS ADD, SUBTRACT, COMPARE, DOUBLE, PLUS TWELVE OTHER ARITHMETIC OPERATIONS
- PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES EXCLUSIVE-OR, COMPARE, AND, NAND, OR, NOR, PLUS TEN OTHER LOGIC OPERATIONS
- FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC **OPERATION ON LONG WORDS**
- INPUT CLAMP DIODES

SN54LS181 SN74LS181

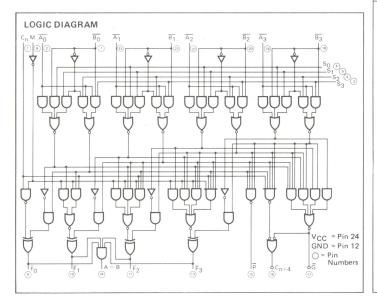
4-BIT ARITHMETIC LOGIC UNIT

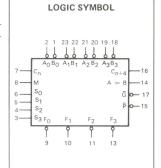
LOW POWER SCHOTTKY

PIN NAMES		LOADING	G (Note a)
		HIGH	LOW
$\overline{A}_0 - \overline{A}_3$, $\overline{B}_0 - \overline{B}_3$	Operand (Active LOW) Inputs	1.5 U.L	0.75 U.L.
S ₀ -S ₃	Function - Select Inputs	2.0 U.L.	1.0 U.L.
M	Mode Control Input	0.5 U.L.	0.25 U.L.
C _n	Carry Input	2.5 U.L.	1.25 U.L.
$\overline{F}_0 - \overline{F}_3$	Function (Active LOW) Outputs	10 U.L.	5 (2.5) U.L.
A = B	Comparator Output	Open Collector	5 (2.5) U.L.
G	Carry Generator (Active LOW) Output	10 U.L.	10 U.L.
P	Carry Propagate (Active LOW) Output	10 U.L.	5 U.L.
C_{n+4}	Carry Output	10 U.L.	5 (2.5) U.L.

NOTES:

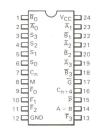
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.





 $V_{CC} = Pin 16$ GND = Pin 8

CONNECTION DIAGRAMS DIP (TOP VIEW)



J Suffix — Case 623-05 (Ceramic) N Suffix - Case 649-03

(Plastic)

NOTE:

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

FUNCTIONAL DESCRIPTION — The SN54LS/74LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \dots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals \overline{P} (Carry Propagate) and \overline{G} (Carry Generate), \overline{P} and \overline{G} are not affected by carry in. When speed requirements are not stringent, the LS181 can be used in a simple ripple carry mode by connecting the Carry Output (C_{n+4}) signal to the Carry Input (C_n) of the next unit. For high speed operation the LS181 is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of the four LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A=B output from the LS181 goes HIGH when all four \overline{F} outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A=B output is open collector and can be wired-AND with other A=B outputs to give a comparison for more than four bits. The A=B signal can also be used with the C_{n+4} signal to indicate A>B and $A\le B$.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, the LS181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

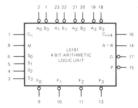
MODE SELECT INPUTS	ACTIVE LOW INPUTS & OUTPUTS	ACTIVE HIGH INPUTS & OUTPUTS
s ₃ s ₂ s ₁ s ₀	LOGIC ARITHMETIC** (M = H) (M = L) (C _n = L)	LOGIC ARITHMETIC** (M = H) (M = L)(C _n = H)
	A minus 1 AB AB minus 1 A+B AB minus 1 A+B AP minus 1 A+B AP lus (A+B) B AB plus (A+B) A ⊕ B A minus B minus 1 A+B A Plus (A+B) A ⊕ B A Plus (A+B) A ⊕ B A Plus B B AB plus (A+B) A+B A+B B AB plus B B AB plus B B AB plus B B AB plus B B AB plus A+B	A A A B A + B A A + B B A B A + B B A B A
нннн	A A	A A minus 1

L = LOW Voltage Level

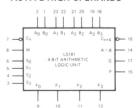
H = HIGH Voltage Level

LOGIC SYMBOLS

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



^{*}Each bit is shifted to the next more significant position

^{* *} Arithmetic operations expressed in 2s complement notation

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA
Vон	Output Voltage — High (A=B only)	54,74			5.5	V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS	B 4 A 3 /	UNITS	TEST	CONDITIONS	
V _{IH}	Input HIGH Voltage		2.0	TYP	MAX	V	Guaranteed In	put HIGH Voltage for	
V _{IL}	Input LOW Voltage	54 74			0.7	V	-	put LOW Voltage for	
VIK	Input Clamp Diode Volta	ige		-0.65	-1.5	V	V _{CC} = MIN, I _I	N =-18 mA	
Voн	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _C	$O_H = MAX, V_{IN} = V_{IH}$	
VOH	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Trut	th Table	
	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$		
	Except $\overline{\mathbb{G}}$ and $\overline{\mathbb{P}}$	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	$V_{CC} = V_{CC} MIN, V_{IN} =$	
VOL	Output G	54,74			0.7	V	$I_{OL} = 16 \text{ mA}$	V _{IL} or V _{IH} per Truth Table	
	Output P	54 74			0.6 0.5	V	I _{OL} = 8.0 mA		
ЮН	Output HIGH Current	54,74			100	μΑ	V _{CC} = MIN, I _C or V _{IL} per Trut	$_{\mathrm{DH}}=\mathrm{MAX},\mathrm{V_{IN}}=\mathrm{V_{IH}}$	
¹ ін	Input HIGH Current Mode Input Any Ā or Ē Input Any S Input C _n Input				20 60 80 100	μΑ	V _{CC} = MAX,	√ _{IN} = 2.7 ∨	
10	Mode Input Any A or B Input Any S Input C _n Input				0.1 0.3 0.4 0.5	mA	V _{CC} = MAX, V	√ _{IN} = 7.0 ∨	
l _{IL}	Input Low Current Mode Input Any Ā or B Input Any S Input Cn Input				-0.4 -1.2 -1.6 -2.0	mA	V _{CC} = MAX, \	$V_{1N} = 0.4 \text{ V}$	
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
	Power Supply Current	54			32				
1	See Note 1A	74			34				
lcc		54			35	mA	$V_{CC} = MAX$		
	See Note 1B	See Note 1B 74			37				

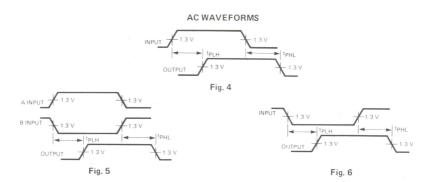
Note 1.

With outputs open, I_{CC} is measured for the following conditions: A. SO through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.

B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

 $\textbf{AC CHARACTERISTICS:} \ T_{\mbox{\scriptsize A}} = 25 ^{\circ} \mbox{\scriptsize C}, \ V_{\mbox{\scriptsize CC}} = 5.0 \ \mbox{\scriptsize V}, \ \mbox{\scriptsize Pin } 12 = \mbox{\scriptsize GND}, \ \mbox{\scriptsize C}_{\mbox{\scriptsize L}} = 15 \ \mbox{\scriptsize pF}$

		LIM	IITS			
SYMBOL	PARAMETER	TYP	MAX	UNITS	CONDITIONS	
^t PLH ^t PHL	Propagation Delay, $(C_n \text{ to } C_{n+4})$	18 13	27 20	ns	M = 0 V, (Sum or Diff Mode) See Fig. 4 and Tables I and II	
^t PLH ^t PHL	(C _n to F Outputs)	17 13	26 20	ns	M = 0 V, (Sum Mode) See Fig. 4 and Table I	
^t PLH ^t PHL	(\overline{A} or \overline{B} Inputs to \overline{G} Output)	19 15	29 23	ns	$M = S_1 = S_2 = 0 \text{ V}, S_0 = S_3 = 4.5 \text{ V}$ (Sum Mode) See Fig. 4 and Table I	
^t PLH ^t PHL	(A or B Inputs to G Output)	21 21	32 32	ns	$M = S_0 = S_3 = 0 \text{ V}, S_1 = S_2 = 4.5 \text{ V}$ (Diff Mode) See Fig. 5 and Table II	
^t PLH ^t PHL	(A or B Inputs to P Output)	20 20	30 30	ns	$M = S_1 = S_2 = 0 \text{ V}, S_0 = S_3 = 4.5 \text{ V}$ (Sum Mode) See Fig. 4 and Table I	
^t PLH ^t PHL	(Ā or B Inputs to P Output)	20 22	30	ns	$M=S_0=S_3=0\ V,\ S_1=S_2=4.5\ V$ (Diff Mode) See Fig. 5 and Table II	
^t PLH ^t PHL	(A or B Inputs to any F Output)	21 13	32 20	ns	$M = S_1 = S_2 = 0 \text{ V}, S_0 = S_3 = 4.5 \text{ V}$ (Sum Mode) See Fig. 4 and Table I	
^t PLH ^t PHL	(Ā or B Inputs to any F Output)	21 21	32 32	ns	$M = S_0 = S_3 = 0 \text{ V}, S_1 = S_2 = 4.5 \text{ V}$ (Diff Mode) See Fig. 5 and Table II	
^t PLH ^t PHL	(Ā or B Inputs to F Outputs)	22 26	33 38	ns	M = 4.5 V (Logic Mode) See Fig. 4 and Table III	
^t PLH ^t PHL	$(\overline{A} \text{ or } \overline{B} \text{ Inputs to } C_{n+4} \text{ Output})$	25 25	38 38	ns	$\text{M}=\text{0 V},\text{S}_0=\text{S}_3=4.5\text{ V},\text{S}_1=\text{S}_2=\text{0 V}$ (Sum Mode) See Fig. 6 and Table I	
^t PLH ^t PHL	$(\overline{A} \text{ or } \overline{B} \text{ Inputs to C}_{n+4} \text{ Output})$	27 27	41 41	ns	$M = 0 \text{ V, } S_0 = S_3 = 0 \text{ V, } S_1 = S_2 = 4.5 \text{ V}$ (Diff Mode)	
^t PLH ^t PHL	$(\bar{A} \text{ or } \bar{B} \text{ Inputs to } A = B \text{ Output})$	33 41	50 62	ns	$\begin{array}{l} \text{M} = \text{S}_0 = \text{S}_3 = \text{0 V, S}_1 = \text{S}_2 = 4.5 \text{ V} \\ \text{R}_L = 2 \text{ k}\Omega \\ \text{(Diff Mode) See Fig. 5 and Table II} \end{array}$	



DIFF MODE TEST TABLE II

FUNCTION	INPUTS: 9	S1 =	$S_2 = 0$	4.5 V.	Sn=	S2 =	M =	0 V

PARAMETER	INPUT	OTHER SAME		OTHER DA	TA INPUTS	OUTPUT UNDER	
FARAIVIETER	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST	
^t PLH ^t PHL	Ā	None	B	Remaining A	Remaining B, C _n	FI	
^t PLH ^t PHL	B	Ā	None	Rem <u>ai</u> ning A	Remaining B, C _n	FI	
^t PLH ^t PHL	ĀĮ	None	\overline{B}_{I}	Remaining B, C _n	Rem <u>ai</u> ning A	F _I + 1	
^t PLH ^t PHL	Bl	ĀI	None	Remaining B, C _n	Rem <u>ai</u> ning A	F _I + 1	
^t PLH ^t PHL	Ā	None	B	None	Remaining A and B, Cn	P	
^t PLH ^t PHL	B	Ā	None	None	Remaining A and B, C _n	P	
^t PLH ^t PHL	Ā	B	None	None	Remaining A and B _I , C _n	G	
^t PLH ^t PHL	В	None	Ā	None	Remaining A and B, Cn	G	
^t PLH ^t PHL	Ā	None	B	Remaining A	Remaining B, C _n	A = B	
^t PLH ^t PHL	B	Ā	None	Rem <u>ai</u> ning A	Remaining B, C _n	A = B	
^t PLH ^t PHL	Ā	B	None	None	Remaining A and B, C _n	C _n + 4	
^t PLH ^t PHL	B	None	Ā	None	Remaining A and B, C _n	C _n + 4	
^t PLH ^t PHL	C _n	None	None	$\frac{\text{All}}{\text{A} \text{ and } \text{B}}$	None	C _n + 4	

LOGIC MODE TEST TABLE III

242445752	INPUT	OTHER INPUT SAME BIT		OTHER DA	ATA INPUTS	OUTPUT	FUNCTION INDUTO	
PARAMETER	UNDER TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	UNDER TEST	FUNCTION INPUTS	
^t PLH ^t PHL	Ā	None	B	None	Remaining Ā and B, C _n	Any F	$S_1 = S_2 = M = 4.5 \text{ V}$ $S_0 = S_3 = 0 \text{ V}$	
^t PLH ^t PHL	B	None	Ā	None	Remaining Ā and B, C _n	Any F	$S_1 = S_2 = M = 4.5 \text{ V}$ $S_0 = S_3 = 0 \text{ V}$	

SUM MODE TEST TAB	LE I	FUNCTION INPUTS: $s_0 = s_3 = 4.5 \text{ V}, s_1 = s_2 = \text{M} = 0 \text{ V}$
	OTHER INDUST	-

PARAMETER	INPUT UNDER	OTHER I SAME		OTHER DA	TA INPUTS	OUTPUT UNDER
FARAIVIETER	TEST			APPLY 4.5 V	APPLY GND	TEST
^t PLH ^t PHL	ĀI	BI	None	Remaining A and B	C _n	FI
^t PLH ^t PHL	B _I	ĀI	None	Remaining A and B	C _n	Fi
^t PLH ^t PHL	Āl	BI	None	Cn	Remaining A and B	Fi + 1
^t PLH ^t PHL	BI	ĀĮ	None	Cn	Remaining A and B	$\bar{F}_{I} + 1$
tPLH tPHL	Ā	B	None	None	Remaining A and B, Cn	P
tPLH tPHL	B	Ā	None	None	Remaining A and B, C _n	Ē
[†] PĽH [†] PHL	Ā	None	B	Remaining B	Remaining Ā, C _n	G
[†] PLH [†] PHL	B	None	Ā	Remaining B	Remaining A, C _n	G
[†] PLH [†] PHL	Ā	None	B	Remaining B	Remaining A, C _n	C _{n+4}
[†] PLH [†] PHL	B	None	Ā	Remaining B	Remaining A, C _n	C _{n+4}
^t PLH ^t PHL	C _n	None	None	AII Ā	AII B	Any F or C _{n+4}



DESCRIPTION — The SN54LS/74LS182 is a high-speed Carry Lookahead Generator. It is generally used with the SN54LS/74LS181 4-Bit Arithmetic Logic Unit to provide high speed lookahead over word lengths of more than four bits. The carry lookahead generator is fully compatible with all members of the Motorola TTL Family.

- PROVIDES CARRY LOOKAHEAD ACROSS A **GROUP OF FOUR ALUS**
- MULTI-LEVEL LOOKAHEAD FOR HIGH-SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION **EFFECTS**

SN54LS182 SN74LS182

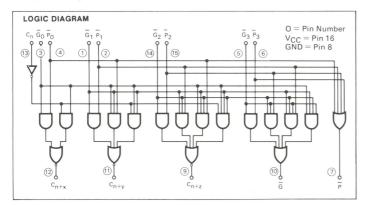
CARRY LOOKAHEAD GENERATOR

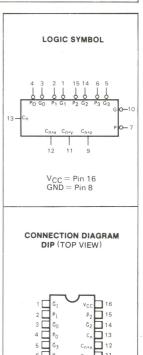
LOW POWER SCHOTTKY

LOADING (Note a) HIGH LOW

		-	
PIN NAMES		HIGH	LOW
$\begin{array}{c} C_n \\ \overline{G}_{0} \\ \overline{G}_{1} \\ \overline{G}_{1} \\ \overline{G}_{1} \\ \overline{G}_{1} \\ \overline{G}_{2} \\ \overline{G}_{1} \\ \overline{G}_{2} \\ \overline{G}_{1} \\ \overline{G}_{2} \\ \overline{G}_{2} \\ \overline{G}_{3} \\ \overline{G}_{1} \\ \overline{G}_{2} \\ \overline{G}_{3} \\ \overline{G}_{2} \\ \overline{G}_{3} \\ \overline{G}_{2} \\ \overline{G}_{3} $	Carry Input	0.5 U.L.	0.25 U.L.
\overline{G}_{o} , \overline{G}_{2}	Carry Generate (Active LOW) Inputs	3.5 U.L.	1.75 U.L.
\overline{G}_1	Carry Generate (Active LOW) Input	4.0 U.L.	2.0 U.L.
$\overline{G}_{\scriptscriptstyle 3}$	Carry Generate (Active LOW) Input	2.0 U.L.	1.0 U.L.
\overline{P}_{o} , \overline{P}_{1}	Carry Propagate (Active LOW) Inputs	2.0 U.L.	1.0 U.L.
\overline{P}_{2}	Carry Propagate (Active LOW) Input	1.5 U.L.	0.75 U.L.
\overline{P}_3	Carry Propagate (Active LOW) Input	1.0 U.L.	0.5 U.L.
\underline{C}_{n+x} , C_{n+y} , C_{n+z}	Carry Outputs (Note b)	10 U.L.	5 (2.5) U.L.
G	Carry Generate (Active LOW) Output	10 U.L.	5 (2.5) U.L.
	(Note b)		
P	Carry Propagate (Active LOW) Output	10 U.L.	5 (2.5) U.L.
	(Note b)		

- a. 1 Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.







J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

NOTE:

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The SN54LS/74LS182, carry lookahead generator $\underline{accepts\ up\ to\ four\ pairs\ of\ active\ LOW\ Carry\ Propagate\ (\overline{P}_0,\overline{P}_1,\overline{P}_2,\overline{P}_3)\ and\ Carry\ Generate\ (\overline{G}_0,\overline{P}_1,\overline{P}_2,\overline{P}_3)}$ \overline{G}_1 , \overline{G}_2 , \overline{G}_3) signals and an active HIGH Carry Input (C_n) and provides anticipated active HIGH carries (C_{n+x} , C_{n+y} , C_{n+z}) across four groups of binary adders. The SN54LS/74LS182 also has active LOW Carry Propagate $\overline{(P)}$ and Carry Generate $\overline{(G)}$ outputs which may be used for further levels of lookahead.

The logic equations provided at the outputs are:

$$\begin{array}{l} c_{n+x} = g_0 + P_0 C_n \\ c_{n+y} = g_1 + P_1 G_0 = P_1 P_0 C_n \\ c_{n+z} = g_2 + P_2 g_1 = P_2 P_2 G_0 + P_2 P_1 P_0 C_n \\ \overline{G} = \overline{g_3 + P_3 G_2} + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 \\ \overline{P} = P_3 P_2 P_1 P_0 \end{array}$$

Also, the SN54LS/74LS182 can be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry lookahead generator are identical in both cases.

TRUTH TABLE

				INPUTS	3					.0	UTPUTS		
Cn	\bar{G}_0	P ₀	G ₁	P ₁	G ₂	\overline{P}_2	G ₃	P ₃	C _{n+x}	C _{n+y}	C _{n+z}	G	P
×	н	н.							: L				
L	Н	×							. L				
X	L	· ×							н				
Н	×	L							н				
X	×	×	Н	Н				-5		L			
X	Н	Н	Н	×						L			
L	Н	×	Н	×						L			
X	×	×	L	×						Н			
X	L	×	×	L						Н			
Н	×	L	×	L						Н			
X	X	×	X	X	Н	Н					L		
X	×	X	Н	Н	Н	X					L		
X	Н	Н	Н	X	Н	X					L		
L	Н	X	Н	X	Н	X					L		
X	×	×	×	×	L	×					Н		
X	×	×	L	X	×	L					Н		
X	L	×	×	L	X	L					Н		
Н	×	L	×	L	×	L					Н		
	X		×	X	X	X	Н	Н				Н	
	X		X	X	Н	Н	Н	×				Н	
	X		Н	Н	Н	×	Н	×				Н	
	Н		Н	X	Н	×	Н	×				Н	
	×		×	X	X	X	L	×				L	
	×		X	×	L	×	×	L				L	
	×		L	X	×	L	×	L				L	
	L		X	L	×	L	×	L				L	
		Н		×		×		X					Н
		×		Н		×		×					Н
		×		×		Н		×					Н
		X		×		×		Н					Н
		L		L		L		L					L

H = HIGH Voltage Level

L = LOW Voltage Level X = Immaterial

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS	
STIVIBUL	PARAIVIETER		MIN	TYP	MAX	UNITS		
VIH	Input HIGH Voltage		2.0	* 3		V	Guaranteed In All Inputs	put HIGH Voltage for
		54			0.7			put LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN	I _{IN} = -18 mA
VoH	Output HIGH Voltage	54	2.5			V	I _{OH} = MAX	$V_{CC} = MIN, V_{IN} = V_{IH}$
		74	2.7	1 2 1 -				or VIL per Truth Table
VOL	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = MIN, V_{IN} = V_{IH}$
· OL		74		0.35	0.5		$I_{OL} = 8.0 \text{ mA}$	or V _{IL} per Truth Table
lo.	Cn G0, G2 G3, P0, P1 P2 P3 G1				20 140 80 60 40 160	μΑ		N = 2.7 V N = 2.7 V N = 2.7 V
liн	C _n G ₀ , Ḡ ₂ Ḡ ₃ , P̄ ₀ , P̄ ₁ P̄ ₂ P̄ ₃ Ḡ ₁				0.1 0.7 0.4 0.3 0.2 0.8	mA	$V_{IN} = 7.0 \text{ V}$ $V_{CC} = \text{MAX}$	
I _{IL}	Cn Go, G2 G3, Po, P1 P2 P3 G1				-0.4 -2.8 -1.6 -1.2 -0.8 -3.2	mA		N = 0.4 V $CC = MAX$
los	Output Short-Circuit Cu	rrent	-20		-100	mA		DUT = 0 V
lcc	Power Supply Current Total, Output HIGH				12	mA	VC	$_{C} = MAX$
	Total, Output LOW				16			

AC CHARACTERISTICS: $T_A = 25^{\circ}C$, $V_{CC} = 5.0 \text{ V}$, $C_L = 15 \text{ pF}$

0.44501	5.5		LIMITS			TECT CONDITIONS
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
tPLH tPHL	$(C_n \text{ to } C_{n+x}, C_{n+y}, C_{n+z})$		12 17	25 30	ns	$\overline{P}_0 = \overline{P}_1 = \overline{P}_2 = \overline{G}$ nd, $\overline{G}_0 = \overline{G}_1 = \overline{G}_2 = 4.5$ V, Fig. 1
^t PLH ^t PHL	$(\overline{P}_0, \overline{P}_1, \text{ or } \overline{P}_2 \text{ to } C_{n+x}, C_{n+y}, C_{n+z})$		9.0 10	21 22	ns	$\overline{P}_X = Gnd$ (if not under test), $C_n = \overline{G}_0 = \overline{G}_1 = \overline{G}_2 = 4.5 \text{ V, Fig. 2}$
tPLH tPHL	$(\overline{G}_0, \overline{G}_1, \text{ or } \overline{G}_2 \text{ to } C_{n+x}, C_{n+y}, C_{n+z})$		9.0 10	21 22	ns	$\overline{G}_X = 4.5 \text{ V (If not under test),}$ $C_n = \overline{P}_0 = \overline{P}_1 = \overline{P}_2 = \text{Gnd, Fig. 2}$
tPLH tPHL	(P ₁ , P ₂ or P ₃ to G)		12 8.0	24 20	ns	$ \overline{\overset{P}{G}}_{x} = \text{Gnd (If not under test)}, \\ \overline{\overset{G}{G}}_{0} = \overline{\overset{G}{G}}_{1} = \overline{\overset{G}{G}}_{2} = \overline{\overset{G}{G}}_{3} = \overset{C}{\overset{C}{G}}_{n} = 0.0 \text{ V}, \\ \overline{\overset{F}{\text{ig. 1}}} = \overset{C}{\overset{C}{\overset{C}{G}}} = \overset{C}{\overset{C}{\overset{C}{G}}} = \overset{C}{\overset{C}{\overset{C}{G}}} = \overset{C}{\overset{C}{\overset{C}{G}}} = \overset{C}{\overset{C}{\overset{C}{\overset{C}{G}}}} = \overset{C}{\overset{C}{\overset{C}{\overset{C}{G}}}} = \overset{C}{\overset{C}{\overset{C}{\overset{C}{\overset{C}{G}}}}} = \overset{C}{\overset{C}{\overset{C}{\overset{C}{\overset{C}{\overset{C}{\overset{C}{\overset{C}$
^t PLH ^t PHL	$(\overline{G}_0, \overline{G}_1, \overline{G}_2 \text{ or } \overline{G}_3 \text{ to } \overline{G})$		13 8.0	25 20	ns	$\overline{G}_X = 4.5 \text{ V (If not under test)},$ $\overline{P}_1 = \overline{P}_2 = \overline{P}_3 = \text{Gnd, Fig. 1}$
^t PLH ^t PHL	$(\bar{P}_0, \bar{P}_1, \bar{P}_2 \text{ or } \bar{P}_3 \text{ to } \bar{P})$		12 8.0	24 20	ns	$\overline{P}_{X} = Gnd$ (If not under test), Fig. 1

AC WAVEFORMS

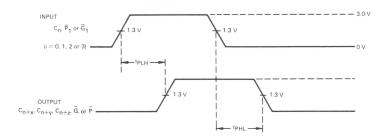


Fig.1

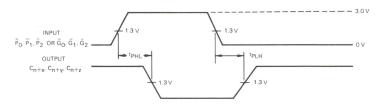


Fig. 2



DESCRIPTION—The SN54LS/74LS183 is a Dual Adder. This device features high-speed, high-fan-out Darlington outputs and all inputs are diode clamped for system design simplification. An individual carry output from each bit is featured for use in multiple-input, carry-save techniques to produce true sum and true carry outputs with no more than two gate delays.

- FOR USE IN HIGH-SPEED WALLACE-TREE SUMMING NETWORKS
- HIGH-SPEED, HIGH-FAN-OUT DARLINGTON OUTPUTS

FUNCTION TABLE

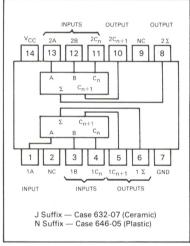
INPUTS		OUTPUTS						
В А		Σ	C _{n+1}					
L	L	L	L					
L	Н	Н	L					
Н	L	Н	L					
Н	Н	L	Н					
L	L	Н	L					
L	Н	L	Н					
Н	L	L	Н					
Н	Н	Н	Н					
	B L L H H	B A L L H H L H L H L L L H L L	B A Σ L L L H H H L H L H L L H L L H L L L L L L L L L L L L					

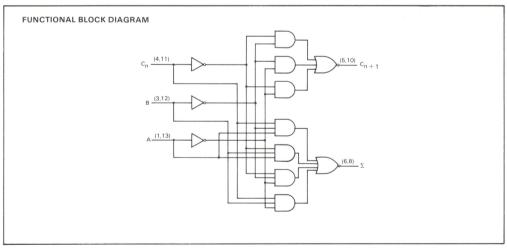
H = high level, L = low level

SN54LS183 SN74LS183

DUAL CARRY-SAVE FULL ADDER

LOW POWER SCHOTTKY





SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
Тд	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High				-0.4	mA
OL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMAROL	PARAMETER			LIMITS		UNITS	TEST	CNIDITIONS
SYMBOL	PARAMETE		MIN TYP MAX UNI		UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage All Inputs	
		54			0.7	.,		out LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} =-18 mA	
VOH	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$
	Output midn voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
					60	μΑ	V _{CC} = MAX, V _I	N = 2.7 V
lН	Input HIGH Current				0.3	mA	V _{CC} = MAX, V _I	N = 7.0 V
ΙΙL	Input LOW Current				-1.2	mA	V _{CC} = MAX, V _I	N = 0.4 V
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
lcc	Power Supply Current Total, Output HIGH Total, Output LOW				14 17	mA	V _{CC} = MAX	

AC CHARACTERISTICS: TA = 25°C

CVMPOL	PARAMETER		LIMITS		LINUTO	TECT COMPLTIONS	
SYMBOL		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH	Propagation Delay Time, Low-to-High Level Output	,	9.0	15	ns	V _{CC} = 5.0 V	
^t PHL	Propagation Delay Time, High-to-Low Level Output		20	33	ns	$C_L = 15 \text{ pF}$	



DESCRIPTION — The SN54LS/74LS190 is a synchronous UP/DOWN BCD Decade (8421) Counter and the SN54LS/74LS191 is a synchronous UP/DOWN Modulo-16 Binary Counter. State changes of the counters are synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

An asynchronous Parallel Load (\overline{PL}) input overrides counting and loads the data present on the P_n inputs into the flip-flops, which makes it possible to use the circuits as programmable counters. A Count Enable (\overline{CE}) input serves as the carry/borrow input in multi-stage counters. An Up/Down Count Control (\overline{U}/D) input determines whether a circuit counts up or down. A Terminal Count (TC) output and a Ripple Clock (\overline{RC}) output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multi-stage counter applications.

- LOW POWER . . . 90 mW TYPICAL DISSIPATION
- HIGH SPEED . . . 25 MHz TYPICAL COUNT FREQUENCY
- SYNCHRONOUS COUNTING
- ASYNCHRONOUS PARALLEL LOAD
- INDIVIDUAL PRESET INPUTS
- COUNT ENABLE AND UP/DOWN CONTROL INPUTS
- CASCADABLE
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

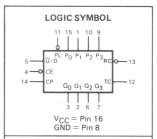
PIN NA	MES	LOADIN	IG (Note a)
		HIGH	LOW
CE	Count Enable (Active LOW) Input	1.5 U.L.	0.7 U.L.
CP	Clock Pulse (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
Ū/D	Up/Down Count Control Input	0.5 U.L.	0.25 U.L.
PL	Parallel Load Control (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5 (2.5) U.L.
RC	Ripple Clock Output (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54LS/74LS190 SN54LS/74LS191

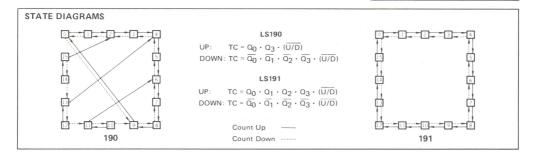
PRESETTABLE BCD/DECADE
UP/DOWN COUNTERS
PRESETTABLE 4-BIT BINARY
UP/DOWN COUNTERS
LOW POWER SCHOTTKY



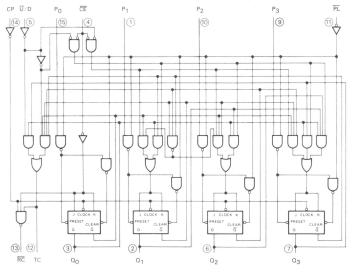
CONNECTION DIAGRAM DIP (TOP VIEW)



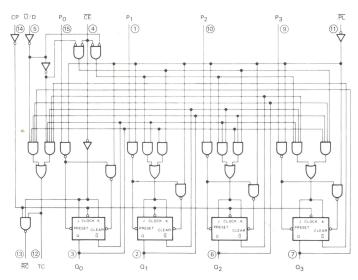
- J Suffix Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)
- The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



LOGIC DIAGRAMS



DECADE COUNTER LS190



V_{CC} = Pin 16 GND = Pin 8

= Pin Numbers

BINARY COUNTER LS191 **FUNCTIONAL DESCRIPTION** — The LS190 is a synchronous Up/Down BCD Decade Counter and the LS191 is a synchronous Up/Down 4-Bit Binary Counter. The operating modes of the LS190 decade counter and the LS191 binary counter are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (\overline{PL}) input is LOW, information present on the Parallel Data inputs (P_0-P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{\text{CE}}$ input inhibits counting. When $\overline{\text{CE}}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{\text{U}}/\text{D}$ input signal, as indicated in the Mode Select Table. When counting is to be enabled, the $\overline{\text{CE}}$ signal can be made LOW when the clock is in either state. However, when counting is to be inhibited, the LOW-to-HIGH $\overline{\text{CE}}$ transition must occur only while the clock is HIGH. Similarly, the $\overline{\text{U}}/\text{D}$ signal should only be changed when either $\overline{\text{CE}}$ or the clock is HIGH.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (9 for the LS190, 15 for the LS191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{\rm U}/{\rm D}$ is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock (\overline{RC}) output. The \overline{RC} output is normally HIGH. When \overline{CE} is LOW and TC is HIGH, the \overline{RC} output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-stage counters, as indicated in Figures a and b. In Figure a, each \overline{RC} output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on \overline{CE} inhibits the \overline{RC} output pulse, as indicated in the \overline{RC} Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the RC outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the RC output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The \overline{CE} input signal for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own \overline{CE} .

MODE SELECT TABLE

	INF	UTS	MODE	
PL	CE	Ū/D	CP	MODE
Н	L	L	Ţ	Count Up
Н	L	Н	1	Count Down
L	X	Χ	Χ	Preset (Asyn.)
Н	Н	X	Χ	No Change (Hold)

RC TRUTH TABLE

THO THIS THIS TABLE										
C										
PUT										
Г										
1										
ł										

*TC is generated internally

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

Γ = I OW-to-HIGH Clock Transition

☐= LOW Pulse

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ЮН	Output Current — High	54,74			-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DARAMETER	PARAMETER		LIMITS		UNITS	TEST CONDITIONS		
STIVIBUL	PARAMETER			TYP	MAX	UNITS	TEST COL	NDITIONS	
VIH	Input HIGH Voltage		2.0			V .	Guaranteed Input HIGH Voltage for All Inputs		
		54	-		0.7	.,		put LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Voltag	ge		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
Vон	Output HIGH Voltage	54	2.5	3.5		V		$_{H} = MAX, V_{IN} = V_{IH}$	
VOH	Output man voltage	74	2.7	3.5		V	or V _{IL} per Trut	h Table	
VOL Output LOW Voltage		54,74		0.25	0.4	V	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN,$	
	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA	V _{IN} = V _{IL} or V _{IH} per Truth Table	
	Input HIGH Current								
IH	Other Inputs				20 60	μΑ	V _{CC} = MAX, V	$I_{1N} = 2.7 \text{ V}$	
	Other Inputs				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V		
,	Input LOW Current	1							
IL	Other Inputs				-0.4 -1.2	mA	V _{CC} = MAX, V	$I_{1N} = 0.4 \text{ V}$	
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current				35	mA	V _{CC} = MAX		

AC CHARACTERISTICS: $T_A = 25$ °C

SYMBOL	DARAMETER		LIMITS		LINUTO	TEGT COMPLETIONS	
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
fMAX	Maximum Clock Frequency	20	25	1	MHz		
^t PLH ^t PHL	Propagation Delay, PL to Output Q		22 33	33 50	ns		
^t PLH ^t PHL	Data to Output Q		20 27	32 40	ns	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 15 \text{ pF}$	
^t PLH ^t PHL	Clock to RC		13 16	20 24	ns		
^t PLH ^t PHL	Clock to Output Q		16 24	24 36	ns		
^t PLH ^t PHL	Clock to TC		28 37	42 52	ns		
^t PLH ^t PHL	Ū/D to RC		30 30	45 45	ns		
[†] PLH [†] PHL	Ū/D to TC		21 22	33 33	ns		
^t PLH ^t PHL	CE to RC		21 22	33 33	ns		

AC SETUP REQUIREMENTS: $T_A = 25$ °C

SYMBOL	DADAMETED		LIMITS			TECT COMPLETIONS	
	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
tw	CP Pulse Width	25			ns		
t₩	PL Pulse Width	35			ns	V _{CC} = 5.0 V	
t _S	Data Setup Time	20			ns		
th	Data Hold Time	5.0			ns		
t _{rec}	Recovery Time	40			ns		

DEFINITIONS OF TERMS:

SETUP TIME (t_s) . is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

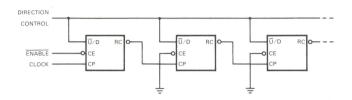


Fig. a) n-stage counter using ripple clock.

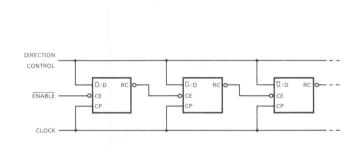


Fig. b) Synchronous n-stage counter using ripple carry/borrow.

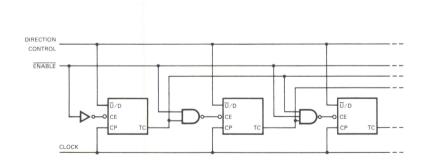


Fig. c) Synchronous n-stage counter with parallel gated carry/borrow.

AC WAVEFORMS

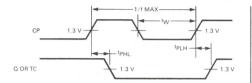
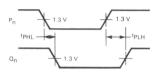


Fig. 1



NOTE: PL = LOW

Fig. 3

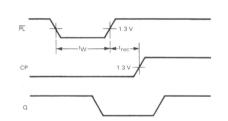


Fig. 5

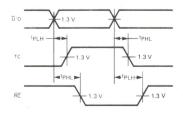


Fig. 7

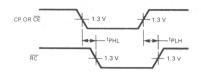


Fig. 2

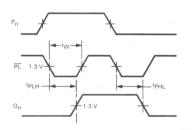
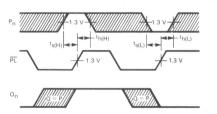


Fig. 4



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6

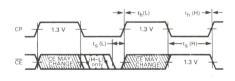


Fig. 8



DESCRIPTION — The SN54LS/74LS192 is an UP/DOWN BCD Decade (8421) Counter and the SN54LS/74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

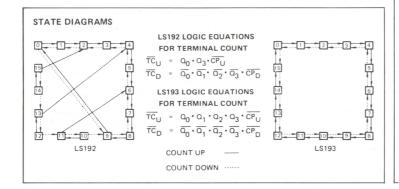
Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load $\overline{(PL)}$ and the Master Reset (MR) inputs asynchronously override the clocks.

- LOW POWER . . . 95 mW TYPICAL DISSIPATION
- HIGH SPEED . . . 40 MHz TYPICAL COUNT FREQUENCY
- SYNCHRONOUS COUNTING
- ASYNCHRONOUS MASTER RESET AND PARALLEL LOAD
- INDIVIDUAL PRESET INPUTS
- CASCADING CIRCUITRY INTERNALLY PROVIDED
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

PIN NA	AMES	LOADING (Note a)		
		HIGH	LOW	
CPU	Count Up Clock Pulse Input	0.5 U.L.	0.25 U.L.	
CPD	Count Down Clock Pulse Input	0.5 U.L.	0.25 U.L.	
MR	Asynchronous Master Reset (Clear) Input	0.5 U.L.	0.25 U.L.	
PL	Asynchronous Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.	
Pn	Parallel Data Inputs	0.5 U.L.	0.25 U.L.	
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5(2.5) U.L.	
TCD	Terminal Count Down (Borrow) Output (Note b)	10 U.L.	5(2.5) U.L.	
TCU	Terminal Count Up (Carry) Output (Note b)	10 U.L.	5(2.5) U.L.	

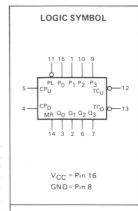
NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW
- b. The Output LOW drive factor is 2.5 U.L. for MILITARY (54) and 5 U.L. for COMMERCIAL (74) Temperature Ranges.

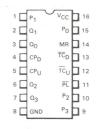


SN54LS/74LS192 SN54LS/74LS193

PRESETTABLE BCD/DECADE
UP/DOWN COUNTER
PRESETTABLE 4-BIT BINARY
UP/DOWN COUNTER
LOW POWER SCHOTTKY



CONNECTION DIAGRAM DIP (TOP VIEW)

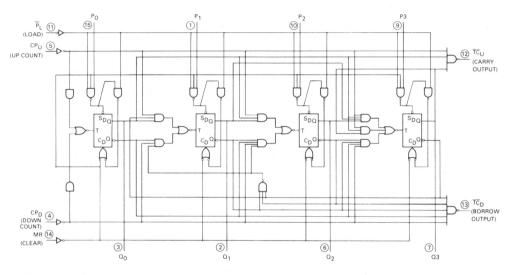


J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

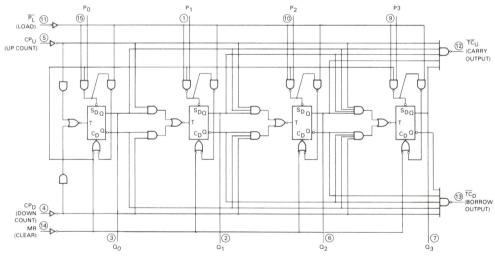
NOTE

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAMS



LS192



LS193

V_{CC} = Pin 16 GND = Pin 8

= Pin Number

FUNCTIONAL DESCRIPTION — The LS192 and LS193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous UP/DOWN (Reversable) Counters. The operating modes of the LS192 decade counter and the LS193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up (\overline{TC}_U) and Terminal Count Down (\overline{TC}_D) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the LS192, 15 for the LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the \overline{TC}_D output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load (\overline{PL}) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

MODE SELECT TABLE

MR	PL	CPU	CPD	MODE
Н	Х	X	X	Reset (Asyn.)
L	L	×	X	Preset (Asyn.)
L	Н	Н	Н	No Change
L	Н	1	Н	Count Up
L	Н	Н	1	Count Down

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMAROL	DADAMETER			LIMITS		LINUTC	TECT	ONDITIONS		
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST	ONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for		
		54			0.7	.,		ut LOW Voltage for		
VIL	Input LOW Voltage	74	,		0.8	V	All Inputs			
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN$, $I_{IN} = -18 \text{ mA}$			
VOH	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$		
		74	2.7	3.5		V	or V _{IL} per Truth Table			
.,	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$v_{CC} = v_{CC} \text{ MIN},$		
VOL		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table		
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V		
lн	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _I	N = 7.0 V		
l _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V		
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$			
lcc	Power Supply Current				34	mA	$V_{CC} = MAX$			

AC CHARACTERISTICS: $T_A = 25$ °C

CVMAROL	DADAMETED		LIMITS		LINUTO	TEGT CONDITIONS			
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS			
fMAX	Maximum Clock Frequency	25	32		MHz				
^t PLH ^t PHL	CPU Input to TCU Output		17 18	26 24	ns				
^t PLH ^t PHL	CPD Input to TCD Output		16 15	24 24	ns	V _{CC} = 5.0 V			
^t PLH ^t PHL	Clock to Q		27 30	38 47	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$			
^t PLH ^t PHL	PL to Q		24 25	40 40	ns				
^t PHL	MR Input to Any Output		23	35	ns				

AC SETUP REQUIREMENTS: $T_A = 25$ °C

SYMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS				
		MIN	TYP	MAX		TEST CONDITIONS				
tw	Any Pulse Width	20			ns					
ts	Data Setup Time	20			ns	V _{CC} = 5.0 V				
th	Data Hold Time	5.0	-		ns	100 0.0 1				
t _{rec}	Recovery Time	40			ns					

DEFINITIONS OF TERMS:

SETUP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the $\overline{\text{PL}}$ transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the $\overline{\text{PL}}$ transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the $\overline{\text{PL}}$ transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

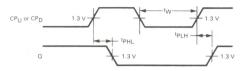


Fig. 1

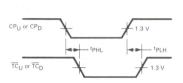


Fig. 2

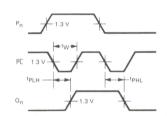
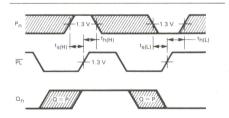
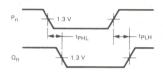


Fig. 4



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6



NOTE: PL = LOW

Fig. 3

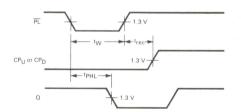


Fig. 5

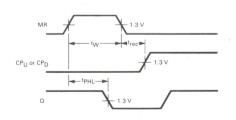


Fig. 7



DESCRIPTION — The SN54LS/74LS194A is a High Speed 4-Bit Bidirectional Universal Shift Register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The LS194A is similar in operation to the LS195A Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL families.

- TYPICAL SHIFT FREQUENCY OF 36 MHz
- ASYNCHRONOUS MASTER RESET
- HOLD (DO NOTHING) MODE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

PIN NAM	ES	LOADIN	G (Note a)
		HIGH	LOW
S ₀ , S ₁	Mode Control Inputs	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
DSR	Serial (Shift Right) Data Input	0.5 U.L.	0.25 U.L.
D _{SL}	Serial (Shift Left) Data Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES

- a. 1 TTL Unit Load (U.L.) = $40 \,\mu\text{A}$ HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54LS194A SN74LS194A

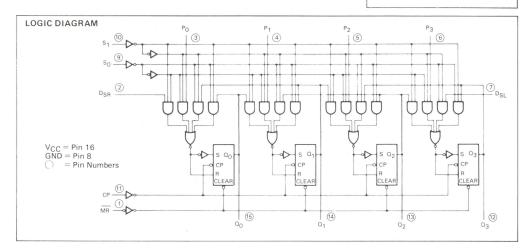
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

LOW POWER SCHOTTKY

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)



FUNCTIONAL DESCRIPTION — The Logic Diagram and Truth Table indicate the functional characteristics of the LS194A 4-Bit Bidirectional Shift Register. The LS194A is similar in operation to the Motorola LS195A Universal Shift Register when used in serial or parallel data register transfers. Some of the common features of the two devices are described below:

- 1. All data and mode control inputs are edge-triggered, responding only to the LOW to HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.
- 2. The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implementing very high speed CPUs, or the memory buffer registers.
- 3. The four parallel data inputs (P_0, P_1, P_2, P_3) are D-type inputs. When both S_0 and S_1 are HIGH, the data appearing on P_0, P_1, P_2 , and P_3 inputs is transferred to the Q_0, Q_1, Q_2 , and Q_3 outputs respectively following the next LOW to HIGH transition of the clock.
- 4. The asynchronous Master Reset (MR), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the LS194A design which increase the range of application are described below:

- 1. Two mode control inputs (S_0, S_1) determine the synchronous operation of the device. As shown in the Mode Selection Table, data can be entered and shifted from left to right (shift right, $\Omega_0 \rightarrow \Omega_1$, etc.) or right to left (shift left, $\Omega_3 \rightarrow \Omega_2$, etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both S_0 and S_1 are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH to LOW clock transition.
- 2. D-type serial data inputs (DSR, DSL) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

MODE SELECT - TRUTH TABLE

			INI	OUTPUTS						
OPERATING MODE	MR	S ₁	s ₀	DSR	DSL	Pn	σ0	Q ₁	02	03
Reset	L	×	×	×	X	×	L	L	L	L
Hold	Н	1	ı	×	×	×	90	91	q ₂	93
Shift Left	Н	h	1	×	1	×	91	92	q3	L
Shift Left	н	h	1	×	h	×	q ₁	92	q3	Н
Shift Right	Н	1	h	1	×	×	L	90	91	q ₂
Shirt Right	н	1	h	h	×	×	Н	90	91	92
Parallel Load	Н	h	h	×	×	pn	P ₀	P ₁	, P2	p ₃

L = LOW Voltage Level

H= HIGH Voltage Level

X = Don't Care

I = LOW voltage level one set-up time prior to the LOW to HIGH clock transition

h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition

 $p_{n}(q_{n})$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74	7		-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMETER			LIMITS		LINUTO	TECT	ONDITIONS		
SYMBOL	PARAMETER	(MIN	TYP	MAX	UNITS	TEST CONDITIONS			
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for		
		54			0.7			ut LOW Voltage for		
VIL	Input LOW Voltage	74			0.8	V	All Inputs			
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$			
Vон	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IF}$		
		74	2.7	3.5		V	or V _{IL} per Truth Table			
.,	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$		
VOL		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	VIN = VIL or VIH per Truth Table		
					20	μΑ	$V_{CC} = MAX, V_I$	N = 2.7 V		
lн	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _I	N = 7.0 V		
IL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _I	N = 0.4 V		
os	Short Circuit Current		-20		-100	mA	V _{CC} = MAX			
СС	Power Supply Current				23	mA	$V_{CC} = MAX$	- 1 1 1		

AC CHARACTERISTICS: $T_{\mbox{\scriptsize A}} = 25 \ensuremath{^{\circ}}\mbox{\scriptsize C}$

CVMPOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
SYMBOL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
fMAX	Maximum Clock Frequency	25	36		MHz	
^t PLH ^t PHL	Propagation Delay, Clock to Output		14 17	22 26	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
^t PHL	Propagation Delay, MR to Output		19	30	ns	

AC SETUP REQUIREMENTS: TA = 25°C

CVA ADOL	242445752		LIMITS		LIMITO	TEST CONDITIONS		
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS			
tw	Clock or MR Pulse Width	20			ns			
t _S	Mode Control Setup Time	30			ns			
t _s	Data Setup Time	20			ns	$V_{CC} = 5.0 V$		
th	Hold Time, Any Input	0			ns			
t _{rec}	Recovery Time	25			ns			

DEFINITIONS OF TERMS:

SET UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

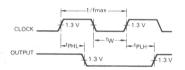
 ${\sf HOLD\,TIME}$ (${\sf th}$) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEVFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

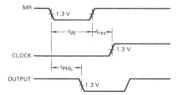
CLOCK TO OUTPUT DELAYS CLOCK PULSE WIDTH AND fmax



OTHER CONDITIONS: S1 = L, MR = H, S0 = H

Fig. 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



OTHER CONDITIONS: S_0 , $S_1 = H$ $P_0 = P_1 = P_2 = P_3 = H$

Fig. 2

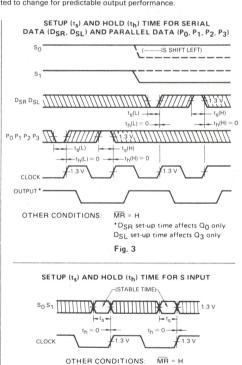


Fig. 4



DESCRIPTION — The SN54LS/74LS195A is a high speed 4-Bit Shift Register offering typical shift frequencies of 39 MHz. It is useful for a wide variety of register and counting applications. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

- TYPICAL SHIFT RIGHT FREQUENCY OF 39 MHz
- ASYNCHRONOUS MASTER RESET
- J. K INPUTS TO FIRST STAGE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

SN54LS195A SN74LS195A

UNIVERSAL 4-BIT SHIFT REGISTER

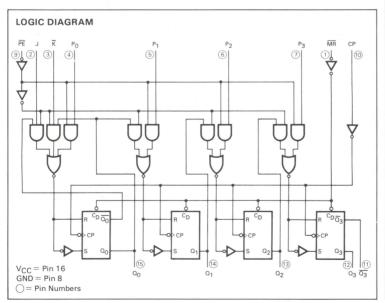
LOW POWER SCHOTTKY

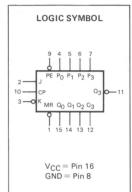
PIN NAMES	5	LOADING (Note a)				
		HIGH	LOW			
PE	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.			
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.			
J	First Stage J (Active HIGH) Input	0.5 U.L.	0.25 U.L.			
<u>J</u>	First Stage K (Active LOW) Input	0.5 U.L.	0.25 U.L.			
CP	Clock (Active HIGH Going Edge)					
	Input	0.5 U.L.	0.25 U.L.			
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.			
$\sigma_0 - \sigma_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.			
\bar{Q}_3	Complementary Last Stage Output	10 U.L.	5(2.5) U.L.			
	(Note b)		,			

NOTES:

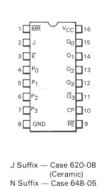
a. 1 TTL Unit Load (U.L.) = $40 \mu A HIGH/1.6 mA LOW$.

 The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.









NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

(Plastic)

FUNCTIONAL DESCRIPTION — The Logic Diagram and Truth Table indicate the functional characteristics of the LS195A 4-Bit Shift Register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The LS195A has two primary modes of operation, shift right $(Q_0 \rightarrow Q_1)$ and parallel load which are controlled by the state of the Parallel Enable (\overline{PE}) input. When the PE input is HIGH, serial data enters the first flip-flop Q_0 via the J and \overline{K} inputs and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW to HIGH clock transition. The \overline{JK} inputs provide the flexibility of the JK type input for special applications, and the simple D type input for general applications by tying the two pins together. When the \overline{PE} input is LOW, the LS195A appears as four common clocked D flip-flops. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs following the LOW to HIGH clock transition. Shift left operations $(Q_3 \rightarrow Q_2)$ can be achieved by tying the Q_0 outputs to the P_{n-1} inputs and holding the \overline{PE} input LOW.

All serial and parallel data transfers are synchronous, occurring after each LOW to HIGH clock transition. Since the LS195A utilizes edge-triggering, there is no restriction on the activity of the J, \overline{K} , P_n and \overline{PE} inputs for logic operation – except for the set-up and release time requirements.

A LOW on the asynchronous Master Reset (\overline{MR}) input sets all Q outputs LOW, independent of any other input condition.

MODE SELECT - TRUTH TABLE

	T											
OPERATING MODES		INPUTS						OUTPUTS				
OFERATING MODES	MR	PE	J	K	Pn	α ₀	Ω ₁	02	Ω3	$\bar{\mathbf{Q}}_3$		
Asynchronous Reset	L	X	×	X	X	L	L	L	L	Н		
Shift, Set First Stage	Н	h	h	h	Х	Н	q ₀	91	q ₂	q ₂		
Shift, Reset First Stage	Н	h	1	1	X	L	q ₀	q ₁	q_2	\overline{q}_2		
Shift, Toggle First Stage	H	h	h	1	X	q ₀	q ₀	q ₁	q_2	\overline{q}_2		
Shift, Retain First Stage	Н	h	- 1	h	X	90	q ₀	q ₁	q ₂	\overline{q}_2		
Parallel Load	Н	- 1	X	X	p _n	P ₀	p ₁	P ₂	p ₃	p ₃		

L = LOW voltage levels

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lor	Output Current — Low	54 74			4.0 8.0	mA

H = HIGH voltage levels

X = Don't Care

I = LOW voltage level one set-up time prior to the LOW to HIGH clock transition.

h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition.

 $p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the$

LOW to HIGH clock transition.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS			
SYMBOL	PARAIVIETER	FARAIVIETER		TYP	MAX	UNITS	TEST CONDITIONS			
VIH	Input HIGH Voltage		Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
		54			0.7	.,		put LOW Voltage for		
VIL	Input LOW Voltage	74			0.8	V	All Inputs			
VIK	Input Clamp Diode Volt	age	1 4	-0.65	-1.5	V	$V_{CC} = MIN$, $I_{IN} = -18 \text{ mA}$			
VOH	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{OH}$ or V_{IL} per Truth Table			
VОН		74	2.7	3.5		V				
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$		
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table		
					20	μΑ	$V_{CC} = MAX, V$	/ _{IN} = 2.7 V		
lН	Input HIGH Current				0.1	mA	V _{CC} = MAX, V	/ _{IN} = 7.0 V		
IIL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V	/IN = 0.4 V		
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$			
lcc	Power Supply Current				21	mA	$V_{CC} = MAX$			

AC CHARACTERISTICS: $T_A = 25$ °C

SYMBOL	PARAMETER		LIMITS			TECT CONDITIONS
		MIN	TYP	MAX	UNITS	TEST CONDITIONS
fMAX	Maximum Clock Frequency	30	39		MHz	
^t PLH ^t PHL	Propagation Delay Clock to Output		14 17	22 26	ns	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 15 \text{ pF}$
^t PHL	Propagation Delay MR to Output		19	30	ns	, , ,

AC SETUP REQUIREMENTS: $T_A = 25$ °C

CVMBOL	PARAMETER		LIMITS		UNITS	TEST COMPITIONS		
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
t₩	CP Clock Pulse Width	16			ns			
tw	MR Pulse Width	12			ns			
t _S	PE Setup Time	25			ns	V _{CC} = 5.0 V		
t _S	Data Setup Time	15			ns	VCC = 3.0 V		
t _{rec}	Recovery Time	25			ns			
t _{rel}	PE Release Time			10	ns			
th	Data Hold Time	0			ns			

SETUP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (th) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (tren) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH data to the Q outputs.

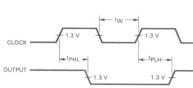
AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance,

CLOCK TO OUTPUT DELAYS

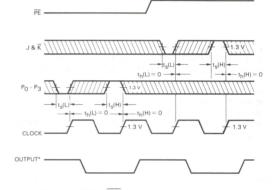
AND CLOCK PULSE WIDTH

SETUP (\underline{t}_s) AND HOLD (t_h) TIME FOR SERIAL DATA (J & K) AND PARALLEL DATA (Po, P1, P2, P3)



CONDITIONS: $J = \overline{PE} = \overline{MR} = H$ $\overline{K} = L$

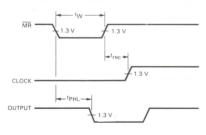
Fig. 1



CONDITIONS: MR = H *J and $\overline{\mathsf{K}}$ set-up time affects Q_0 only

Fig. 2

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

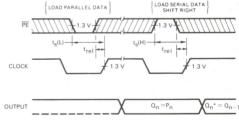


 $P_0 = P_1 = P_2 = P_3 = H$

CONDITIONS: PE = L

Fig. 3

SETUP (t_s) AND HOLD (t_h) TIME FOR \overline{PE} INPUT



CONDITIONS: $\overline{MR} = H$ *Q_0 state will be determined by J and \overline{K} inputs

Fig. 4



DESCRIPTION — The SN54LS/74LS196 decade counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8,4,2,1) sequence or in a bi-quinary mode producing a 50% duty cycle output. The SN54LS/74LS197 contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. Low Power Schottky technology is used to achieve typical count rates of 70 MHz and power dissipation of only 80 mW.

Both circuit types have a Master Reset (\overline{MR}) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input (\overline{PL}) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when \overline{PL} is LOW and storing the data when \overline{PL} is HIGH.

- LOW POWER CONSUMPTION TYPICALLY 80 mW
- HIGH COUNTING RATES TYPICALLY 70 MHz
- CHOICE OF COUNTING MODES BCD, BI-QUINARY, BINARY
- ASYNCHRONOUS PRESETTABLE
- ASYNCHRONOUS MASTER RESET
- EASY MULTISTAGE CASCADING
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

PIN NAMES

		,
	HIGH	LOW
Clock (Active LOW Going Edge)	1.0 U.L.	1.5 U.L.
Clock (Active LOW Going Edge)	2.0 U.L.	1.75 U.L.
Clock (Active LOW Going Edge) Input to Divide-by-Eight Section	1.0 U.L.	0.8 U.L.
Master Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
Data Inputs Outputs (Notes b, c)	0.5 U.L. 10 U.L.	0.25 U.L. 5(2.5) U.L.
	Input to Divide-by-Two Section Clock (Active LOW Going Edge) Input to Divide-by-Five Section Clock (Active LOW Going Edge) Input to Divide-by-Eight Section Master Reset (Active LOW) Input Parallel Load (Active LOW) Input Data Inputs	Clock (Active LOW Going Edge) Input to Divide-by-Two Section Clock (Active LOW Going Edge) Input to Divide-by-Five Section Clock (Active LOW Going Edge) Input to Divide-by-Fight Section Master Reset (Active LOW) Input Parallel Load (Active LOW) Input Data Inputs 1.0 U.L. 0.5 U.L. 0.5 U.L.

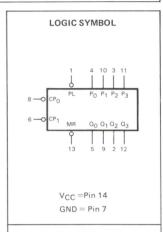
NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
- c. In addition to loading shown, Q $_0$ can also drive $\overline{\text{CP}}_1$

SN54LS/74LS196 SN54LS/74LS197

4-STAGE PRESETTABLE RIPPLE COUNTERS

LOW POWER SCHOTTKY



CONNECTION DIAGRAM DIP (TOP VIEW)



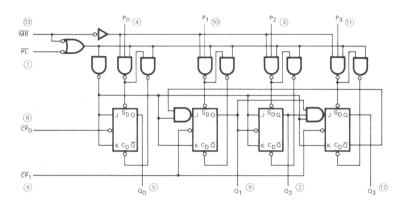
J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

NOTE

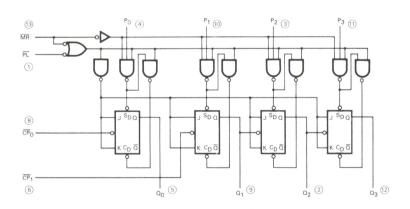
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOADING (Note a)

LOGIC DIAGRAM



LS196



LS197

$$V_{CC} = Pin 14$$
 $GND = Pin 7$
 O = Pin Numbers

FUNCTIONAL DESCRIPTION — The LS196 and LS197 are asynchronously presettable decade and binary ripple counters. The LS196 Decade Counter is partitioned into divide-by-two and divide-by-five sections while the LS197 is partitioned into divide-by-two and divide-by-two and divide-by-two and divide-by-two and divide-by-two and divide-by-two and divide-by-two and divide-by-two and divide-by-two and divide-by-two and divide-by-two and divide-by-two and divide-by-tipped sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH to LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{\text{CP}_0}$ input serves the Q₀ flip-flop in both circuit types while the $\overline{\text{CP}_1}$ input serves the divide-by-five or divide-by-eight section. The Q₀ output is designed and specified to drive the rated fan-out plus the $\overline{\text{CP}_1}$ input. With the input frequency connected to $\overline{\text{CP}_0}$ and Q₀ driving $\overline{\text{CP}_1}$, the LS197 forms a straightforward module-16 counter, with Q₀ the least significant output and Q₃ the most significant output.

The LS196 Decade Counter can be connected up to operate in two different count sequences, as indicated in the tables of Figure 2. With the input frequency connected to $\overline{\text{CP}_0}$ and with Ω_0 driving $\overline{\text{CP}_1}$, the circuit counts in the BCD (8, 4, 2, 1) sequence. With the input frequency connected to $\overline{\text{CP}_1}$ and Ω_3 driving $\overline{\text{CP}_0}$, Ω_0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The LS196 and LS197 have an asynchronous active LOW Master Reset input (MR) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input (PL) overrides the clock inputs and loads the data from Parallel Data (P0—P3) inputs into the flip-flops. While PL is LOW, the counters act as transparent latches and any change in the $P_{\rm D}$ inputs will be reflected in the outputs.

Figure 2: LS196 COUNT SEQUENCES

	DECA	DE (NOTE 1)			BI-QUIN	NARY (NOTE	2)	
COUNT	03	02	Ω ₁	Ω0	COUNT	Ω ₀	03	02	Q ₁
0	L	L	L	L	0	L	L	L	L
1	L	L	L	н	1	L	L	L	Н
2	L	L	Н	L	2	L	L	Н	L
3	L	L	Н	H	3	L	L	Н	Н
4	L	Н	L	L	4	L Z	Н	L	L
5	L	Н	L	Н	5	н	L	L	L
6	L	Н	Н	L	6	н	L	L	Н
7	L	H	Н	Н	7	н	r L	Н	L
8	Н	L	L	L	8	н	L	Н	Н
9	н	L	L	н	9	Н	Н	L	L

NOTES:

- Signal applied to CP₀, Q₀ connected to CP₁.
- 2. Signal applied to CP₁, Q₃ connected to CP₀.

MODE SELECT TABLE

	INPUTS	DESCRIPTION											
MR	MR PL	CP	RESPONSE										
L	×	X	Reset (Clear)										
Н	L	X	Parallel Load										
Н	н	l l	Count										

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

= HIGH to Low Clock Transition

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
OL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS		
SYMBOL	PARAMETER	11.7	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for	
1/	I	54			0.7			put LOW Voltage for	
V _{IL}	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _I N	$_{\rm N} = -18 \; {\rm mA}$	
Voн	Output HIGH Voltage	54	2.5	3.5		V		$_{H} = MAX, V_{IN} = V_{IH}$	
*On	Output more voltage	74	2.7	3.5		V	or V _{IL} per Trut	h Table	
	0	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN$	
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA	V _{IN} = V _{IL} or V _{IH} per Truth Table	
I _I н	Input HIGH <u>Current</u> Data, <u>PL</u> MR, <u>CP₀ (LS196)</u> MR, <u>CP₀, CP₁ (LS197)</u> <u>CP₁ (LS196)</u>				20 40 40 80	μΑ	V _{CC} = MAX, V	7 _{IN} = 2.7 V	
1111	Data, PL MR, CP ₀ (LS196) MR, CP ₀ , CP ₁ (LS197) CP ₁ (LS196)				0.1 0.2 0.2 0.4	mA	V _{CC} = MAX, V _{IN} = 7.0 V		
^I IL	Input LOW Current Data, PL MR CPO CP1 (LS196) CP1 (LS197)				-0.4 -0.8 -2.4 -2.8 -1.3	mA	V _{CC} = MAX =	V _{IN} = 0.4 V	
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current				27	mA	V _{CC} = MAX		

AC CHARACTERISTICS: TA = 25°C

CVAADOL	DADAMETED			LIN	1ITS			UNITS	TEST CONDITIONS
SYMBOL	PARAMETER		LS196	L		LS197		UNITO	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
fMAX	Maximum Clock Frequency	30	40		30	40		MHz	
^t PLH ^t PHL	CP _O Input to Q _O Output		8.0 13	15 20		8.0 14	15 21	ns	
^t PLH ^t PHL	CP ₁ Input to Q ₁ Output		16 22	24 33		12 23	19 35	ns	
^t PLH ^t PHL	CP ₁ Input to Q ₂ Output		38 41	57 62		34 42	51 63	ns	V _{CC} = 5.0 V
tPLH tPHL	CP ₁ Input to Q ₃ Output		12 30	18 45		55 63	78 95	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
tPLH tPHL	Data to Output		20 29	30 44		18 29	27 44	ns	
tPLH tPHL	PL Input to Any Output		27 30	41 45		26 30	39 45	ns	
t _{PHL}	MR Input to Any Output		34	51		34	51	ns	

AC SETUP REQUIREMENTS: TA = 25°C

CVMDOL	DARAMETER			LIN	/ITS			UNITS	TEST CONDITIONS	
SYMBOL	PARAMETER	LS196			LS197			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX			
tw	CPO Pulse Width	20			20			ns		
tW	CP ₁ Pulse Width	30			30			ns		
tw	PL Pulse Width	20			20			ns		
tw	MR Pulse Width	15			15			ns		
t _S	Data Input Setup Time — HIGH	10			10			ns	V _{CC} = 5.0 V	
t _S	Data Input Setup Time — LOW	15			15			ns		
th	Data Hold Time — HIGH	t _W (PL)			t _W (PL)			ns		
th	Data Hold Time — LOW	t _W (PL)	1		t _W (PL)			ns		
t _{rec}	Recovery Time	30			30			ns		

DEFINITIONS OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

 $HOLD\ TIME\ (t_h)-is\ defined\ as\ the\ minimum\ time\ following\ the\ clock\ transition\ from\ HIGH\ to\ LOW\ that\ the\ logic\ level\ must\ be\ maintained\ at\ the\ input\ in\ order\ to\ ensure\ continued\ recognition.\ A\ negative\ HOLD\ TIME\ indicates\ that\ the\ correct\ logic\ level\ may\ be\ released\ prior\ to\ the\ clock\ transition\ from\ HIGH\ to\ LOW\ and\ still\ be\ recognized.$

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer LOW Data to the Q outputs.

AC WAVEFORMS

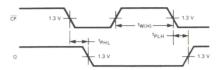
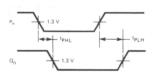


Fig. 1



NOTE: PL = LOW

Fig. 2

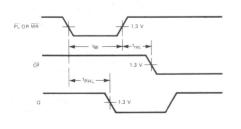


Fig. 4

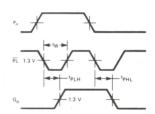
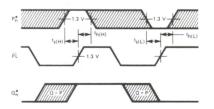


Fig. 3



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 5



DESCRIPTION — Each multivibrator of the LS221 features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

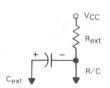
Pulse triggering occurs at a voltage level and is not related to the transition time of the input pulse. Schmitt-trigger input circuitry for B input allows jitter-free triggering for inputs as slow as 1 volt/second, providing the circuit with excellent noise immunity. A high immunity to VCC noise is also provided by internal latching circuitry.

Once triggered, the outputs are independent of further transitions of the inputs and are a function of the timing components. The output pulses can be terminated by the overriding clear. Input pulse width may be of any duration relative to the output pulse width. Output pulse width may be varied from 35 nanoseconds to a maximum of 70 s by choosing appropriate timing components. With $R_{\mbox{ext}}=2~k\Omega$ and $C_{\mbox{ext}}=0$, a typical output pulse of 30 nanoseconds is achieved. Output rise and fall times are independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for greater than six decades of timing capacitance (10pF to 10 μF), and greater than one decade of timing resistance (2 to 70 k Ω for the SN54LS221, and 2 to 100 k Ω for the SN74LS221). Pulse width is defined by the relationship: tw/out) = $C_{ext}R_{ext}$ in 2 ≈ 0.7 $C_{ext}R_{ext}$. If pulse cutoff is not critical, capacitance up to 1000 μF and resistance as low as 1.4 k Ω may be used. The range of jitter-free pulse widths is extended if V_{CC} is 5 V and 25°C temperature.

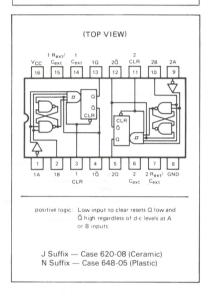
- SN54LS221 and SN74LS221 IS A DUAL HIGHLY STABLE ONE-SHOT
- OVERRIDING CLEAR TERMINATES OUTPUT PULSE
- PIN OUT IS IDENTICAL TO SN54LS/74LS123



SN54LS221 SN74LS221

DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

LOW POWER SCHOTTKY



FUNCTION TABLE

(EACH MONOSTABLE)

IN	PUTS	OUTPUTS		
CLEAR	Α	В	Q	ā
L	X	Х	L	Н
×	Н	X	L	Н
×	X	L	L	Н
H	L	1	Л	T
H	1	н.	л	T
1	L	Н	Л	П

TYPE	TYPICAL POWER DISSIPATION	MAXIMUM OUTPUT PULSE LENGTH
SN54LS221	23 mW	49 s
SN74LS221	23 mW	70 s

Once in the pulse trigger mode, the output pulse width is determined by $t_W = R_{ext} C_{ext} \ln 2$, as long as R_{ext} and C_{ext} are within their minimum and maximum valves and the duty cycle is less than 50%. This pulse width is essentially independent of V_{CC} and temperature variations. Output pulse widths varies typically no more than $\pm 0.5\%$ from device to device.

If the duty cycle, defined as being $100^{\bullet} \frac{\text{tW}}{\text{T}}$ where T is the period of the input pulse, rises above 50%, the output pulse width will

become shorter. If the duty cycle varies between low and high valves, this causes the output pulse width to vary in length, or jitter. To reduce jitter to a minimum, R_{ext} should be as large as possible. (Jitter is independent of C_{ext}). With $R_{ext} = 100$ K, jitter is not appreciable until the duty cycle approaches 90%.

Although the LS221 is pin-for-pin compatible with the LS123, it should be remembered that they are not functionally identical. The LS123 is retriggerable so that the output is dependent upon the input transitions once it is high. This is not the case for the LS221. Also note that it is recommended to externally ground the LS123 C_{ext} pin. However, this cannot be done on the LS221.

The SN54LS/74LS221 is a dual, monolithic, non-retriggerable, high-stability one shot. The output pulse width, two can be varied over 9 decades of timing by proper selection of the external timing components, Rext and Cext.

Pulse triggering occurs at a voltage level and is, therefore, independent of the input slew rate. Although all three inputs have this Schmitt-trigger effect, only the B input should be used for very long transition triggers ($\geqslant 1.0 \,\mu\text{V/s}$). High immunity to V_{CC} noise (typically 1.5 V) is achieved by internal latching circuitry. However, standard V_{CC} bypassing is strongly recommended.

The LS221 has four basic modes of operation.

Clear Mode: If the clear input is held low, irregardless of the previous output state and other input states, the Q output is low.

Inhibit Mode: If either the A input is high or the B input is low, once the Q output goes low, it cannot be retriggered by other

inputs.

Pulse Trigger

Mode:

This occurs when none of the other modes are in effect and the Q output is low. A proper transition by either the CLR, A or B input, as shown in the truth table, will cause the Q output to go high and remain high for the pulse time tw.

Once triggered, as long as the output remains high, all input transitions (except for Clear, see Note 4) are ignored.

Overriding

Clear Mode: If the Q output is high, it may be forced low by bringing the clear input low.

SYMBOL	PARAMETER	-	MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	. 5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ЮН	Output Current — High	54,74			-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS	
SYMBOL	- PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{T+}	Positive-Going Threshold Voltage at A Input			1.0	2.0	V	V _{CC} = MIN	
V _T _	Negative-Going Threshold	54	0.7	1.0		V		
*	Voltage at A Input	74	0.8	1.0		V	V _{CC} = MIN	
V_{T+}	Positive-Going Threshold Voltage at B Input			1.0	2.0	V	V _{CC} = MIN	
V _T _	Negative-Going Threshold	54	0.7	0.9		V		
*	Voltage at B Input	74	0.8	0.9		V	V _{CC} = MIN	
VIK	Input Clamp Voltage				-1.5	V	$V_{CC} = MIN$, $I_{IN} = -18 \text{ mA}$	
Vон	Output HIGH Voltage	54	2.5	3.4		V	V _{CC} = MIN, I _{OH} = MAX	
VОН	Output Hight Voltage	74	2.7	3.4		V	VCC = WINV, TOH = WAX	
VOL	Output LOW Voltage	54		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = MIN$	
VOL	Output LOVV Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA	
Iн	Input HIGH Current				20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$	
чн	input marr current				0.1	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$	
I _{IL}	Input LOW Current Input A Input B Clear				-0.4 -0.8 -0.8	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$	
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
^I CC	Power Supply Current Quiescent			4.7	11	mA	$V_{CC} = MAX$	
.00	Triggered			19	27		100	

ac characteristics: $v_{CC} = 5.0 \text{ V}$, $t_A = 25^{\circ}\text{C}$

SYMBOL	FROM	TO		LIMITS		UNIT	TE	ST CONDITIONS
STIVIBUL	(INPUT)	(OUTPUT)	MIN	TYP	MAX	UNIT	TES	ST CONDITIONS
^t PLH	А	Q		45	70	ns		
YPLH	В	Q		35	55	110		
[†] PHL	А	ā		50	80	ns		$C_{\text{ext}} = 80 \text{ pF}, R_{\text{ext}} = 2 \text{ k}\Omega$
PHL	В	ā		40	65	113		Cext OO pr , riext - 2 ks2
tPHL	Clear	Q		35	55	ns	C _L =15 pF,	
^t PLH	Clear	ā		44	65	ns		
			70	120	150		See Figure 1	$C_{ext} = 80 pF, R_{ext} = 2 \Omega$
tW(out)	A or B	Q or \overline{Q}	20	47	70	ns	20.00	$C_{ext} = 0$, $R_{ext} = 2 k\Omega$
·vv(out)	7.51 B	2 51 4	600	670	750			$C_{ext} = 100 \text{ pF}, R_{ext} = 10 \text{ k}\Omega$
			6	6.9	7.5	ms		$C_{\text{ext}} = 1 \mu \text{F}, R_{\text{ext}} = 10 \text{k}\Omega$

AC SETUP REQUIREMENTS $V_{CC} = 5.0 \text{ V}, T_A = 25^{\circ}\text{C}$

CVAADOL	DADAMETER	PARAMETER				UNITS
SYMBOL	PARAMETER	PARAIVIETER				
dv/dt	Rate of Rise or Fall of Input Pulse					
	Sch	mitt, B	1.0			V/s
	Logic I	nput, A	1.0			V/μs
tw	Input Pulse Width					
	A or B	A or B, t _{W(in)} Clear, t _W (clear)				ns
	Clear, t _M					1.0
t _S	Clear-Inactive-State Setup Time		15			ns
R _{ext}	External Timing Resistance	54	1.4		70	kΩ
''ext	External filling hesistance	74	1.4		100	K12
C _{ext}	External Timing Capacitance		0	80	1000	μF
	Output Duty Cycle					
	RT =	$RT = 2.0 \text{ k}\Omega$			50	%
	$R_T = MA$	X R _{ext}			90	,,,

AC WAVEFORMS

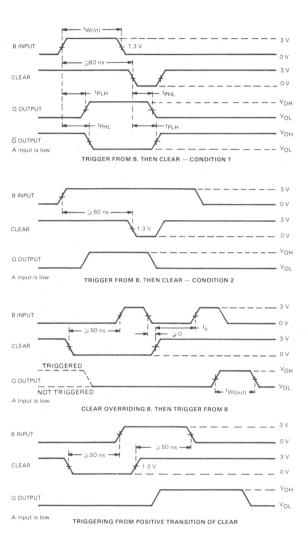


Fig. 1



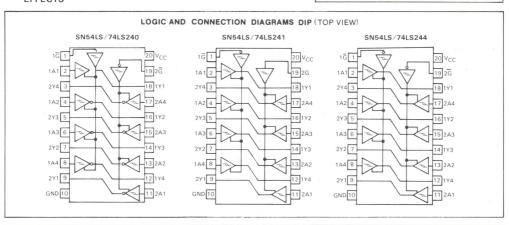
DESCRIPTION — The SN54LS/74LS240, 241 and 244 are Octal Buffers and Line Drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density.

- HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGINS
- 3-STATE OUTPUTS DRIVE BUS LINES OR BUFFER MEMORY ADDRESS REGISTERS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION **EFFECTS**

SN54LS/74LS240 SN54LS/74LS241 SN54LS/74LS244

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY



TRUTH TABLES

SN54LS/74LS240

INPL	JTS	QUITBUIT
1Ğ,2Ğ	D	OUTPUT
L	L	н
L	н	L
Н	Χ	(Z)

SN54LS/74LS244

INP	JTS	QUITDUT
1G,2G	D	OUTPUT
L	L	L
L	н	Н
Н	Х	(Z)

SN54LS/74LS241

INP	UTS	QUITBUIT	INP	UTS	OUTBUT				
1Ġ	D	OUTPUT	2G	D	OUTPUT				
L L H	L H X	L H (Z)	H	L H X	L H (Z)				

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = HIGH Impedance

J Suffix — Case 732-03 (Ceramic) N Suffix - Case 738-01 (Plastic)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74	_ = x		-3.0	mA
		54 74			-12 -15	mA
lor	Output Current — Low	54 74			12 24	mA

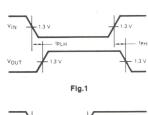
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

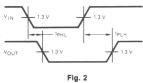
SYMBOL	PARAMET	ED		LIMITS	4.1	UNITS	TEST CONDITIONS	
STIVIBUL	PANAIVIET	-n	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
VIH	Input HIGH Voltage	Input HIGH Voltage				V	Guaranteed Input HIGH Voltage for All Inputs	
		54			0.7	.,	Guaranteed Input LOW Voltage for	
V _{IL}	Input LOW Voltage	74			0.8	V	All Inputs	
$V_{T+}-V_{T-}$	Hysteresis	•	0.2	0.4		V	V _{CC} = MIN	
VIK	Input Clamp Diode Vo	ltage		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$	
Voн	Output HIGH Voltage	54,74	2.4	3.4		V	$V_{CC} = MIN$, $I_{OH} = -3.0 \text{ mA}$	
ОП	output man voltage	54,74	2.0			V	V _{CC} = MIN, I _{OH} = MAX	
		54,74		0.25	0.4	V	I _{OL} = 12 mA V _{CC} = V _{CC} MIN,	
VOL	OL Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 24 mA V _{IN} = V _{IL} or V _{IH} per Truth Table	
lozh	Output Off Current H	GH			20	μΑ	$V_{CC} = MAX, V_{OUT} = 2.4 V$	
lozL	Output Off Current LO	WC			-20	μΑ	$V_{CC} = MAX, V_{OUT} = 0.4 V$	
					20	μΑ	$V_{CC} = MAX, V_{IN} = 2.7 V$	
lн	Input HIGH Current				0.1	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$	
ΊL	Input LOW Current		- 1		-0.2	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$	
los	Output Short Circuit	Current	-40		-225	mA	V _{CC} = MAX	
	Power Supply Curre Total, Output HIGH	nt			27			
lcc	Total, Output LOW	LS240			44		$V_{CC} = MAX$	
		LS241/244			46	mA	ACC - INIAX	
	Total at HIGH Z	LS240			50			
		LS241/244			54			

AC CHARA	CTFRISTICS:	$T_A = 25^{\circ}C$	Vcc = 50 V

CVAADOL	DADAMETED		LIMITS		LINUTC	TEST COMPLETIONS	
SYMBOL PARAMETER	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
tPLH tPHL	Propagation Delay, Data to Output LS240		9.0 12	14 18	ns		
^t PLH ^t PHL	Propagation Delay, Data to Output		12 12	18 18	ns	$C_L = 45 \text{ pF},$ $R_L = 667 \Omega$	
^t PZH	Output Enable Time to HIGH Level		15	23	ns		
tPZL	Output Enable Time to LOW Level		20	30	ns		
tPLZ	Output Disable Time from LOW Level		15	25	ns	$C_L = 5.0 \text{ pF}$	
tPHZ	Output Disable Time from HIGH Level		10	18	ns	$R_L = 667 \Omega$	

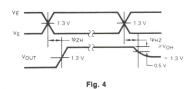
AC WAVEFORMS





1.3 V VOUT 1.3 V

Fig. 3



TO OUTPUT UNDER TEST

SWITCH POSITIONS

SW1	SW2
Open	Closed
Closed	Open
Closed	Closed
Closed	Closed
	Open Closed Closed

Fig. 5



DESCRIPTION — The SN54LS/74LS242 and SN54LS/74LS243 are Quad Bus Transmitters/Receivers designed for 4-line asynchronous 2-way data communications between data buses.

- HYSTERISIS AT INPUTS TO IMPROVE NOISE IMMUNITY
- 2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

TRUTH TABLES

SN54LS/74LS242

INP	UTS	ОИТРИТ		INP	UTS	OUTPUT	
GAB	D	001701		GAB	D	OUTPUT	
III	L H X	H L (Z)		H	X L H	(Z) H L	

SN54LS/74LS243

INP	UTS	QUITDUIT	INP	UTS	OUTPUT	
GAB	D	OUTPUT	GAB	D	OUTPUT	
L L H	L H X	H (Z)	H H	X L H	(Z) L H	

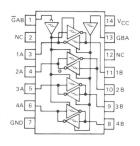
SN54LS/74LS242 SN54LS/74LS243

QUAD BUS TRANSCEIVER

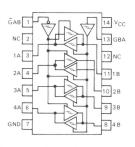
LOW POWER SCHOTTKY



SN54LS/74LS242



SN54LS/74LS243



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

NOTE:

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedence

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-3.0	mA
		54 74	,		-12 -15	mA
loL	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMBOL	DADAMETE			LIMITS		UNITS	TEST CONDITIONS				
SYMBOL VIH VIL VT+ — VT- VIK VOH	PARAMETER	1	MIN	TYP	MAX	UNITS	TEST CONDITIONS				
VIH	Input HIGH Voltage		2.0			٧	Guaranteed Input HIGH Voltage for All Inputs				
.,		54			0.7		Guaranteed Input LOW Voltage for				
VIL	Input LOW Voltage	74			0.8	V	All Inputs				
$V_{T+} - V_{T-}$	Hysteresis		0.2	0.4		V	V _{CC} = MIN				
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$				
Vоц	Output HIGH Voltage	54,74	2.4	3.4		V	V _{CC} = MIN I _{OH} = -3.0 mA				
·OH	Output Thier Voltage	54,74	2.0			V	$V_{CC} = MIN$, $I_{OH} = MAX$				
	0	54,74		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN},$				
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 24 mA V _{IN} = V _{IL} or V _{IH} per Truth Table				
lozh	Output Off Current HIG	rrent HIGH			40	μΑ	$V_{CC} = MAX, V_{OUT} = 2.4 V$				
lozL	Output Off Current LOV	N			μΑ	$V_{CC} = MAX, V_{OUT} = 0.4 V$					
		D, \bar{E}_1 , E_2			20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$				
IIH	Input HIGH Current	Ē ₁ , E ₂			0.1	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$				
		D Input			0.1	mA	$V_{CC} = MAX, V_{IN} = 5.5 V$				
ΊL	Input LOW Current				-0.2	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$				
los	Output Short Circuit Cu	ırrent	-40		-225	mA	V _{CC} = MAX				
	Power Supply Current Total, Output HIGH	t			38	-64	7 72				
CC	Total, Output LOW				50	mA	V _{CC} = MAX				
	Total at HIGH Z	LS242			50						
	Total at FIGH Z	LS243			54						

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER			LIIV	1ITS		UNITS	TEST CONDITIONS			
STIVIBUL	PARAMETER	LS242				LS243		UNITS	TEST CONDITIONS		
	v * ;	MIN	TYP	MAX	MIN	TYP	MAX				
^t PLH ^t PHL	Propagation Delay, Data to Output		9.0 12	14 18		12 12	18 18	ns	$C_L = 45 \text{ pF}$		
^t PZH	Output Enable Time to HIGH Level		15	23		15	23	ns	$R_L = 667 \Omega$		
tPZL	Output Enable Time to LOW Level		20	30		20	30	ns			
^t PLZ			15	25		15	25	ns	$C_{L} = 5.0 pF$		
^t PHZ			Output Disable Time from HIGH Level	evel 10	10	18		10	18	ns	$R_L = 667 \Omega$

AC WAVEFORMS

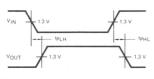


Fig.1

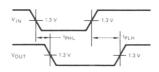


Fig. 2

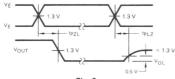
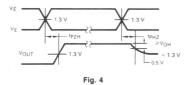


Fig. 3



TO OUTPUT UNDER TEST SW2

SWITCH POSITIONS

SYMBOL	SW1	SW2		
tPZH	Open	Closed		
tPZL	Closed	Open		
tPLZ	Closed	Closed		
t _{PHZ}	Closed	Closed		

Fig. 5



DESCRIPTION — The SN54LS/74LS245 is an Octal Bus Transmitter/ Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DR) controls transmission of Data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input (\overline{E}) can be used to isolate the buses.

- HYSTERESIS INPUTS TO IMPROVE NOISE IMMUNITY
- 2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION
- INPUT DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

TRUTH TABLE

INP	UTS	
G	DIR	OUTPUT
L	L H X	Bus B Data to Bus A Bus A Data to Bus B Isolation

H = HIGH Voltage Level

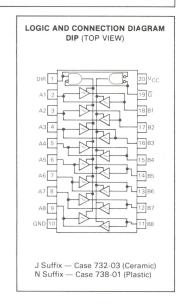
L = LOW Voltage Level

X = Immaterial

SN54LS245 SN74LS245

OCTAL BUS TRANSCEIVER

LOW POWER SCHOTTKY



D OI EILAINIG ILAIGEO					
PARAMETER		MIN	TYP	MAX	UNIT
Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
Output Current — High	54,74			-3.0	mA
	54 74			-12 -15	mA
Output Current — Low	54 74			12 24	mA
	PARAMETER Supply Voltage Operating Ambient Temperature Range Output Current — High	PARAMETER Supply Voltage 54 74 74 Operating Ambient Temperature Range 54 74 74 Output Current — High 54,74 54 74 Output Current — Low 54	PARAMETER	PARAMETER	PARAMETER MIN TYP MAX Supply Voltage 54 4.5 5.0 5.5 74 4.75 5.0 5.25 Operating Ambient Temperature Range 54 -55 25 125 74 0 25 70 Output Current — High 54,74 -3.0 54 -12 -15 Output Current — Low 54 12

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMAROL	PARAME	TED		LIMITS		UNITS	TEST C	ONDITIONS		
V _{IL} I _I V _{T+-V_T- F} V _{IK} I _I V _{OH} C C C C C C C C C	PARAIVIE	IER	MIN	TYP	MAX	UNITS	TEST C	ONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp	ut HIGH Voltage for		
		54			0.7		Guaranteed Input LOW Voltage for			
VIH I VIL I VT+-VT- F VIK I VOH (VOL (IOZH IOZL (I)IH I	Input LOW Voltage	74				V	All Inputs			
$V_{T+}-V_{T-}$	Hysteresis	'	0.2	0.4		V	V _{CC} = MIN			
VIK	Input Clamp Diode Vo	Itage		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN}$	= -18 mA		
Vон	Output HIGH Voltage	54,74	2.4	3.4		V	V _{CC} = MIN, I _{OF}	$_{\rm H} = -3.0 \; {\rm mA}$		
топ	Output man voltage	54,74	2.0			V	V _{CC} = MIN, I _O	~ A \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\		
		54,74		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$	$V_{CC} = V_{CC} MIN,$		
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 24 mA	VIN = VIL or VIH per Truth Table		
lozh	Output Off Current HI	GH			20	μΑ	V _{CC} = MAX, V _{OUT} = 2.4 V			
lozL	Output Off Current LC)W			-200	μΑ	V _{CC} = MAX, V _C	OUT = 0.4 V		
		A or B, DR or $\overline{\mathbb{E}}$			20	μΑ	$V_{CC} = MAX, V_{II}$	N = 2.7 V		
lін	Input HIGH Current	put HIGH Current DR or E			0.1	mA	V _{CC} = MAX, V _{II}	N = 7.0 V		
OZL		A or B			0.1	mA	V _{CC} = MAX, V _I	N = 5.5 V		
IIL	Input LOW Current				-0.2	mA	$V_{CC} = MAX, V_{II}$	N = 0.4 V		
los	Output Short Circuit C	urrent	-40		-225	mA	$V_{CC} = MAX$			
	Power Supply Currer Total, Output HIGH			70						
lcc	Total, Output LOW				90	mA	$V_{CC} = MAX$			
	Total at HIGH Z				95					

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS
STIVIBUL	FARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
^t PLH ^t PHL	Propagation Delay, Data to Output		8.0 8.0	12 12	ns	C _I = 45 pF
^t PZH	Output Enable Time to HIGH Level		25	40	ns	$R_L = 667 \Omega$
tPZL	Output Enable Time to LOW Level		27	40	ns	
t _{PLZ}	Output Disable Time from LOW Level		15	25	ns	C _L = 5.0 pF
^t PHZ	Output Disable Time from HIGH Level		15	25	ns	$R_L = 667 \Omega$



DESCRIPTION — The SN54LS/74LS247 thru SN54LS/74LS249 are BCD-to-Seven-Segment Decoder/Drivers.

The LS247 and LS248 are functionally and electrically identical to the LS47 and LS48 with the same pinout configuration. The LS249 is a 16-pin version of the 14-pin LS49 and includes full functional capability for lamp test and ripple blanking which was not available in the LS49.

The composition of all characters, except the 6 and 9 are identical between the LS247, 248, 249 and the LS47, 48 and 49. The LS47 thru 49 compose the \mathcal{E} and \mathcal{E} without tails, the LS247 thru 249 compose the \mathcal{E} and \mathcal{E} with the tails. The LS247 has active-low outputs for direct drive of indicators. The LS248 and 249 have active-high outputs for driving lamp buffers.

All types feature a lamp test input and have full ripple-blanking input/output controls. On all types an automatic leading and/or trailing-edge zero-blanking control (RBI and RBO) is incorporated and an overriding blanking input (BI) is contained which may be used to control the lamp intensity by pulsing or to inhibit the output's lamp test may be performed at any time when the BI/RBO node is at high level. Segment identification and resultant displays are shown below. Display pattern for BCD input counts above 9 are unique symbols to authenticate input conditions.

LS247

- . OPEN-COLLECTOR OUTPUTS DRIVE INDICATORS DIRECTLY
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION

LS248

- INTERNAL PULL-UPS ELIMINATE NEED FOR EXTERNAL RESISTORS
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION

LS249

- OPEN-COLLECTOR OUTPUTS
- LAMP-TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

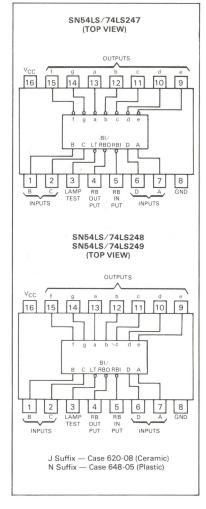


SEGMENT IDENTIFICATION

SN54LS/74LS247 SN54LS/74LS248 SN54LS/74LS249

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

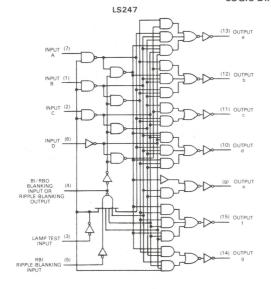
LOW POWER SCHOTTKY

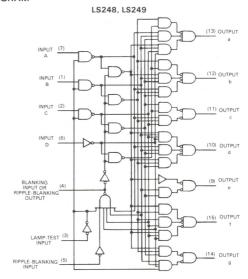


ALL CIRCUIT TYPES FEATURE LAMP INTENSITY MODULATION CAPABILITY

		DRIVER OUTPUTS									
TYPE	ACTIVE	OUTPUT	SINK	MAX	POWER						
	LEVEL	CONFIGURATION	CURRENT	VOLTAGE	DISSIPATION						
SN54LS247	low	open-collector	12 mA	15 V	35 mW						
SN54LS248	high	2-kΩ pull-up	2.0 mA	5.5 V	125 mW						
SN54LS249	high	open-collector	4.0 mA	5.5 V	40 mW						
SN74LS247	low	open-collector	24 mA	15 V	35 mW						
SN74LS248	high	2-kΩ pull-up	6.0 mA	5.5 V	125 mW						
SN74LS249	high	open-collector	8.0 mA	5.5 V	40 mW						

LOGIC DIAGRAM





LS247 FUNCTION TABLE

DECIMAL OR			INP	UTS			BI/RBO [†]			C	UTPUT	S			NOTE
FUNCTION	LT	RBI	D	С	В	Α	BI/ KBO	a	b	С	d	е	f	g	NOTE
0	Н	Н	L	L	L	L	Н	ON	ON	ON	ON	ON	ON	OFF	
1	Н	X	L	L	L	Н	Н	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	Н	X	L	L	Н	L	Н	ON	ON	OFF	ON	ON	OFF	ON	
3	Н	X	L	L	Н	Н	Н	ON	ON	ON	ON	OFF	OFF	ON	
4	Н	X	L	Н	L	L	Н	OFF	ON	ON	OFF	OFF	ON	ON	
5	Н	X	L	Н	L	Н	Н	ON	OFF	ON	ON	OFF	ON	ON	
6	Н	X	L	Н	Н	L	Н	ON	OFF	ON	ON	ON	ON	ON	
7	Н	X	L	Н	Н	Н	Н	ON	ON	ON	OFF	OFF	OFF	OFF	1
8	Н	X	Н	L	L	L	Н	ON	ON	ON	ON	ON	ON	ON	
9	Н	X	Н	L	L	Н	Н	ON	ON	ON	ON	OFF	ON	ON	
10	Н	X	Н	L	Н	L	Н	OFF	OFF	OFF	ON	ON	OFF	ON	
11	Н	X	Н	L	Н	Н	Н	OFF	OFF	ON	ON	OFF	OFF	ON	
12	Н	Х	Н	Н	L	L	Н	OFF	ON	OFF	OFF	OFF	ON	ON	
13	Н	X	Н	Н	L	Н	Н	ON	OFF	OFF	ON	OFF	ON	ON	
14	Н	X	Н	Н	H	L	Н	OFF	OFF	OFF	ON	ON	ON	ON	
15	Н	X	Н	Н	Н	Н	Н	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
ВІ	Х	X	Х	Χ	Х	Х	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	Н	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	Н	ON	ON	ON	ON	ON	ON	ON	4

LS248, LS249 FUNCTION TABLE

DECIMAL OR		1	INP	UTS			BI/RBO [†]			C	UTPUT	s	* 1		NOTE
FUNCTION	LT	RBI	D	С	В	Α	BI/ NBO	а	b	С	d	е	f	g	NOTE
0	Н	Н	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	L	1
1	H	X	L	L	L	H	Н	L	Н	Н	L	L	L	L	1
2	Н	X	L	L	Н	L	Н	Н	Н	L	Н	Н	L	Н	
3	Н	X	L	L	Н	Н	Н	Н	Н	Н	Н	L	L	Н	
4	Н	X	L	Н	L	L	Н	L	Н	Н	L	L	Н	Н	
5	Н	X	L	Н	L	Н	Н	Н	L	Н	Н	L	Н	Н	
6	Н	X	L	H	Н	L	Н	Н	L	Н	Н	Н	H	Н	
7	Н	X	L	Н	Н	Н	Н	Н	Н	Н	L	L	L	L	1
8	Н	X	Н	- L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	
9	Н	X	Н	L	L	Н	Н	Н	Н	Н	Н	L	Н	Н	
10	Н	X	Н	L	Н	L	Н	L	L	L	Н	Н	L	Н	
11	Н	X	Н	L	Н	Н	Н	L	L	Н	Н	L	L	H	
12	Н	X	Н	Н	L	L	Н	L	Н	L	L	L	Н	Н	
13	Н	X	Н	Н	L	Н	Н	Н	L	L	Н	L	Н	Н	
14	Н	X	Н	H	Н	L	Н	L	L	L	Н	Н	Н	Н	
15	Н	X	Н	Н	Н	Н	н .	L	L	L	L	L	L	L	
BI	Х	X	Х	X	X	X	L	L	L	L	L	L	L	L	2
RBI	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	н	Н	Н	Н	Н	Н	Н	Н	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (B1) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

- 2. When a low logic level is applied directly to the blanking input (B1), all segment outputs are off regardless of the level of any other input.
- 3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
- 4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on. †BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High BI/RBO	54,74			-50	μΑ
lOL	Output Current — Low BI/RBO	54 74			1.6 3.2	mA
V _{O(off)}	Off-State Output Voltage a—g	54,74			15	V
I _{O(on)}	On-State Output Current a—g a—g	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DADAMETER			LIMITS		UNITS	TEST COMPITIONS
STIVIBUL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
	1 - 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1	54			0.7	.,,	Guaranteed Input LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = MIN$, $I_{IN} = -18 \text{ mA}$
Vон	Output HIGH Voltage	54	2.4	4.2		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH}$
VОН	BI/RBO	74	2.4	4.2		V	or V _{IL} per Truth Table
	Output LOW Voltage	54,74		0.25	0.4	V	I _{OL} = 1.6 mA V _{CC} = V _{CC} MIN,
VOL	BI/RBO	74		0.35	0.5	V	I _{OL} = 3.2 mA V _{IN} = V _{IL} or V _{IH} per Truth Table
O(off)	Off-State Output Current a—g	54,74			250	μΑ	$V_{CC} = MAX$, $V_{IH} = 2.0 V$, $V_{O(off)} = 15 V$, $V_{IL} = MAX$
	On-State Output Voltage	54,74		0.25	0.4	V	$I_{O(on)} = 12 \text{ mA} V_{CC} = MIN,$
VO(on)	а—д	74		0.35	0.5	V	$\frac{IO(on) - I2 \text{ mA}}{IO(on)} = 24 \text{ mA}$ $\frac{VCC}{VIH} = 2.0 \text{ V},$ $\frac{VIH}{VIL} \text{ per Truth Table}$
					20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$
IL	Input LOW Current Any Input, except BI/RB0)			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
	BI/RBO				-1.2	1	VCC - WAX, VIIV - 0.4 V
OS	Short Circuit Current BI/RBO		-0.3		-2.0	mA	$V_{CC} = MAX$
СС	Power Supply Current			7.0	13	mA	V _{CC} = MAX

AC CHARACTERISTICS: $V_{CC} = 5.0 \text{ V}$, $T_A = 25^{\circ}\text{C}$

SYMBOL	PARAMETER	LIMITS			LINUTC	TEST CONDITIONS		
STIVIBUL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
^t PLH ^t PHL	Turn-Off Time from A Input Turn-On Time from A Input			100 100	ns	C _L = 15 pF,		
tPHL tPLH	Turn-Off Time from RBI Input Turn-On Time from RBI Input			100 100	ns	$R_L = 665 \Omega$		

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High BI/RBO	54,74			-50	μΑ
	a—g	54,74			-100	
lOL	Output Current — Low BI/RBO BI/RBO	54 74			1.6 3.2	mA
	a-g a-g	54 74			2.0 6.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST	CONDITIONS
STIVIBUL	PARAMETER		MIN	TYP	MAX	UNITS	IEST	CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for
	1	54			0.7	V		put LOW Voltage for
V_{IL}	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, III	N = −18 mA
Vон	Output HIGH Voltage	54	2.4	4.2		V		$_{OH} = MAX, V_{IN} = V_{IH}$
•ОП	a—g and BI/RBO	74	2.4	4.2		V	or V _{IL} per Trut	h Table
10	Output Current a—g	54,74	-1.3	-2.0		mA	V _{CC} = MIN, V Input Condition	
	Output LOW Voltage							
	a—q	54,74		0.25	0.4	V	$I_{OL} = 2.0 \text{ mA}$	$V_{CC} = MIN,$
V _{OL}		74		0.35	0.5		$I_{OL} = 6.0 \text{ mA}$	V _{IH} = 2.0 V,
	BI/RBO	54,74	-	0.25	0.4	V	$I_{OL} = 1.6 \text{ mA}$	V _{IL} = per Truth Table
		74		0.35	0.5	·	$I_{OL} = 3.2 \text{ mA}$	1 P P 1 1 2 2 1 2 2 2 2 2 2 2 2 2 2 2 2
	Input HIGH Current				20	μΑ	V _{CC} = MAX, V	$y_{1N} = 2.7 \text{ V}$
lіН	Any Input, except BI/RBO				0.1	mA	V _{CC} = MAX, V	$y_{1N} = 7.0 \text{ V}$
կլ	Input LOW Current Any Input, except BI/RBC)			-0.4	mA	V _{CC} = MAX, V	/IN = 0.4 V
	BI/RBO				-1.2		141747, 4	1114
los	Short Circuit Current BI/RBO		-0.3		-2.0	mA	V _{CC} = MAX	
lcc	Power Supply Current			25	38	mA	V _{CC} = MAX	

AC CHARACTERISTICS: $V_{CC} = 5.0 \text{ V}$, $T_A = 25^{\circ}\text{C}$

SYMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS	
STIVIBUL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
	Propagation Delay Time, High-to-Low-Level Output from A Input Propagation Delay Time, Low-to-High-Level Output from A Input			100 100	ns	$C_L = 15 \text{ pF, R}_L = 4.0 \text{ k}\Omega$	
	Propagation Delay Time, High-to-Low-Level Output from RBI Input Propagation Delay Time, Low-to-High-Level Output from RBI Input			100 100	ns	$C_L = 15 \text{ pF, } R_L = 6.0 \text{ k}\Omega$	

SYMBOL	PARAME	ΓER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage		54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temper	ature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	BI/RBO	54,74	* ,		-50	μΑ
IOL	Output Current — Low	BI/RBO BI/RBO	54 74			1.6 3.2	mA
VOH	Output Voltage — High	а—д	54,74			5.5	V
lOL	Output Current — Low	a—g a—g	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		LIMITO	TEST CONDITIONS
STIVIBUL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
		54			0.7	.,	Guaranteed Input LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs
VIK	Input Clamp Diode Voltage		-	-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$
Voн	Output HIGH Voltage	54	2.4	4.2		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH}$
VОН	BI/RBO	74	2.4	4.2		V	or V _{IL} per Truth Table
ЮН	Output HIGH Current a—g	54,74			250	μΑ	V _{CC} = MIN, V _{IH} = 2.0 V, V _{OH} = 5.5 V, V _{IL} = MAX
	Output LOW Voltage						
	BI/RBO	54,74		0.25	0.4	V	$I_{OL} = 1.6 \text{ mA}$ $V_{CC} = MIN,$
VOL		74		0.35	0.5		$I_{OL} = 3.2 \text{ mA}$ $V_{IH} = 2.0 \text{ V}$
	a—g	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{IL} = \text{per Truth Table}$
		74		0.35	0.5		I _{OL} = 8.0 mA
	Input HIGH Current	У.			20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$
lН	Any Input, except BI/RBO				0.1	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$
ll L	Input LOW Current Any Input, except BI/RB0)			-0.4	mA	$V_{CC} = MAX, V_{IN} = 0.4 V$
	BI/RBO				-1.2	111/2	VCC 141/7/, V[[V] = 0.4 V
los	Short Circuit Current BI/RBO		-0.3		-2.0	mA	V _{CC} = MAX
lcc	Power Supply Current			8.0	15	mA	V _{CC} = MAX

AC CHARACTERISTICS: $V_{CC} = 5.0 \text{ V}$, $T_A = 25^{\circ}\text{C}$

SYMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS
STIVIBUL	FARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
	Propagation Delay Time, High-to-Low-Level Output from A Input Propagation Delay Time, Low-to-High-Level Output from A Input			100 100	ns	$C_L = 15 \text{ pF}, R_L = 2.0 \text{ k}\Omega$
	Propagation Delay Time, High-to-Low-Level Output from RBI Input Propagation Delay Time, Low-to-High-Level Output from RBI Input			100 100	ns	$C_L = 15 \text{ pF}, R_L = 6.0 \text{ k}\Omega$



DESCRIPTION — The TTL/MSI SN54LS/74LS251 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS251 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- INVERTING AND NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION FFFFCTS

SN54LS251 SN74LS251

8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

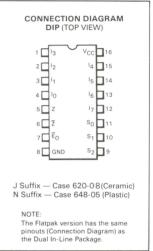
PIN NAME	S	LOADING	(Note a)
		HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$S_0 - S_2$ \overline{E}_0	Output Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
I ₀ — I ₇	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	65 (25) U.L.	15 (7.5) U.L.
Z	Complementary Multiplexer Output	65 (25) U.L.	15 (7.5) U.L.

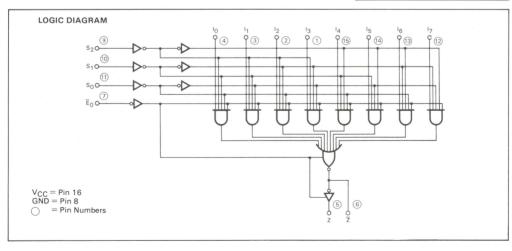
NOTES

a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

(Note b)

b. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.





FUNCTIONAL DESCRIPTION — The LS251 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0 , S_1 , S_2 . Both assertion and negation outputs are provided. The Output Enable input (\overline{E}_0) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{\mathsf{E}}_{\mathsf{O}} \cdot (\mathsf{I}_{\mathsf{0}} \cdot \overline{\mathsf{S}}_{\mathsf{0}} \cdot \overline{\mathsf{S}}_{\mathsf{1}} \cdot \overline{\mathsf{S}}_{\mathsf{2}} + \mathsf{I}_{\mathsf{1}} \cdot \mathsf{S}_{\mathsf{0}} \cdot \overline{\mathsf{S}}_{\mathsf{1}} \cdot \overline{\mathsf{S}}_{\mathsf{2}} + \mathsf{I}_{\mathsf{2}} \cdot \overline{\mathsf{S}}_{\mathsf{0}} \cdot \mathsf{S}_{\mathsf{1}} \cdot \overline{\mathsf{S}}_{\mathsf{2}} + \mathsf{I}_{\mathsf{3}} \cdot \mathsf{S}_{\mathsf{0}} \cdot \mathsf{S}_{\mathsf{1}} \cdot \overline{\mathsf{S}}_{\mathsf{2}} + \mathsf{I}_{\mathsf{3}} \cdot \mathsf{S}_{\mathsf{0}} \cdot \mathsf{S}_{\mathsf{1}} \cdot \overline{\mathsf{S}}_{\mathsf{2}} + \mathsf{I}_{\mathsf{3}} \cdot \mathsf{S}_{\mathsf{0}} \cdot \mathsf{S}_{\mathsf{1}} \cdot \mathsf{S}_{\mathsf{2}} + \mathsf{I}_{\mathsf{3}} \cdot \mathsf{S}_{\mathsf{0}} \cdot \mathsf{S}_{\mathsf{1}} \cdot \mathsf{S}_{\mathsf{2}}).$$

When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

TRUTH TABLE

s ₂	S ₁	s ₀	10	11	12	13	14	15	16	17	Z	Z
X	X	X	Х	X	X	X	×	×	X	×	(Z)	(Z)
L	L	L	L	X	X	×	×	×	×	×	н	L
L	L	L	н	×	X	×	×	×	×	×	L	н
L	L	Н	×	L	X	×	×	×	×	×	н	L
L	L	Н	×	Н	X	X	X	X	X	X	L	н
L	Н	L	×	X	L	X	×	×	X	X	н	L
L	Н	L	X	X	Н	X	×	×	×	×	L	н
L	Н	Н	X	×	×	L	×	×	×	X	н	L
L	Н	Н	×	X	X	Н	X	X	X	X	L	н
H	L	L	×	×	X	X	L	×	×	X	н	L
н	L	L	×	×	×	×	Н	×	X	×	L	н
н	L	Н	×	×	X	×	×	L	×	X	Н	L
н	L	Н	×	×	×	×	×	Н	X	X	L	н
н	н	L	×	X	×	×	×	×	L	X	Н	L
н	Н	L	×	×	×	×	×	×	Н	X	L	н
н	Н	н	×	×	×	X	X	X	X	L	Н	L
н	Н	Н	X	X	×	X	×	×	×	Н	L	Н
	X	X X L L L L L L L L L L L L L L L L L L	X X X L L L L L L H L H L H L L H H L H H L H H L H H H L L H H H L L H H H H L H H H H H H H H H H	X	X X X X X X X L L L L X L L H X L L H X X X X	X X X X X X X X X X X X X X X X X X X	X	X	X	X	X	X X X X X X X X X X X X X X X X X L L L L L X X X X X X X X X X X X X L L L L L X X X X X X X X X X L L L L L L X X X X X X X X X X X L L L L L L X X X X X X X X X X L L L L L L X X X X X X X X X X L L L L L L X X X X X X X X X L L L L L L X X X X X X X X X X L L L L L X X X X X X X X X L L L L L X

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

(Z) = High Impedance (Off)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER	7	MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	٧
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54 74			-1.0 -2.6	mA
lOL	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST	CONDITIONS	
STIVIDOL	PARAMETER		MIN	TYP	MAX	UNITS	1231 CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Ir All Inputs	put HIGH Voltage for	
\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	54			0.7	.,,		put LOW Voltage for		
VIL	Input LOW Voltage				0.8	V	All Inputs		
VIK	Input Clamp Diode Voltage			-0.65	-1.5	- V	V _{CC} = MIN, I _I	N = −18 mA	
Vон	Output HIGH Voltage	54	2.4	3.4		V		$_{DH} = MAX, V_{IN} = V_{IH}$	
TON Catput men venage	Output man voltage	74	2.4	3.1		V	or V _{IL} per Tru	uth Table	
_	0	54,74		0.25	0.4	V		$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 24 mA	V _{IN} = V _{IL} or V _{IH} per Truth Table	
lozh	Output Off Current HIGH				20	μΑ	V _{CC} = MAX,	V _{OUT} = 2.4 V	
lozL	Output Off Current LOW				-20	μΑ	$V_{CC} = MAX, V$	V _{OUT} = 0.4 V	
					20	μΑ	V _{CC} = MAX,	V _{IN} = 2.7 V	
lн	Input HIGH Current				0.1	mA	V _{CC} = MAX,	/ _{IN} = 7.0 V	
IIL	Input LOW Current				-0.4	mA	V _{CC} = MAX,	V _{IN} = 0.4 V	
los	Short Circuit Current		-30		-130	mA	V _{CC} = MAX		
lcc	Power Supply Current				10	mA	V _{CC} = MAX,	√Ē = 0.0 V	
					12	mA	V _{CC} = MAX,	√Ē = 4.5 V	
			-		-				

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

		_						
SYMBOL	PARAMETER		LIMITS	,	UNITS	TEST CONDITIONS		
OTWIDOL	TANAMETER	MIN	TYP	MAX	ONITS			
^t PLH ^t PHL	Propagation Delay, Select to Z Output		20 21	33 33	ns	Fig. 1		
^t PLH ^t PHL	Propagation Delay, Select to Z Output		29 28	45 45	ns	Fig. 2		
^t PLH ^t PHL	Propagation Delay, Data to Z Output		10 9.0	15 15	ns	Fig. 1	C _L = 15 pF,	
^t PLH ^t PHL	Propagation Delay, Data to Z Output		17 18	28 28	ns	Fig. 2	$R_L = 2K \Omega$	
^t PZH ^t PZL	Output Enable Time to Z Output		17 24	27 40	ns	Figs. 4, 5		
^t PZH ^t PZL	Output Enable Time to Z Output		30 26	45 40	ns	Figs. 3, 5		
^t PHZ ^t PLZ	Output Disable Time to Z Output		37 15	55 25	ns	Figs. 3, 5 Figs. 4, 5 $C_L = 5 \text{ pF}$ $R_L = 667 \Omega$		
^t PHZ ^t PLZ	Output Disable Time to Z Output		30 15	45 25	ns			

3-STATE AC WAVEFORMS

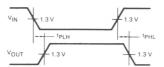


Fig. 1

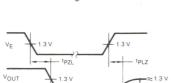


Fig. 3

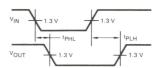


Fig. 2

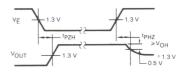


Fig. 4

AC LOAD CIRCUIT

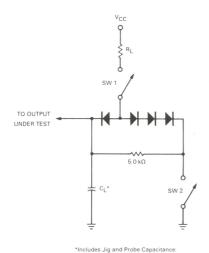


Fig. 5

SWITCH POSITIONS

SYMBOL	SW1	SW2		
^t PZH	Open	Closed		
tPZL	Closed	Open		
tPLZ	Closed	Closed		
^t PHZ	Closed	Closed		



DESCRIPTION — The LSTTL/MSI SN54LS/74LS253 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\bar{\mathbb{E}}_0$) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

SN54LS253 SN74LS253

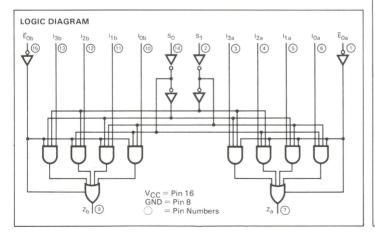
DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

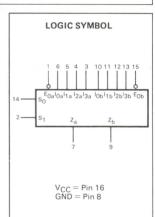
LOW POWER SCHOTTKY

	LOADING (Note a)				
	HIGH	LOW			
Common Select Inputs	0.5 U.L.	0.25 U.L.			
Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.			
Multiplexer Inputs	0.5 U.L.	0.25 U.L.			
Multiplexer Output (Note b)	65(25) U.L.	15(7.5) U.L.			
Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.			
Multiplexer Inputs	0.5 U.L.	0.25 U.L.			
Mutiplexer Output (Note b)	65(25) U.L.	15(7.5) U.L.			
	Output Enable (Active LOW) Input Multiplexer Inputs Multiplexer Output (Note b) Output Enable (Active LOW) Input Multiplexer Inputs	HIGH			

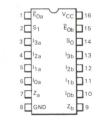
NOTES

- a. 1 TTL Unit Load (U.L.) = $40 \,\mu\text{A}$ HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.





CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

NOTE

NOIE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package. **FUNCTIONAL DESCRIPTION** — The LS253 contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1) . The 4-input multiplexers have individual Output Enable $(\overline{E}_{0a}, \overline{E}_{0b})$ inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$\begin{split} Z_{\mathbf{a}} &= \overline{E}_{0\mathbf{a}} \cdot (\mathsf{I}_{0\mathbf{a}} \cdot \overline{S}_1 \cdot \overline{S}_0 + \mathsf{I}_{1\mathbf{a}} \cdot \overline{S}_1 \cdot S_0 + \mathsf{I}_{2\mathbf{a}} \cdot S_1 \cdot \overline{S}_0 + \mathsf{I}_{3\mathbf{a}} \cdot S_1 \cdot S_0) \\ Z_{\mathbf{b}} &= \overline{E}_{0\mathbf{b}} \cdot (\mathsf{I}_{0\mathbf{b}} \cdot \overline{S}_1 \cdot \overline{S}_0 + \mathsf{I}_{1\mathbf{b}} \cdot \overline{S}_1 \cdot S_0 + \mathsf{I}_{2\mathbf{b}} \cdot S_1 \cdot \overline{S}_0 + \mathsf{I}_{3\mathbf{b}} \cdot S_1 \cdot S_0) \end{split}$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

	ECT UTS		DATA	INPUTS	OUTPUT ENABLE	ОИТРИТ	
s ₀	s ₁	10	11	12	13	E ₀	Z
X	X	Х	X	X	X	Н	(Z)
L	L	L	×	×	×	L	L
L	L	Н	×	×	X	L	н
Н	L	×	L	×	×	L	L
Н	L	×	Н	×	×	L	н
L	Н	×	×	L	×	L	L
L	Н	×	×	Н	×	L	н
Н	Н	×	×	×	L	L	L
Н	Н	X	X	X	Н	L	Н

H = HIGH Level

L = LOW Level

X = Irrelevant

(Z) = High Impedance (off)

Address inputs So and So are common to both sections.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage 54 74		4.5 4.75	5.0 5.0	5.5 5.25	V
Тд	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54 74			-1.0 -2.6	mA
lOL	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TECT	CONDITIONS
STIVIBUL	PARAIVIETER		MIN		MAX	UNITS	TEST CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for
					0.7	.,		put LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltag	e		-0.65	-1.5	V	V _{CC} = MIN, I _I	N = −18 mA
Vон	Output HIGH Voltage 54		2.4	3.4		V		OH = MAX, VIN = VIH
VOH Catput man voltage	74	2.4	3.1		V	or V _{IL} per Tru	th Table	
V _{OL} Output LOW Voltage	54,74		0.25	0.4	V		V _{CC} = V _{CC} MIN,	
	74		0.35	0.5	V	I _{OL} = 24 mA	V _{IN} = V _{IL} or V _{IH} per Truth Table	
lozh	Output Off Current HIGH	•			20	μΑ	$V_{CC} = MAX, V$	V _{OUT} = 2.4 V
lozL	Output Off Current LOW				-20	μΑ	$V_{CC} = MAX, V$	V _{OUT} = 0.4 V
					20	μΑ	$V_{CC} = MAX, V$	$V_{1N} = 2.7 \text{ V}$
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V$	$V_{1N} = 7.0 \text{ V}$
IIL	Input LOW Current			× 2	-0.4	mA	$V_{CC} = MAX, V$	V _{IN} = 0.4 V
los	Short Circuit Current		-30		-130	mA	$V_{CC} = MAX$	
lcc	Power Supply Current		1 1		12	mA	$V_{CC} = MAX, V$	√Ē = 0.0 V
					14	mA	V _{CC} = MAX, V	/E = 4.5 V

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0$ V (See SN54LS251 for Waveforms)

SYMBOL	DADAMETER		LIMITS		LINUTC	TEGT COMPLETIONS		
	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIO		
^t PLH ^t PHL	Propagation Delay, Data to Output	1 = = =	17 13	25 20	ns	Fig. 1		-> "_
^t PLH ^t PHL	Propagation Delay, Select to Output		30 21	45 32	ns	Fig. 1	$C_L = 45 \text{ pF},$ $R_L = 667 \Omega$	
^t PZH ^t PZL	Output Enable Time		15 15	28 23	ns	Figs. 4, 5		
^t PHZ ^t PLZ	Output Disable Time		27 18	41 27	ns	Figs. 3, 5	$C_L = 5.0 \text{ pF}$ $R_L = 667 \Omega$	

MOTOROLA

DESCRIPTION — The SN54LS/74LS256 is a Dual 4-Bit Addressable Latch with common control inputs: these include two Address inputs (A₀, A₁), an active LOW Enable input (E) and an active LOW Clear input (CL). Each latch has a Data input (D) and four outputs (Q0-Q3).

When the Enable (\overline{E}) is HIGH and the Clear input (\overline{CL}) is LOW, all outputs (Q_0-Q_3) are LOW. Dual 4-channel demultiplexing occurs when the (\overline{CL}) and \overline{E} are both LOW. When \overline{CL} is HIGH and \overline{E} is LOW, the selected output (Q_Q-Q₃), determined by the Address inputs, follows D. When the E goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode (E=LOW, CL=HIGH), changing more than one bit of the Address (A_O, A₁) could impose a transient wrong address. Therefore, this should be done only while in the memory mode (E=CL=HIGH).

- SERIAL-TO-PARALLEL CAPABILITY
- OUTPUT FROM EACH STORAGE BIT AVAILABLE
- RANDOM (ADDRESSABLE) DATA ENTRY
- EASILY EXPANDABLE
- ACTIVE LOW COMMON CLEAR
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION **EFFECTS**

PIN NAMES		LOADING (Note a)			
		HIGH	LOW		
A ₀ , A ₁	Address Inputs	0.5 U.L.	0.25 U.L.		
Da, Db	Data Inputs	0.5 U.L.	0.25 U.L.		
Ē	Enable Input (Active LOW)	1.0 U.L.	0.5 U.L.		
CL	Clear Input (Active LOW)	0.5 U.L.	0.25 U.L.		
Q _{0a} -Q _{3a} , Q _{0b} -Q _{3b}	Parallel Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.		

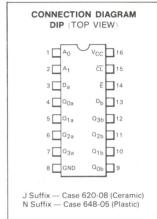
NOTES

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

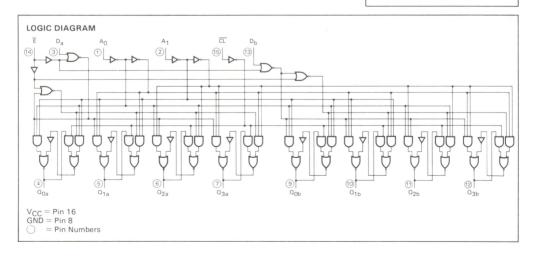
SN54LS256 SN74LS256

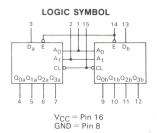
DUAL 4-BIT ADDRESSABLE LATCH

LOW POWER SCHOTTKY



The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.





TRUTH TABLE

CL	Ē	D	A ₀	Α1	α ₀	Q ₁	02	03	MODE
L	Н	X	X	X	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	Demultiplex
L	L	Н	L	L	Н	L	L	L	
L	L	L	Н	L	L	L	L	L	
L	L	Н	Н	L	L	Н	L	L	
L	L	L	L	Н	L	L	L	L	
L	L	Н	L	Н	L	L	Н	L	
L	L	L	Н	Н	L	L	L	L	
L	L	Н	Н	Н	L	L	L	Н	
Н	Н	X	X	X	Q_{N-1}	Q_{N-1}	Q_{N-1}	Q_{N-1}	Memory
Н	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}	Addressable
Н	L	H	L	L	Н	Q_{N-1}	Q_{N-1}	Q_{N-1}	Latch
Н	L	L	Н	L	Q_{N-1}	L	Q_{N-1}	Q_{N-1}	
Н	L	Н	Н	L	Q_{N-1}	Н	Q_{N-1}	Q_{N-1}	
Н	L	L	L	Н	Q_{N-1}	Q_{N-1}	L	Q_{N-1}	
Н	L	Н	L	H	Q_{N-1}	Q_{N-1}	Н	Q_{N-1}	
Н	L	L	Н	Н	Q_{N-1}	Q_{N-1}	Q_{N-1}	L	
Н	L	Н	Н	Н	Q_{N-1}	Q_{N-1}	Q_{N-1}	Н	

H = High Voltage Level L = LOW Voltage Level

X = Immaterial

MODE SELECTION

Ē	CL	MODE
L	Н	Addressable Latch
Н	Н	Memory
L	L	Dual 4-Channel Demultiplexer
Н	L	Clear

GUARANTEED OPERATING RANGES

00/110 111122	0. 1					
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DADAMETED		LIMITS			TEST CONDITIONS			
STIVIBUL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
.,		54			0.7	.,	Guaranteed Input LOW Voltage for		
V_{IL}	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = MIN$, $I_{IN} = -18 \text{ mA}$		
VOH	Output HIGH Voltage	54	2.4	3.5		V	$V_{CC} = MIN$, $I_{OH} = MAX$, $V_{IN} = V_{IH}$		
	Output High Voltage	74	2.4	3.5		V	or V _{IL} per Truth Table		
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN},$		
V _{OL}	Output LOW Voltage	74		0.35	0.5	V	IOL = 8.0 mA VIN = VIL or VIH per Truth Table		
lн	Input HIGH Current Others E Input	ef			20 40	μΑ	V _{CC} = MAX, V _{IN} = 2.7 V		
чн	Others E Input				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V		
IIL	Input LOW Current Others E Input			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V			
los	Short Circuit Current	-20		-100	mA	V _{CC} = MAX			
lcc	Power Supply Current			25	mA	V _{CC} = MAX			

AC CHARACTERISTICS: $T_{\mbox{\scriptsize A}} = 25 \ensuremath{^{\circ}}\mbox{\scriptsize C}$

SYMBOL	DARAMETER	LIMITS			LINUTO	TEST COMPITIONS	
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH ^t PHL	Turn-Off Delay, Enable to Output Turn-On Delay, Enable to Output		20 16	27 24	ns ns	$V_{CC} = 5.0 \text{ V, } C_L = 15 \text{ pF}$ Fig. 1	
^t PLH ^t PHL	Turn-Off Delay, Data to Output Turn-On Delay, Data to Output		20 13	30 20	ns ns	$V_{CC} = 5.0 \text{ V, } C_L = 15 \text{ pF}$ Fig. 2	
tPLH tPHL	Turn-Off Delay, Address to Output Turn-On Delay, Address to Output		20 14	30 24	ns ns	$V_{CC} = 5.0 \text{ V, } C_L = 15 \text{ pF}$ Fig. 3	
^t PHL	Turn-On Delay, Clear to Output		12	23	ns	$V_{CC} = 5.0 \text{ V, } C_L = 15 \text{ pF}$ Fig. 5	

AC SETUP REQUIREMENTS: $T_A = 25$ °C

SYMBOL	PARAMETER		LIMITS			TEST CONDITIONS
STIVIBUL	FARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
t _S	Data Setup Time	20			ns	V _{CC} = 5.0 V Fig. 4
t _S	Address Setup Time	0			ns	Fig. 6
th	Data Hold Time	0			ns	V _{CC} = 5.0 V Fig. 4
th	Address Hold Time	15			ns	V _{CC} = 5V Fig. 6
t₩	Enable Pulse Width	15			ns	V _{CC} = 5.0 V Fig. 1

AC WAVEFORMS

Fig. 1 TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH

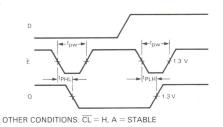


Fig. 2 TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT

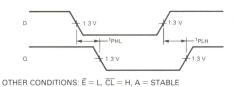


Fig. 3 TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT

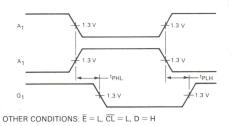


Fig. 4 SETUP AND HOLD TIME, DATA TO ENABLE

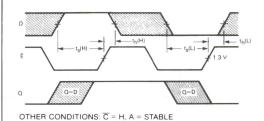


Fig. 5 TURN-ON DELAY, CLEAR TO OUTPUT

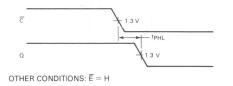
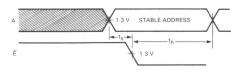


Fig. 6 SETUP TIME, ADDRESS TO ENABLE

(SEE NOTES 1 AND 2)



OTHER CONDITIONS: $\overline{\text{CL}} = \text{H}$

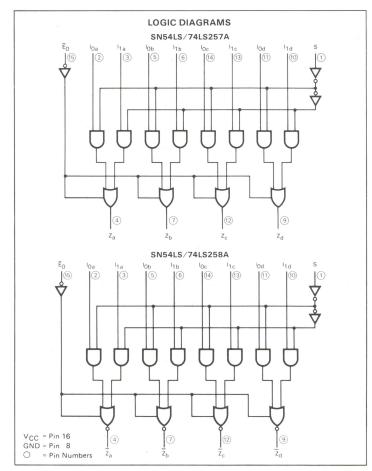
NOTES

- The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- 2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.



$$\label{eq:DESCRIPTION} \begin{split} \text{DESCRIPTION} &- \text{The LSTTL/MSI SN54LS/74LS257A} \text{ and the SN54LS/74LS258A} \text{ are Quad 2-Input Multiplexers with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (EO) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.$$

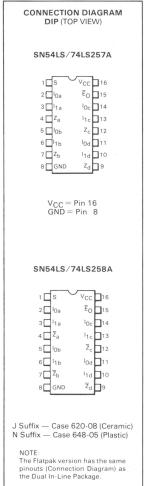
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS



SN54LS/74LS257A SN54LS/74LS258A

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY



FUNCTIONAL DESCRIPTION — The LS257A and LS258A are Quad 2-Input Multiplexers with 3-state outputs. They select four bits of data from two sources each under control of a Common Data Select Input. When the Select Input is LOW, the IQ inputs are selected and when Select is HIGH, the I1 inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form for the LS257A and in the inverted form for the LS258A.

The LS257A and LS258A are the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

When the Output Enable Input (\overline{E}_O) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS LS257A	OUTPUTS LS258A				
ĒO	S	10	11	Z	Z				
Н	X	Χ	X	(Z)	(Z)				
L	Н	X	L	L	Н				
L	Н	X	Н	Н	L				
L	L	L	X	L	Н				
L	L	Н	X	H	L				

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

(Z) = High impedance (off)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V .
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54 74			-1.0 -2.6	mA
lOL	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETE		LIMITS	8	UNITS	TEST CONDITIONS			
STIVIBUL	PARAMET	EK	MIN	TYP	MAX	UNITS	1531 0	CINDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	out HIGH Voltage for	
		54			0.7		Guaranteed Input LOW Voltage for		
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	I = −18 mA	
Vон	Output HIGH Voltage	54	2.4	3.4	-	V	V _{CC} = MIN, I _O	$H = MAX, V_{IN} = V_{IH}$	
vон	Output high voitage	74	2.4	3.1		V	or V _{IL} per Truth	Table	
		54,74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN,	
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 24 mA	V _{IN} = V _{IL} or V _{IH} per Truth Table	
lozh	Output Off Current — H	HIGH			20	μΑ	V _{CC} = MAX, V	OUT = 2.4 V	
lozL	Output Off Current — L	-OW			-20	μΑ	V _{CC} = MAX, V	OUT = 0.4 V	
		Other Inputs			20	μΑ			
lн	Input HIGH Current	S Inputs			40	μΑ	$V_{CC} = MAX, V_{IN} = 2.7 V$		
ıın	Input man current	Other Inputs			0.1	mA	Voc = MAX V	IN = 7.0 V	
		S Inputs			0.2	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$		
IIL	Input LOW Current	Other Inputs			-0.4	mA	$V_{CC} = MAX, V_{IN} = 0.4 V$		
'IL	Imput LOVV Current	S Inputs			-0.8	mA	VCC - IVIAX, V	IN - 0.4 V	
los	Short Circuit Current		-30		-130	mA	V _{CC} = MAX		
	Power Supply Current								
lcc	Total, Output HIGH	LS257A LS258A			10 7.0	mA mA	V _{CC} = MAX		
	Total, Output LOW	LS257A LS258A			16 14	mA mA	, voc wax		
	Total, Output 3-State			19	mA	1			

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0$ V (See SN54LS251 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS		
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS		
^t PLH ^t PHL	Propagation Delay, Data to Output		12 12	18 18	ns	Fig. 1, 2	C _L = 45 pF	
^t PLH ^t PHL	Propagation Delay, Select to Output		14 14	21 21	ns	Fig. 1, 2	C _L = 45 pF	
^t PZH	Output Enable Time to HIGH Level		20	30	ns	Figs. 4, 5	C _L = 45 pF	
^t PZL	Output Enable Time to LOW Level		20	30	ns	Figs. 3, 5	$R_L = 667 \Omega$	
t _{PLZ}	Output Disable Time to LOW Level		16	25	ns	Figs. 3, 5	$C_{L} = 5.0 pF$	
^t PHZ	Output Disable Time from HIGH Level		18	30	ns	Figs. 4, 5	$R_L = 667 \Omega$	



DESCRIPTION — The SN54LS/74LS259 is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable.

- SERIAL-TO-PARALLEL CONVERSION
- EIGHT BITS OF STORAGE WITH OUTPUT OF EACH BIT **AVAILABLE**
- RANDOM (ADDRESSABLE) DATA ENTRY
- ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY
- EASILY EXPANDABLE
- COMMON CLEAR

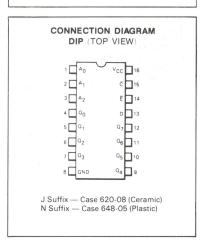
PIN NAMES		LOADIN	G (Note a)
		HIGH	LOW
A ₀ , A ₁ , A ₂ D E C Q ₀ to Q ₇	Address Inputs Data Input Enable (Active LOW) Input Clear (Active LOW) Input Parallel Latch Outputs (Note b)	0.5 U.L. 0.5 U.L. 1.0 U.L. 0.5 U.L. 10 U.L.	0.25 U.L. 0.25 U.L. 0.5 U.L. 0.25 U.L. 5(2.5) U.L.

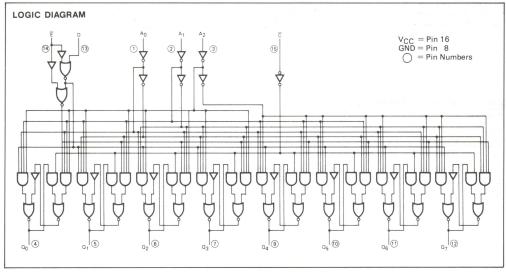
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54LS259 SN74LS259

8-BIT ADDRESSABLE LATCH

LOW POWER SCHOTTKY





FUNCTIONAL DESCRIPTION — The SN54LS/74LS259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the SN54LS/74LS259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operations.

MODE SELECTION

TRUTH TABLE

PRESENT OUTPUT STATES

Ē	C	MODE
L	Н	Addressable Latch
Н	Н	Memory
L	L	Active HIGH Eight-Channel
		Demultiplexer
Н	L	Clear

C E D AOA1A2 QO Q1 Q2 Q3 Q4 Q5 Q6 Q7 MODE L H X X X L N A A									TILOLIA	1 0017	0101	/ (120		1.00	
L L L L L L L L L L L L L L L L L L L	c	Ē	D	A ₀	Α1	Α2	QO	Q ₁	02	03	04	Q ₅	Q ₆	Q7	MODE
L L H L L L L L L L L L L L L L L L L L	L	Н	Χ	Χ	Χ	Χ	L	L	L	L	L	L	L	L	Clear
L L H L L L L L L L L L L L L L L L L L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L L H H L L L L L L L L L L L L L L L L	L	L	Н	L	L	L	Н	L	L	L	L	L	L	L	
	L	L	L	Н	L	L	L	L	L	L	L	L	L	L	
H H X X X X Q _{N-1} —	L	L	Н	Н	L	L	L	Н	L	L	L	L	L	L	
H H X X X X Q _{N-1} —		•	•		•										
H H X X X X Q _{N-1} —		•	•		•					•					
H H X X X X Q _{N-1} —		•	•		•										
H H X X X X Q _{N-1} —		•	•		•		-								,
H H X X X X Q _{N-1} —	٠	•	•		•										
H I I L L L H C QN-1 QN-1 QN-1 Addressable Latch H L H L L L QN-1 L QN-1 H L H H L L QN-1 H QN-1	L	L	Н	Н	Н	Н	L	L	L	L	L	L	L	Н	
H L H L L H QN-1 QN-1	Н	Н	Χ	Χ	Χ	Χ	Q_{N-1}				-				Memory
H L H L L L H Q _{N-1} Q _{N-1} D _{N-1} D _{A-1} D	Н	Τ	1	L	L	L	L	Q _{NI} -1	QN-1	Q _N -1				-	Addressable
H L L H L L Q _{N-1} L Q _{N-1} H L H H L L Q _{N-1} H Q _{N-1} • • • • • • • • • • • • • • • • • • •	Н	L	Н	L	L	L	Н								Latch
H L H H L L Q _{N-1} H Q _{N-1} · · · · · · · · · · · · · · · · · · ·	Н	L	L	Н	L	L	Q _{N-1}	Ĺ						-	
	Н	L	Н	Н	L	L						-		-	
		•													
		•			•										
• • • • • • • • • • • • • • • • • •		•													
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		•			•					•					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		•			•										
$ H L H H H H Q_{N-1} \longrightarrow Q_{N-1} H$	Н	L	L	Н	Н	Н	Q_{N-1}					-	Q_{N-1}	L	-, -, -
	Н	L	Н	Н	Н	Н	Q_{N-1}					-	Q_{N-1}	Н	

X = Don't Care ConditionL = LOW Voltage Level

H = HIGH Voltage Level

 Q_{N-1} = Previous Output State

GUARANTEED OPERATING RANGES

GUARANII	EED OPERATING KANGES					
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74	7 7 7		-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

01/44001			LIMITS						
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST	CONDITIONS	
VIH	Input HIGH Voltage	***	2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
.,		54			0.7	.,		put LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
		54	2.5	3.5		V	V _{CC} = MIN, I _C	$v_{CC} = min$, $i_{OH} = max$, $v_{IN} = v_{IH}$	
Vон	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Truth Table		
		54,74	2	0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MI		
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	$V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table	
					20	μΑ	V _{CC} = MAX, V	/ _{IN} = 2.7 V	
lн	Input HIGH Current				0.1	mA	V _{CC} = MAX, V	V _{CC} = MAX, V _{IN} = 7.0 V	
ΙΙL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V	/IN = 0.4 V	
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current				36	- mA	V _{CC} = MAX	1,11	

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

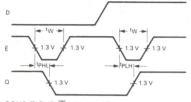
OVAADOL	DARAMETER	LIMITS			UNITS	CONDITIONS
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
tPLH tPHL			22 15	35 24	ns ns	
tPLH tPHL	Turn-Off Delay, Data to Output Turn-On Delay, Data to Output		20 13	32 21	ns ns	$C_{l} = 15 pF$
^t PLH ^t PHL	Turn-Off Delay, Address to Output Turn-On Delay, Address to Output		24 18	38 29	ns ns	ο <u>ς</u> το μ.
tPHL	Turn-On Delay, Clear to Output		17	27	ns	

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER		LIMITS		UNITS	
	FANAIVIETEN		TYP	MAX	UNITS	
t _S	Input Setup Time	20			ns	
tW	Pulse Width, Clear or Enable	15	19		ns	
th	Hold Time, Data	5.0			ns	
th	Hold Time, Address	20			ns	

AC WAVEFORMS

Fig. 1 TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



OTHER CONDITIONS: $\overline{C} = H$, A = STABLE

Fig. 2 TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT

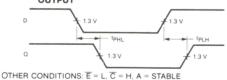


Fig. 3 TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT

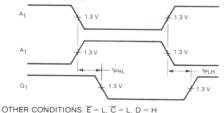
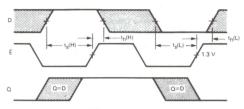


Fig. 4 SETUP AND HOLD TIME, DATA TO ENABLE



OTHER CONDITIONS: $\overline{C} = H$, A = STABLE

Fig. 5 TURN-ON DELAY, CLEAR TO OUTPUT

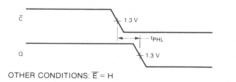
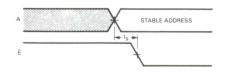


Fig. 6 SETUP TIME, ADDRESS TO ENABLE (SEE NOTES 1 AND 2)

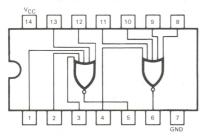


OTHER CONDITIONS: $\overline{C} = H$

NOTES:

- 1. The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- 2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.





J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

SN54LS260 SN74LS260

DUAL 5-INPUT NOR GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP 1	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

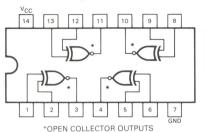
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS			
SYMBOL	PARAIVIETER	1	MIN	TYP	MAX	UNITS	IEST	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp	out HIGH Voltage for	
		54			0.7		Guaranteed Inp	out LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volt	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	=-18 mA	
Voн	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{I}$		
VОН	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth	per Truth Table	
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	V _{CC} = MAX, V _I	N = 2.7 V	
lн	Input HIGH Current		1.0		0.1	mA	V _{CC} = MAX, V _I	N = 7.0 V	
İIL	Input LOW Current				-0.4	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$		
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current Total, Output HIGH Total, Output LOW				4.0 5.5	mA	V _{CC} = MAX		

AC CHARACTERISTICS: $T_A = 25$ °C

CVAADOL	DADAMETER	LIMITS			UNITS	TEST CONDITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH	Turn Off Delay, Input to Output	N	5.0	15	ns	$V_{CC} = 5.0 V$	
tPHL	Turn On Delay, Input to Output		6.0	15	ns	$C_L = 15 pF$	





TRUTH TABLE

	11	V	OUT					
А		В	Z					
L		L	Н					
L		н	L					
Н		L	L					
Н		Н	Н					

SN54LS266 SN74LS266

QUAD 2-INPUT EXCLUSIVE NOR GATE

LOW POWER SCHOTTKY

J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
Vон	Output Voltage — High	54,74			5.5	V
IOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TECT	CONDITIONS	
STIVIBUL	FARAIVIETER		MIN	TYP	MAX	UNITS	TEST	CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for	
	1	54	4		0.7			put LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
V_{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
IOH	Output HIGH Current	54,74			100	μΑ	$V_{CC} = MIN, V_{OH} = MAX$		
	0 0	54,74		0.25	0.4	V		$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	VIN = VIL or VIH per Truth Table	
					40	μΑ	V _{CC} = MAX, V	/ _{IN} = 2.7 V	
lΗ	Input HIGH Current				0.2	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$		
I _{IL}	Input LOW Current				-0.8	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$		
lcc	Power Supply Current				13	mA	V _{CC} = MAX		

AC CHARACTERISTICS: $T_A = 25$ °C

SYMBOL	PARAMETER		LIMITS	UNITS		CONDITIONS		
STIVIBUL	PARAIVIETER	MIN	TYP	MAX	UNITS	CONDITIONS		
^t PLH ^t PHL	Propagation Delay, Other Input LOW		18 18	30 30	ns	V _{CC} = 5.0 V		
^t PLH ^t PHL	Propagation Delay, Other Input HIGH		18 18	30 30	ns	$C_L = 15 \text{ pF}, R_L = 2.0 \text{ k}\Omega$		



DESCRIPTION — The SN54LS/74LS273 is a high-speed 8-Bit Register. The register consists of eight D-Type Flip-Flops with a Common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch lead spacing.

- 8-BIT HIGH SPEED REGISTER
- PARALLEL REGISTER
- COMMON CLOCK AND MASTER RESET
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

SN54LS273 SN74LS273

8-BIT REGISTER WITH CLEAR

LOW POWER SCHOTTKY

DO - D7 Data Inputs 0.5 U.L. 0.25 U.L. <td< th=""><th>PIN NAM</th><th>ES</th><th colspan="4">LOADING (Note a)</th></td<>	PIN NAM	ES	LOADING (Note a)			
DO – D7 Data Inputs 0.5 U.L. 0.25 U.L. MR Master Reset (Active LOW) Input 0.5 U.L. 0.25 U.L.			HIGH	LOW		
-0 -/ ····gioto: outpute (************************************	-	Data Inputs	0.5 U.L.	0.25 U.L. 0.25 U.L. 0.25 U.L. 5(2.5) U.L.		

NOTES:

- a. 1 TTL Unit Load (U.L.) = $40 \mu A$ HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

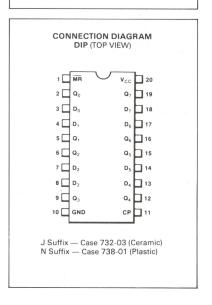
TRUTH TABLE

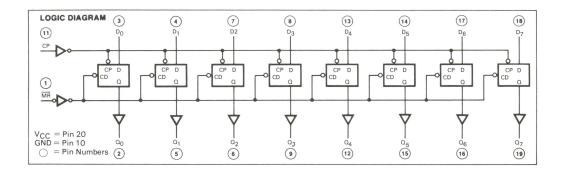
MR	СР	D _X	Ωx
L	Χ	Χ	L
Н		Н	н
Н		L	L

 $H = High \ Logic \ Level$

L = Low Logic Level

X = Immaterial





 $\begin{tabular}{ll} FUNCTIONAL DESCRIPTION — The $N54LS/74LS273$ is an 8-Bit Parallel Register with a common Clock and common Master Reset. \\ \end{tabular}$

When the \overline{MR} input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			LINUTO	TEGT CONDITIONS		
STIMBOL			MIN	TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
	1 1 0 14 1 1 1	54			0.7	.,		put LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
.,	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{I}$ or V_{IL} per Truth Table		
Vон		74	2.7	3.5		V			
.,	Output LOW Voltage	54,74		0.25	0.4	V		V _{CC} = V _{CC} MIN,	
VOL		74		0.35	0.5	V	I _{OL} = 8.0 mA	$V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table	
					20	μΑ	V _{CC} = MAX, \	/ _{IN} = 2.7 V	
lН	Input HIGH Current				0.1	mA	V _{CC} = MAX, \	_{IN} = 7.0 V	
IL	Input LOW Current				-0.4	mA	V _{CC} = MAX, \	/IN = 0.4 V	
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current				27	mA	V _{CC} = MAX		

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST COMPLETIONS	
STIVIBUL	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
fMAX	Maximum Input Clock Frequency	30	40		MHz	Fig. 1	
tPHL	Propagation Delay, MR to Q Output		18	27	ns	Fig. 2	
^t PLH ^t PHL	Propagation Delay, Clock to Output		17 18	27 27	ns	Fig. 1	

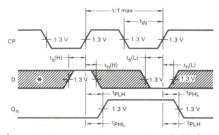
AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER	LIMITS			UNITS	TECT COMPITIONS	
	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_W	Pulse Width, Clock or Clear	20			ns	Fig. 1	
t _S	Data Setup Time	20			ns	Fig. 1	
th	Hold Time	5.0			ns	Fig. 1	
t _{rec}	Recovery Time	25			ns	Fig. 2	

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SETUP AND HOLD TIMES DATA TO CLOCK

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME



^{*}The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

CP 1.3 V 1.3 V 1.3 V 1.3 V 1.3 V 1.3 V

Fig. 2

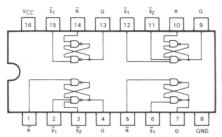
DEFINITION OF TERMS:

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

 $HOLD\ TIME\ (t_h)-is\ defined\ as\ the\ minimum\ time\ following\ the\ clock\ transition\ from\ LOW-to-HIGH\ that\ the\ logic\ level\ must\ be\ maintained\ at\ the\ input\ in\ order\ to\ ensure\ continued\ recognition.\ A\ negative\ HOLD\ TIME\ indicates\ that\ the\ correct\ logic\ level\ may\ be\ released\ prior\ to\ the\ clock\ transition\ from\ LOW-to-HIGH\ and\ still\ be\ recognized.$

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.





J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

TRUTH TABLE

1	NPUTS	OUTPUT	
S ₁	s ₂	R	(Q)
L	L	L	h
L	X	Н	H
X	L.	Н	H
Н	H	L	L
Н	Н	Н	No Change

- $$\begin{split} \mathsf{L} &= \mathsf{LOW} \ \mathsf{Voltage} \ \mathsf{Level} \\ \mathsf{H} &= \mathsf{HiGH} \ \mathsf{Voltage} \ \mathsf{Level} \\ \mathsf{X} &= \mathsf{Don't} \ \mathsf{Care} \\ \mathsf{h} &= \mathsf{The output} \ \mathsf{is} \ \mathsf{HiGH} \ \mathsf{as} \ \mathsf{long} \ \mathsf{as} \\ \mathsf{S}_1 \ \mathsf{or} \ \mathsf{S}_2 \ \mathsf{is} \ \mathsf{LOW}. \ \mathsf{If} \ \mathsf{all} \ \mathsf{inputs} \ \mathsf{go} \\ \mathsf{HiGH} \ \mathsf{simultaneously}, \ \mathsf{the output} \ \mathsf{state} \ \mathsf{is} \ \mathsf{indeterminate}, \ \mathsf{otherwise}, \\ \mathsf{it} \ \mathsf{follows} \ \mathsf{the} \ \mathsf{Truth} \ \mathsf{Table}. \end{split}$$

SN54LS279 **SN74LS279**

QUAD SET-RESET LATCH

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			LINUTO	TECT COMPITIONS	
STIVIBUL			MIN	TYP	MAX	UNITS	TEST CONDITIONS	
VIH	Input HIGH Voltage		2.0		l low	V	Guaranteed Input HIGH Voltage fo All Inputs	
.,	1	54			0.7	.,		put LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltag	ge		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$	
	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{I}$ or V_{IL} per Truth Table	
√он		74	2.7	3.5		V		
		54,74		0.25	0.4	V I _{OL} = 4.0 i	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA	V _{IN} = V _{IL} or V _{IH} per Truth Table
					20	μΑ	V _{CC} = MAX, V	_{IN} = 2.7 V
IH	Input HIGH Current				0.1	mA	V _{CC} = MAX, V	1 _{IN} = 7.0 V
IL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V	(IN = 0.4 V
OS	Short Circuit Current	- 17 15	-20		-100	mA	V _{CC} = MAX	
СС	Power Supply Current		-		7.0	mA	V _{CC} = MAX	

AC CHARACTERISTICS: $T_{\Delta} = 25^{\circ}C$

0)/14001	DARAMETER	LIMITS			UNITS	TEST CONDITIONS				
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS				
tPLH tPHL	Propagation Delay, \$\overline{S}\$ to Output		12 13	22 21	ns	V _{CC} = 5.0 V				
t _{PHL}	Propagation Delay, R to Output		15	27	ns	$C_L = 15 \text{ pF}$				



DESCRIPTION — The SN54LS/74LS280 is a Universal 9-Bit Parity Generator/Checker. It features odd/even outputs to facilitate either odd or even parity. By cascading, the word length is easily expanded.

The LS280 is designed without the expander input implementation, but the corresponding function is provided by an input at Pin 4 and the absence of any connection at Pin 3. This design permits the LS280 to be substituted for the LS180 which results in improved performance. The LS280 has buffered inputs to lower the drive requirements to one LS unit load.

- GENERATES EITHER ODD OF EVEN PARITY FOR NINE DATA LINES
- TYPICAL DATA-TO-OUTPUT DELAY OF ONLY 33 ns
- CASCADABLE FOR n-BITS
- CAN BE USED TO UPGRADE SYSTEMS USING MSI PARITY CIRCUITS
- TYPICAL POWER DISSIPATION = 80 mW

FUNCTON TABLE

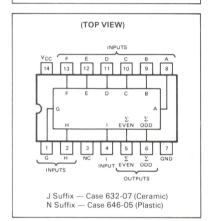
NUMBER OF INPUTS A	OUTPUTS			
THRU 1 THAT ARE HIGH	Σ EVEN	Σ ODD		
0, 2, 4, 6, 8	Н	L		
1, 3, 5, 7, 9	L	Н		

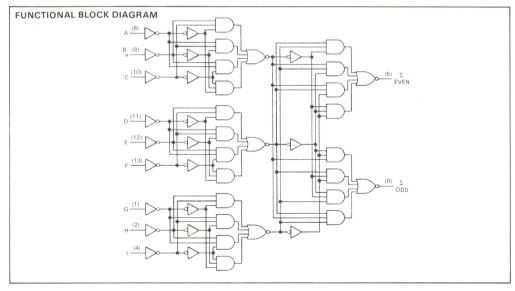
H = high level, L = low level

SN54LS280 SN74LS280

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

LOW POWER SCHOTTKY





GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL			LIMITS			UNITS	TEGT CONDITIONS			
SYMBOL			MIN	TYP	MAX	UNITS	TEST CONDITIONS			
VIH			2.0			V	Guaranteed In All Inputs	put HIGH Voltage for		
		54			0.7	.,		put LOW Voltage for		
VIL	Input LOW Voltage	74			0.8	V	All Inputs			
VIK	Input Clamp Diode Volta	ge		-0.65	-1.5	V	V _{CC} = MIN, III	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
		54	2.5	3.5		V		$V_{CC} = MIN$, $I_{OH} = MAX$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table		
VOH	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Trut			
. ,		54,74		0.25	0.4	V		$V_{CC} = V_{CC} MIN$,		
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA	$V_{IN} = V_{IL}$ or V_{IH} per Truth Table		
					20	μ A	V _{CC} = MAX, V	$V_{1N} = 2.7 \text{ V}$		
IH	Input HIGH Current				0.1	mA	V _{CC} = MAX, V	$V_{CC} = MAX$, $V_{IN} = 7.0 V$		
IL	Input LOW Current			-0.4	mA	V _{CC} = MAX, V	V _{CC} = MAX, V _{IN} = 0.4 V			
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX			
lcc	Power Supply Current				27	mA	V _{CC} = MAX			

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

CVAADOL	DADAMETER	LIMITS			LINITO	TEGT CONDITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t _{PLH}	Propagation Delay, Data to Output $\Sigma {\sf EVEN}$		33 29	50 45	ns	C _I = 15 pF	
t _{PLH}	Propagation Delay, Data to Output Σ ODD		23 31	35 50	ns	3 <u>.</u>	



DESCRIPTION — The SN54LS/74LS283 is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words $(A_1-A_4,\,B_1-B_4)$ and a Carry Input (C_0) . It generates the binary Sum outputs ($\Sigma_1 - \Sigma_4$) and the Carry Output (C₄) from the most significant bit. The LS283 operates with either active HIGH or active LOW operands (positive or negative logic).

SN54LS283 SN74LS283

4-BIT BINARY FULL ADDER WITH FAST CARRY

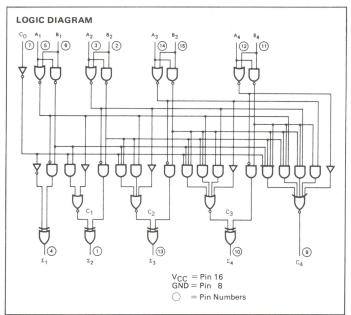
LOW POWER SCHOTTKY

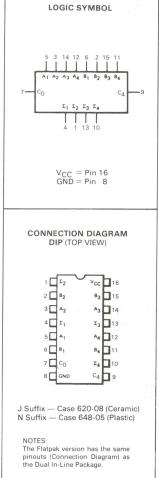
LOADING (Note a) HIGH LOW Operand A Inputs $A_1 - A_4$ 1.0 U.L. 0.5 U.L. $B_1 - B_4$ Operand B Inputs 1.0 U.L. 0.5 U.L. c_0 Carry Input 0.5 U.L. 0.25 U.L. $\Sigma_1 - \Sigma_4$ Sum Outputs (Note b) 10 U.L. 5(2.5) U.L. Carry Output (Note b) 10 U.L. 5(2.5) U.L.

NOTES:

PIN NAMES

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW. b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.





FUNCTIONAL DESCRIPTION — The LS283 adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C₄) outputs.

$$\text{C}_0 + (\text{A}_1 + \text{B}_1) + 2(\text{A}_2 + \text{B}_2) + 4(\text{A}_3 + \text{B}_3) + 8(\text{A}_4 + \text{B}_4) = \ \Sigma_1 + 2 \ \Sigma_2 + 4 \ \Sigma_3 + 8 \ \Sigma_4 + 16\text{C}_4$$
 Where: (+) = plus

Due to the symmetry of the binary add function the LS283 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Exam	nl	e

	CO	A ₁	A_2	Аз	A4	B ₁	B ₂	Вз	В4	Σ1	Σ_2	Σ_3	Σ_4	C4	
logic levels	L	L	Н	L	Н	Н	L	L	Н	Н	Н	L	L	Н	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(c

(10+9=19) (carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C_0 , A_1 , B_1 , can be arbitrarily assigned to pins 7, 5 or 3.

FUNCTIONAL TRUTH TABLE

C (n-1)	An	Bn	Σ_{n}	Cn
L	L	L	L	L
L	L	Н	Н	L
L	Н	L	Н	L
L	Н	Н	L	Н
Н	L	L	Н	L
Н	L	Н	L	Н
Н	Н	L	L	Н
Н	Н	Н	Н	Н

C₁ — C₃ are generated internally

Co is an external input

C4 is an output generated internally

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
loн	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS			
STIVIBUL	PARAIVIETE	:n	MIN	TYP	MAX	UNITS	1531	CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for		
.,		54			0.7			put LOW Voltage for		
VIL	Input LOW Voltage	74	-		0.8	V	All Inputs			
√IK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, III	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
		54	2.5	3.5		V		$_{OH} = MAX, V_{IN} = V_{IH}$		
√он	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Truth Table			
		54,74		0.25	0.4	V	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN,$		
/OL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table		
		CO			20	μΑ	$V_{CC} = MAX, V$	/INI = 2.7 V		
IH	Input HIGH Current	Any A or B			40	μΑ	1	IIV - 2.7 V		
III	pat morroanont	CO			0.1	mA	Vac = MAX V	/IN = 7 0 V		
	*	Any A or B			0.2	mA	$V_{CC} = MAX, V_{IN} = 7.0 V$			
IL	Input LOW Current	CO			-0.4	mA	Voc = MAX V	/INI = 0.4 V		
IL	Imput LOVV Current	Any A or B			-0.8	mA	$V_{CC} = MAX, V_{IN} = 0.4 V$			
os	Short Circuit Current		-20		-100	mA	V _{CC} = MAX			
	Power Supply Current									
CC	Total, Output HIGH				34	mA	$V_{CC} = MAX$			
	Total, Output LOW	* *			39	111/4	ACC = INIMX			

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

CVAADOL	DADAMETER	LIMITS			UNITS	CONDITIONS		
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS		
^t PLH ^t PHL	Propagation Delay, C_0 Input to Any Σ Output		16 15	24 24	ns			
tPLH tPHL	Propagation Delay, Any A or B Input to Σ Outputs		15 15	24 24	ns	$C_{l} = 15 pF$		
^t PLH ^t PHL	Propagation Delay, Co Input to C4 Output		11 11	17 22	ns	Figures 1 and 2		
^t PLH ^t PHL	Propagation Delay, Any A or B Input to C ₄ Output		11 12	17 17	ns			

AC WAVEFORMS

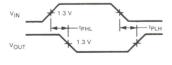


Fig. 1

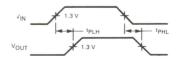


Fig. 2



 ${ t DESCRIPTION}$ — The SN54LS/74LS290 and SN54LS/74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS290) or divide-by-eight (LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{\text{CP}}$) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the LS290 also has a 2-input gated Master Set (Preset 9).

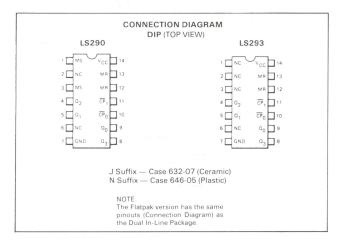
- CORNER POWER PIN VERSIONS OF THE LS90 and LS93
- LOW POWER CONSUMPTION . . . TYPICALLY 45 mW
- HIGH COUNT RATES . . . TYPICALLY 42 MHz
- CHOICE OF COUNTING MODES . . . BCD, BI-QUINARY, BINARY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION **EFFECTS**

	PIN	NAMES	
--	-----	-------	--

		HIGH	LOW
CP ₀	Clock (Active LOW going edge) Input to ÷2 Section.	0.05 U.L.	1.5 U.L.
^{CP} 1	Clock (Active LOW going edge) Input to ÷5 Section (LS290).	0.05 U.L.	2.0 U.L.
CP ₁	Clock (Active LOW going edge) Input to ÷8 Section (LS293).	0.05 U.L.	1.0 U.L.
MR ₁ , MR ₂	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1 , MS_2	Master Set (Preset-9, LS290) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5(2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 & ÷8 Sections (Note b)	10 U.L.	5(2.5) U.L.

LOADING (Note a)

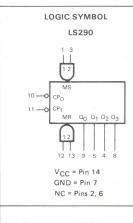
- a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
 b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
- c. The Q₀ Outputs are guaranteed to drive the full fan-out plus the $\overline{\text{CP}}_1$ Input of the device.

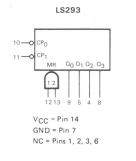


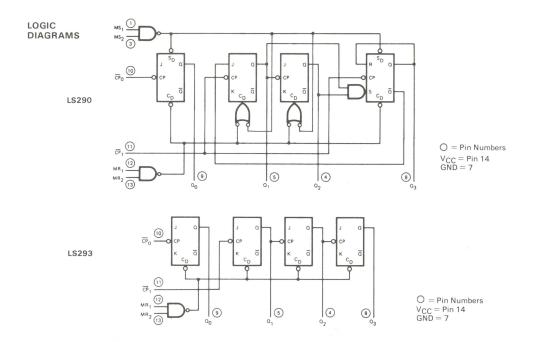
SN54LS/74LS290 SN54LS/74LS293

DECADE COUNTER: **4-BIT BINARY COUNTER**

LOW POWER SCHOTTKY







FUNCTIONAL DESCRIPTION — The LS290 and LS293 are 4-bit ripple type Decade, and 4-Bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS290) or divide-by-eight (LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Ω_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{\text{CP}}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

LS290

- A. BCD Decade (8421) Counter the $\overline{\text{CP}}_1$ input must be externally connected to the Q_0 output. The $\overline{\text{CP}}_0$ input receives the incoming count and a BCD count sequence is produced.
- B. Symmetrical Bi-quinary Divide-By-Ten Counter The Ω_3 output must be externally connected to the $\overline{\text{CP}}_0$ input. The input count is then applied to the $\overline{\text{CP}}_1$ input and a divide-by-ten square wave is obtained at output Ω_0 .
- C. Divide-By-Two and Divide-By-Five Counter No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function $(\overline{\mathsf{CP}}_0$ as the input and Q_0 as the output). The $\overline{\mathsf{CP}}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

1 \$293

- A. 4-Bit Ripple Counter The output Q_0 must be externally connected to input \overline{CP}_1 . The input count pulses are applied to input \overline{CP}_0 . Simultaneous division of 2, 4, 8, and 16 are performed at the Q_0 , Q_1 , Q_2 , and Q_3 outputs as shown in the truth table.
- B. 3-Bit Ripple Counter The input count pulses are applied to input \overline{CP}_1 . Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1 , Q_2 , and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS290 MODE SELECTION

RE	SET/SI	ET INPL	JTS		OUT	PUTS		
MR ₁	MR ₂	MS ₁ MS ₂		α ₀	Ω ₁	Q_2	σ^3	
Н	Н	L	Х	L	L	L	L	
Н	Н	X	L	L	L	L	L	
X	X	Н	Н	Н	L	L	Н	
L	X	L	X	Count				
X	L	X	L	Count				
L	X	X	L	Count				
X	L	L	X		Co	unt		

LS293 MODE SELECTION

	SET UTS		OUT	PUTS			
MR ₁	MR ₂	α ₀	α ₁	Q_2	σ^3		
Н	Н	L	L	L	L		
L	Н		Cou	ınt			
Н	L		Cou	ınt			
L	L		Cou	ınt			

LS290 BCD COUNT SEQUENCE

COUNT		OUT	PUT	
COUNT	Q_0	Q ₁	Q_2	$oldsymbol{Q}_3$
0	L	L	L	L
1	,H	L	L	L
2	L	Н	L	L
3	Н	Н	L	L
4	L	L	Н	L
5	Н	Ļ	Н	L
6	L	Н	Н	L
7	Н	Н	Н	L
8	L	L	L	Н
9	Н	L	L	Н

NOTE: Output Qo is connected to Input CP₁ for BCD count.

H = HIGH Voltage Level L = LOW Voltage Level X = Don't Care

TRUTH TABLE

COUNT		OUT	PUT	
COONT	Q_0	Q_1	Q_2	σ_3
0	L	L	L	L
1	Н	L	L	L
2	L	Н	L	L
3	Н	Н	L	L
4	L	L	Н	L
5	Н	L	Н	L
6	L	Н	Н	L
7	Н	Н	Н	L
8	L	L	L	Н
9	Н	L	L	Н
10	L	Н	L	Н
11	Н	Н	L	Н
12	L	L	Н	Н
13	Н	L	Н	Н
14	L	Н	Н	Н
15	Н	Н	Н	Н

Note: Output Q₀ connected to input CP₁.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
IOH	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	PARAMETER		LIMITS			LINUTC	TEST CONDITIONS	
SYMBOL	PARAIVIETER	ı	MIN	TYP	MAX	UNITS	TEST	ONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp All Inputs	ut HIGH Voltage for
		54			0.7	.,		ut LOW Voltage for
V _{IL}	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN}	= - 18 mA
Voн	Output HIGH Voltage	54	2.5	3.5		V		$H = MAX, V_{IN} = V_{IH}$
VОН	Output man voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table
	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
					20	μΑ	V _{CC} = MAX, V _I	N = 2.7 V
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX, V_I$	N = 7.0 V
I _{IL}	Input LOW Current MS, MR CPO CP1 (LS290) CP1 (LS293)				- 0.4 - 2.4 - 3.2 - 1.6	mA	V _{CC} = MAX, V _I	N = 0.4 V
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX	
lcc	Power Supply Current				15	mA	V _{CC} = MAX	

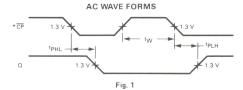
AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0$ V, $C_L = 15$ pF

	k of the first of the second o	LIMITS							
SYMBOL	PARAMETER	LS290			LS293			UNITS	
			TYP	MAX	MIN	TYP	MAX		
fMAX	CPO Input Clock Frequency	32			32			MHz	
fMAX	CP ₁ Input Clock Frequency	16			16			MHz	
^t PLH ^t PHL	Propagation Delay, CP ₀ Input to Q ₀ Output		10 12	16 18		10 12	16 18	ns	
t _{PLH} t _{PHL}	CP ₀ Input to Q ₃ Output		32 34	48 50		46 46	70 70	ns	
^t PLH ^t PHL	CP ₁ Input to Q ₁ Output		10 14	16 21		10 14	16 21	ns	
^t PLH ^t PHL	CP ₁ Input to Q ₂ Output		21 23	32 35		21 23	32 35	ns	
^t PLH ^t PHL	CP ₁ Input to Q ₃ Output		21 23	32 35		34 34	51 51	ns	
^t PHL	MS Input to Q ₀ and Q ₃ Outputs		20	30				ns	
t _{PHL}	MS Input to Q ₁ and Q ₂ Outputs		26	40				ns	
tPHL	MR Input to Any Output		26	40		26	40	ns	

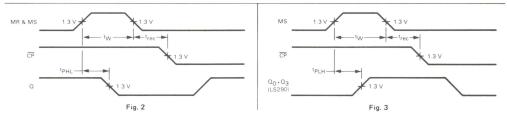
AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

				UNITS		
SYMBOL	PARAMETER	LS290				LS293
		MIN	MAX	MIN	MAX	
tW	CP ₀ Pulse Width	15		15		ns
tw	CP	30		30		ns
tw	MS Pulse Width	15				ns
tw	MR Pulse Width	15		15		ns
t _{rec}	Recovery Time MR to $\overline{\mathbb{CP}}$	25		25		ns

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.



 * The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.





DESCRIPTION — The SN54LS/74LS295A is a 4-Bit Shift Register with serial and parallel synchronous operating modes, and independent 3-state output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfers and shifting occur synchronous with the HIGH to LOW clock transition.

The 3-State output buffers are controlled by an active HIGH Output Enable input (EO). Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion.

The LS295A is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- NEGATIVE EDGE-TRIGGERED CLOCK INPUT
- PARALLEL ENABLE MODE CONTROL INPUT
- 3-STATE BUSSABLE OUTPUT BUFFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

PIN NAMES		LOADING	(Note a)
		HIGH	LOW
PE	Parallel Enable Input	0.5 U.L.	0.25 U.L.
DS	Serial Data Input	0.5 U.L.	0.25 U.L.
P0-P3	Parallel Data Input	0.5 U.L.	0.25 U.L.
E _O CP	Output Enable Input	0.5 U.L.	0.25 U.L.
CP	Clock Pulse (Active LOW Going	0.5 U.L.	0.25 U.L.
	Edge) Input		
$Q_0 - Q_3$	3-State Outputs (Note b)	10(25) U.L.	5(2.5) U.L.

NOTES:

a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

SN54LS295A SN74LS295A

4-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

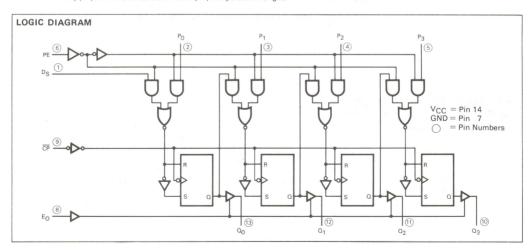
CONNECTION DIAGRAM DIP (TOP VIEW)

1 🗆	DS	vcc	1 14
2	P ₀	α0	13
3	P ₁	Ω1	12
4	P ₂	02	11
5	P ₃	σ3	10
6	PE	CP	9
7	GND	EO	8

J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

NOTE

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



 $\label{eq:FUNCTIONAL DESCRIPTION} The LS295A is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial Data (DS) and four Parallel Data (PO-P3) inputs and four parallel 3-State output buffers (QO-Q3). When the Parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data Inputs (PO-P3) into the register synchronous with the HIGH to LOW transition of the Clock (CP). When the PE is LOW, a HIGH to LOW transition on the clock transfers the serial data on the DS input to register Q0, and shifts data from Q0 to Q1, Q1 to Q2 and Q2 to Q3. The input data and parallel enable are fully edge-triggered and must be stable only one set-up time before the HIGH to LOW clock transition.$

The 3-State output buffers are controlled by an active HIGH Output Enable input (E $_{O}$). When the E $_{O}$ is HIGH, the four register outputs appear at the Q $_{O}$ —Q $_{3}$ outputs. When E $_{O}$ is LOW, the outputs are forced to a high impedance "off" state. The 3-State output buffers are completely independent of the register operation, i.e., the input transitions on the E $_{O}$ input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-State devices whose outputs are tied together are designed so there is no overlap.

MODE SELECT - TRUTH TABLE

00504744046		INP	UTS			OUTP	UTS*	
OPERATING MODE	PE	CP	DS	Pn	σ0	Q ₁	Q_2	σ^3
Shift Right	1	Z	1	×	L	q ₀	Q ₂ Q ₃ q ₁ q ₂ q ₁ q ₂	
Silit Right	1	Z	h	X	Н	q_0	91	q_2
Parallel Load	h	7	×	Pn	P ₀	P ₁	P ₂	p ₃

^{*}The indicated data appears at the Q outputs when E_Q is HIGH. When E_Q is LOW, the indicated data is loaded into the register, but the outputs are all forced to the high impedance "off" state.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lor	Output Current — Low	54 74			4.0 8.0	mA

L = LOW Voltage Levels

H = HIGH Voltage Levels

X = Don't Care

 $p_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

I = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.

h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST COMPITIONS	
STIVIBUL	PARAIVIETER	1	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
	1	54			0.7	.,	Guaranteed Input LOW Voltage for	
V _{IL}	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = MIN$, $I_{IN} = -18 \text{ mA}$	
		54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH}$	
Vон	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN},$	
VOL		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table	
lozh	Output Off Current HIGH				20	μΑ	V _{CC} = MAX, V _{OUT} = 2.4 V	
lozL	Output Off Current LOW				-20	μΑ	$V_{CC} = MAX$, $V_{OUT} = 0.4 V$	
lін	Input HIGH Current				20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$	
'IH	Input mon current				0.1	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$	
IIL	Input LOW Current				-0.4	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$	
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
	Power Supply Current						$V_{CC} = MAX$, $E_0 = 4.5 \text{ V}$, \overline{CP} momentary 3.0 V, then GND	
lcc	Total, Output HIGH				29	mA	$V_{CC} = MAX, E_O = GND, \overline{CP} = GNE$	
	Total, Output LOW			33	1	VCC - IVIAX, EO = GIND, CP = GIND		

AC CHARACTERISTICS: $T_A = 25$ °C

CVMPOL	PARAMETER		LIMITS		LINUTC	TECT COMPITIONS
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
fMAX	Maximum Clock Frequency	30	45		MHz	
t _{PLH}	Propagation Delay Clock to Output		14 19	20 30	ns	0 - 15 - 5
^t PZH	Output Enable Time to HIGH LEVEL		18	26	ns	$C_L = 15 \text{ pF}$ $V_{CC} = 5.0 \text{ V}$
^t PZL	Output Enable Time to LOW Level		20	30	ns	
[†] PLZ	Output Disable Time from LOW Level		13	20	ns	C. — F.OF
^t PHZ	Output Disable Time from HIGH Level		13	20	ns	$C_L = 5.0 \text{ pF}$

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER	LIMITS			UNITS	TECT COMPITIONS	
		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t₩	Clock Pulse Width	16			ns	V 5 0 V	
t_S	Data Setup Time	20			ns	$V_{CC} = 5.0 \text{ V}$	
th	Data Hold Time	0			ns	$C_L = 15 \text{ pF}$	

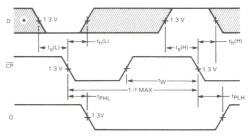
DEFINITION OF TERMS:

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

 $HOLD\ TIME\ (t_h) - is\ defined\ as\ the\ minimum\ time\ following\ the\ clock\ transition\ from\ HIGH\ to\ LOW\ that\ the\ logic\ level\ must\ be\ maintained\ at\ the\ input\ in\ order\ to\ ensure\ continued\ recognition.\ A\ negative\ HOLD\ TIME\ indicates\ that\ the\ correct\ logic\ level\ may\ be\ released\ prior\ to\ the\ clock\ transition\ from\ HIGH\ to\ LOW\ and\ still\ be\ recognized.$

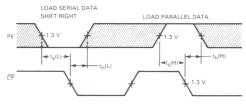
AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



*The Data Input is D_S for PE = LOW and P_n for PE = HIGH.

Fig. 1





DESCRIPTION — The SN54LS/74LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources.) The selected data is transferred to the output register synchronous with the HIGH to LOW transition of the Clock input.

The LS298 is fabricated with the Schottky barrier process for high speed and is completely compatible with all Motorola TTL families.

- SELECT FROM TWO DATA SOURCES
- FULLY EDGE-TRIGGERED OPERATION
- TYPICAL POWER DISSIPATION OF 65 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

SN54LS298 SN74LS298

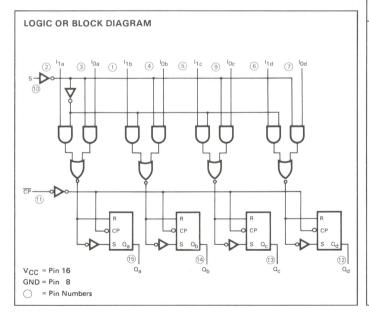
QUAD 2-INPUT MULTIPLEXER WITH STORAGE

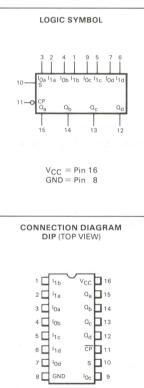
LOW POWER SCHOTTKY

PIN NAMES LOADING (Note a) HIGH LOW Common Select Input 0.5 U.L. 0.25 U.L. CP Clock (Active LOW Going Edge) Input 0.5 U.L. 0.25 U.L $l_{0a}-l_{0d}$ Data Inputs From Source 0 0.5 U.L. 0.25 U.L. I_{1a}—I_{1d} Data Inputs From Source 1 0.5 U.L. 0.25 U.L. Qa-Qd Register Outputs (Note b) 10 U.L. 5(2.5) U.L.

NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.





J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

NOTE

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

 $\label{eq:FUNCTIONAL DESCRIPTION} The LS298 is a high speed Quad 2-Port Register. It selects four bits of data from two sources (ports) under the control of a Common Select Input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH to LOW transition of the Clock input (\overline{CP}). The 4-bit output register is fully edge-triggered. The Data inputs (l) and Select input (S) must be stable only one setup time prior to the HIGH to LOW transition of the clock for predictable operation.$

TRUTH TABLE

	INPUTS	OUTPUT	
S	10	Q	
ı	1	X	L
1	h	X	Н
h	X	1	L
h	X	h	Н

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

I = LOW Voltage Level one setup time prior to the HIGH to LOW clock transition.

h = HIGH Voltage Level one setup time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lor	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

OVAADOL	DARAMETER	LIMITS			UNITS	TEGT COMPITIONS		
SYMBOL	PARAMETER	PARAMETER			MAX	UNITS	TEST CONDITIONS	
VIH	Input HIGH Voltage	2.0			V	Guaranteed In All Inputs	put HIGH Voltage for	
V _{IL} Input LOW V		54			0.7			put LOW Voltage for
	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltage	ge		-0.65	-1.5	V	V _{CC} = MIN, III	N = −18 mA
		54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{I}$ or V_{IL} per Truth Table	
Vон	Output HIGH Voltage	74	2.7	3.5		V		
		54,74		0.25	0.4	V		V _{CC} = V _{CC} MIN,
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
					20	μΑ	V _{CC} = MAX, V	/ _{IN} = 2.7 V
lН	Input HIGH Current				0.1	mA	V _{CC} = MAX, V	/ _{IN} = 7.0 V
IIL	Input LOW Current			-0.4	mA	V _{CC} = MAX, V	/ _{IN} = 0.4 V	
os	Short Circuit Current	-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current			21	mA	$V_{CC} = MAX$		

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER		LIMITS		UNITS	TEST CONDITIONS	
STIVIBUL	PARAIVIETER	MIN	TYP	MAX	UNITS		
tPLH	Propagation Delay,		18	27	ns	$V_{CC} = 5.0 V$	
^t PHL	Clock to Output		21	32	ns	$C_L = 15 pF$	

AC SETUP REQUIREMENTS: $T_{\Delta} = 25^{\circ}C$, $V_{CC} = 5.0 \text{ V}$

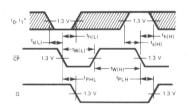
SYMBOL	PARAMETER		LIMITS		LINUTC	TEST CONDITIONS			
	PARAMETER	MIN	TYP	MAX	UNITS				
t₩	Clock Pulse Width	20			ns				
t _s	Data Setup Time	15			ns				
t _S	Select Setup Time	25			ns	$V_{CC} = 5.0 V$			
h	Data Hold Time	5.0			ns				
th	Select Hold Time	0							

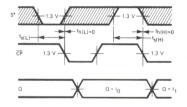
DEFINITIONS OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS





*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

Fig. 2



DESCRIPTION — The SN54LS/74LS299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

- COMMON I/O FOR REDUCED PIN COUNT
- FOUR OPERATION MODES: SHIFT LEFT, SHIFT RIGHT, LOAD AND STORE
- SEPARATE SHIFT RIGHT SERIAL INPUT AND SHIFT LEFT SERIAL INPUT FOR EASY CASCADING
- 3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

PIN NAMES		LOADIN	IG (Note a)
		HIGH	LOW
CP	Clock Pulse (active positive-going edge)		
	Input	0.5 U.L.	0.25 U.L.
DS ₀	Serial Data Input for Right Shift	0.5 U.L.	0.25 U.L.
DS ₇	Serial Data Input for Left Shift	0.5 U.L.	0.25 U.L.
I/On	Parallel Data Input or	0.5 U.L.	0.25 U.L.
1/On	Parallel Output (3-State) (Note c)	65(25) U.L.	15(7.5) U.L.
OE ₁ , OE ₂	3-State Output Enable (active LOW) Inputs	0.5 U.L.	0.25 U.L.
Q ₀ , Q ₇	Serial Outputs (Note b)	10 U.L.	5(2.5) U.L.
MR	Asynchronous Master Reset		
	(active LOW) Input	0.5 U.L.	0.25 U.L.
S ₀ , S ₁	Mode Select Inputs	1 U.L.	0.5 U.L.

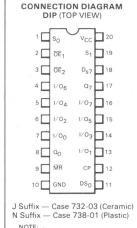
NOTES

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. c. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) , The Output HIGH
- drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

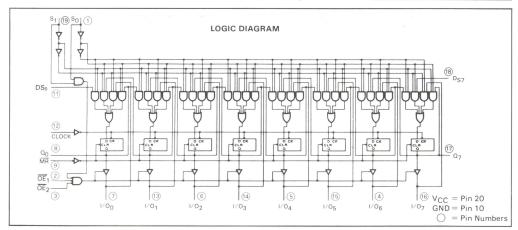
SN54LS299 SN74LS299

8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY



- NOTE:
- The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



GUARANTEED OPERATING RANGES

SYMBOL	PARAM	ETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage		54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temper	ature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	Ω ₀ , Ω ₇	54,74	7		-0.4	mA
loL	Output Current — Low	Q ₀ , Q ₇ Q ₀ , Q ₇	54 74			4.0 8.0	mA
ГОН	Output Current — High	I/0 ₀ —I/0 ₇ I/0 ₀ —I/0 ₇	54 74		x . x	-1.0 -2.6	mA
loL	Output Current — Low	I/0 ₀ —I/0 ₇ I/0 ₀ —I/0 ₇	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETE	-R	LIMITS			UNITS	TEST CONDITIONS		
	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		MIN	TYP	MAX				
VIH	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for	
\/	Input LOW Voltage	54			0.7	V		put LOW Voltage for	
VIL	Input LOVV Voltage	74	,		0.8	V	All Inputs		
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _I	N = -18 mA	
/он	Output HIGH Voltage	54	2.4	3.2		V	$V_{CC} = MIN, I_{C}$	u = MAX	
	1/00—1/07	74	2.4	3.1		V	100	vee wiiit, lon landt	
/он	Output HIGH Voltage	54	2.5	3.4		V	$V_{CC} = MIN, I_{C}$	NH = MAX	
	Ω ₀ , Ω ₇	74	2.7	3.4		V	100 1000		
	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$		
VOL	1/00—1/07	74		0.35	0.5	V	I _{OL} = 24 mA V _{IN} = V _{IL} or V _{IH} per Truth Table		
	Output LOW Voltage	54,74			0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$	
VOL	Q ₀ —Q ₇	74			0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
lozh	Output Off Current HIG	Н	-		40	μΑ	V _{CC} = MAX, V	OUT = 2.4 V	
lozL	Output Off Current LOV I/O ₀ —I/O ₇	V	>		-400	μΑ	V _{CC} = MAX, V	OUT = 0.4 V	
		Others			20	μΑ			
Ін	Input HIGH Current	S ₀ , S ₁ , I/O ₀ —I/O ₇			40	μΑ	$V_{CC} = MAX, V$	$I_{1N} = 2.7 \text{ V}$	
·III	Input man current	Others			0.1	mA	V _{CC} = MAX, \	/INI = 7 0 V	
		S ₀ , S ₁			0.2	mA	1000 101200,	/IN - 7.0 V	
		1/00-1/07			0.1	mA	V _{CC} = MAX, \	/ _{IN} = 5.5 V	
IIL	Input LOW Current	Others			-0.4	mA	V _{CC} = MAX, \	/INI = 0.4 V	
'IL	pat EOTT Garrott	S ₀ , S ₁			-0.8	mA	- 50 10000	- IIV	
los	Short Circuit Current	Q ₀ , Q ₇	-20		-100	mA	$V_{CC} = MAX$		
.03		1/00-1/07	-30		-130	mA	$V_{CC} = MAX$		
Icc	Power Supply Current	= = = = = = =			53	mA	V _{CC} = MAX		

FUNCTION TABLE

			INP	JTS				RESPONSE
MR	S ₁	S ₀	ŌĒ ₁	ŌE ₂	СР	DS ₀	DS ₇	
L L	X X H	X X H	X X	X H X	X X X	X X X	X X X	Asynchronous Reset; $Q_0 = Q_7 = LOW$ I/O Voltage Undetermined
L	L X	X L	L	L	X	X	X	Asynchronous Reset; Q ₀ = Q ₇ = LOW I/O Voltage LOW
Х	L	Н	X L	X L	7	D D	X X	Shift Right; $D\rightarrow Q_0$; $Q_0\rightarrow Q_1$; etc. Shift Right; $D\rightarrow Q_0$ & I/O_0 ; $Q_0\rightarrow Q_1$ & I/O_1 ; etc.
Н	Н	L	X L	.X L	7	X	D D	Shift Left; D \rightarrow Q ₇ ; Q ₇ \rightarrow Q ₆ ; etc. Shift Left; D \rightarrow Q ₇ & I/O ₇ ; Q ₇ \rightarrow Q ₆ & I/O ₆ ; etc.
Н	Н	Н	Х	X	7	X	X	Parallel Load; I/O _n →Q _n
Н	L L	L L	H X	X H	X X	X X	X X	Hold: I/O Voltage undetermined
Н	L	L	L	L	X	X	X	Hold: $I/O_n = Q_n$

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

AC CHARACTERISTICS: $T_A = 25^{\circ}C$, $V_{CC} = 5.0 \text{ V}$

TO OTIATIA	TEMISTICS. 1A - 25 C, VCC - 5.0	V					
SYMBOL	DADAMETER		LIMITS		LINUTC	TEST COMPITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
fMAX	Maximum Clock Frequency	25	35		MHz		
^t PHL ^t PLH	Propagation Delay, Clock to Q ₀ or Q ₇		26 22	39 33	ns	$C_{\rm I} = 15 \rm pF$	
^t PHL	Propagation Delay, Clear to Q ₀ or Q ₇		27	40	ns	, st. 10 p.	
^t PHL ^t PLH	Propagation Delay, Clock to I/O ₀ — I/O ₇		26 17	39 25	ns	C _I = 45 pF,	
^t PHL	Propagation Delay, Clear to I/O ₀ — I/O ₇		26	40	ns	$R_{\rm I} = 667 \Omega$	
^t PZH ^t PZL	Output Enable Time		13 19	21 30	ns	n_ = 307 12	
^t PHZ ^t PLZ	Output Disable Time		10 10	15 15	ns	C _L = 5.0 pF	

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

CVAADOL	DADAMETER		LIMITS		LINUTC	TEST CONDITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS		
tw	Clock Pulse Width HIGH	30			ns		
tw	Clock Pulse Width LOW	10			ns		
tw	Clock Pulse Width LOW	20			ns		
t _S	Data Setup Time	20			ns	$V_{CC} = 5.0 \text{ V}$	
t _S	Select Setup Time	35			ns	VCC = 3.0 V	
th	Data Hold Time	0			ns		
th	Select Hold Time	10			ns		
t _{rec}	Recovery Time	20			ns		

DEFINITION OF TERMS:

SETUP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.



DESCRIPTION — These 8-bit shift registers have multiplexed input/output data ports to accomplish full 8-bit data handling in a single 20-pin package. Serial data may enter the shift-right register through either D0 or D1 inputs as selected by the data select pin. A serial output is also provided. Synchronous parallel loading is achieved by taking the register enable and the S/\overline{P} inputs low. This places the three-state input/output ports in the data input mode. Data is entered on the low-to-high clock transition. The data extend function repeats the sign in the Q_{A} flip-flop during shifting. An overriding clear input clears the internal registers when taken low whether the outputs are enabled or off. The output enable does not affect synchronous operation of the register.

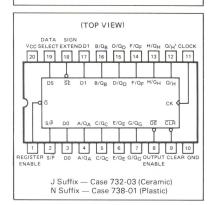
- MULTIPLEXED INPUTS/OUTPUTS PROVIDE IMPROVED BIT DENSITY
- SIGN EXTEND FUNCTION
- DIRECT OVERRIDING CLEAR
- 3-STATE OUTPUTS DRIVE BUS LINES DIRECTLY

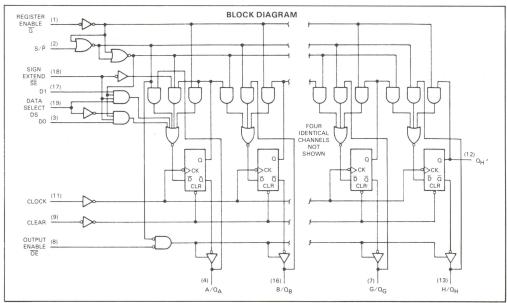
MC 3487

SN54LS322A SN74LS322A

8-BIT SHIFT REGISTERS WITH SIGN EXTEND

LOW POWER SCHOTTKY





GUARANTEED OPERATING RANGES

SYMBOL	PARAM	ETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V	
ТД	Operating Ambient Temper	ature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	QH'	 54,74		o expli	-0.4	mA
lOL	Output Current — Low	Ω _H ′ Ω _H ′	54 74			4.0 8.0	mA
ГОН	Output Current — High	Ω _A —Ω _H Ω _A —Ω _H	54 74			-1.0 -2.6	mA
loL	Output Current — Low	Ω _A —Ω _H Ω _A —Ω _H	54 74		01 1	12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMADOL	DADAME	TED		LIMITS		UNITS	TECT	CONDITIONS			
SYMBOL	PARAME	IEK	MIN	TYP	MAX	UNITS	TEST CONDITIONS				
VIH	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for			
	1	54			0.7	V	Guaranteed Input LOW Voltage for				
VIL	Input LOW Voltage	74			0.8	V	All Inputs				
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{II}	N = -18 mA			
Vон	Output HIGH Voltage	54	2.4	3.2		V	$V_{CC} = MIN, I_{C}$	$_{DH} = MAX$			
	QA-QH	74	2.4	3.2		V	00	VCC WIN, IOH WICK			
√он	Output HIGH Voltage 54		2.5	3.4		V	$V_{CC} = MIN, IC$	ou = MAX			
	QH'	74	2.7	3.4		V	1000 1011111, 10)H 141/ 01			
	Output LOW Voltage	54,74		0.25	0.4	V	I _{OL} = 12 mA	$V_{CC} = V_{CC} MIN,$			
VOL	QA-QH	74	-7,0	0.35	0.5	V	I _{OL} = 24 mA V _{IN} = V _{IL} or V per Truth Tabl				
.,	Output LOW Voltage	54,74			0.4	V	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN,$			
VOL	Q _H ′	74			0.5	V	I _{OL} = 8.0 mA V _{IN} = V _{IL} or per Truth Tal				
lozh	Output Off Current HIGH QA-QH				40	μΑ	V _{CC} = MAX, \	/ _{OUT} = 2.4 V			
lozL	Output Off Current LC)W			-400	μΑ	V _{CC} = MAX, V	OUT = 0.4 V			
		Other			20	μΑ	$V_{CC} = MAX, V_{IN} = 2.7 V$				
		A-H, Data Select			40	μΑ					
I _{IH}	Input HIGH Current	Sign Extend			60	μΑ					
		Other			0.1	mA					
		Data Select			0.2	mA	$V_{CC} = MAX, V$	$I_{1N} = 7.0 \text{ V}$			
		Sign Extend			0.3	mA					
	1	A-H			0.1	mA	V _{CC} = MAX, V	/ _{IN} = 5.5 V			
		Other			-0.4	mA					
IIL	Input LOW Current	Data Select			-0.8	mA	$V_{CC} = MAX, V$	$I_{1N} = 0.4 \text{ V}$			
		Sign Extend			-1.2	mA					
los	Short Circuit Current	QH'	-20		-100	mA	$V_{CC} = MAX$				
		Q _A -Q _H	-30		-130	mA	$V_{CC} = MAX$				
Icc	Power Supply Current				60	mA	$V_{CC} = MAX$				

FUNCTION TABLE

7.				INPUTS				- 1	NPUTS/0	OUTPUT	S	OUTDUT
OPERATION	CLEAR	REGISTER ENABLE	S/P	SIGN EXTEND	DATA SELECT	OUTPUT ENABLE	CLOCK	A/QA	B/QB	c/Qc.	. н/он	OUTPUT QH'
Clear	L	Н	X	×	X	L	X	L	L	L	L	L
Clear	L	×	Н	×	X	L	X	L	L	L	L	L
Hold	Н	Н	Х	×	X	L	X	Q _{A0}	Q _{B0}	GC0	QH0	QH0
Shift Right	Н	L	Н	Н	L	L	1	D0	QAn	QBn	QGn	QGn
Jillit Hight	Н	L	Н	н	н	L	1	D1	QAn	QBn	Q_{Gn}	Q_{Gn}
Sign Extend	Н	L	Н	L	X	L	↑	Q _{An}	QAn	QBn	Q_{Gn}	QGn
Load	Н	L	L	X	X	X	1	а	b	С	h	' h .

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/P input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

- H = high level (steady state)
- L = low level (steady state)
- X = irrelevant (any input, including transitions)
- ↑ = transition from low to high level
- $Q_{A0} \dots Q_{H0}$ = the level of Q_A through Q_H , respectively, before the indicated steady-state conditions were established $Q_{An} \dots Q_{Hn}$ = the level of Q_A through Q_{H} , respectively, before the most recent \uparrow transition of the clock D0, D1 = the level of steady-state inputs at inputs D0 and D1 respectively
- a . . . h = the level of steady-state inputs at inputs A through H respectively

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

0)/440.01	DARAMETER		LIMITS		LINUTO	TEST SOMBITIONS
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
fMAX	Maximum Clock Frequency	25	35		MHz	
tPHL tPLH	Propagation Delay, Clock to QH'		26 22	35 33	ns	C _L = 15 pF
tPHL	Propagation Delay, Clear to QH'		27	35	ns	
tPHL tPLH	Propagation Delay, Clock to Q _A -Q _H		22 16	33 25	ns	
tPHL	Propagation Delay, Clear to Q _A -Q _H		22	35	ns	$C_L = 45 \text{ pF},$ $R_L = 667 \Omega$
^t PZH ^t PZL	Output Enable Time	1 4.4	15 15	35 35	ns	
^t PHZ ^t PLZ	Output Disable Time		15 15	25 25	ns	C _L = 5.0 pF

AC SETUP REQUIREMENTS: $T_{\Delta} = 25^{\circ}C$, $V_{CC} = 5.0 \text{ V}$

CVAADOL	DADAMETER		LIMITS		LINUTC	TEST CONDITIONS
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
tw	Clock Pulse Width HIGH	30			ns	
tw	Clock Pulse Width LOW	10			ns	
tW	Clear Pulse Width LOW	20			ns	
t _S	Data Setup Time	20			ns	V
t _S	Select Setup Time	10			ns	$V_{CC} = 5.0 \text{ V}$
th	Data Hold Time	0			ns	
th	Select Hold Time	10			ns	
t _{rec}	Recovery Time	20			ns	

DEFINITION OF TERMS:

SETUP TIME ts is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME th is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

 $\textbf{RECOVERYTIME} \ \ t_{\textbf{rec}} \ \ \text{is defined as the minimum time required between the end of the reset pulse and the clock transition from the recovery of the reset pulse and the clock transition from the recovery of the reset pulse and the clock transition from the recovery of the reset pulse and the clock transition from the recovery of the$ LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.



DESCRIPTION — The SN54LS/74LS323 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Its function is similar to the SN54LS/74LS299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate inputs and outputs are provided for flip-flops Q₀ and Q₇ to allow easy cascading.

Four operation modes are possible: hold (store), shift left, shift right, and parallel load. All modes are activated on the LOW-to-HIGH transition of the Clock

- COMMON I/O FOR REDUCED PIN COUNT
- FOUR OPERATION MODES: SHIFT LEFT, SHIFT RIGHT, PARALLEL LOAD AND STORE
- \bullet SEPARATE CONTINUOUS INPUTS AND OUTPUTS FROM Q_0 AND Q_7 ALLOW EASY CASCADING
- FULLY SYNCHRONOUS RESET
- 3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

PIN NAME	S	LOADIN	G (Note a)
		HIGH	LOW
CP	Clock Pulse (active positive-going edge) Input	0.5 U.L.	0.25 U.L.
DS _O	Serial Data Input For Right Shift	0.5 U.L.	0.25 U.L.
DS ₇	Serial Data Input For Left Shift	0.5 U.L.	0.25 U.L.
I/On	Parallel Data Input or	1.0 U.L.	0.5 U.L.
	Parallel Output (3-State) (Note c)	65(25) U.L.	15(7.5) U.L.
\overline{OE}_1 , \overline{OE}_2	3-State Output Enable (active LOW) Inputs	0.5 U.L.	0.25 U.L.
Q ₀ , Q ₇	Serial Outputs (Note b)	10 U.L.	5(2.5) U.L.
S ₀ , S ₁ SR	Mode Select Inputs	1 U.L.	
SR	Synchronous Reset (active LOW) Input	0.5 U.L.	0.25 U.L.

NOTES:

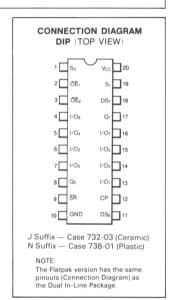
- a. 1 TTL LOAD = . 40 μ A HIGH/1.6 mA LOW.
- The output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial Temperature Ranges.
- The output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial Temperature Ranges.

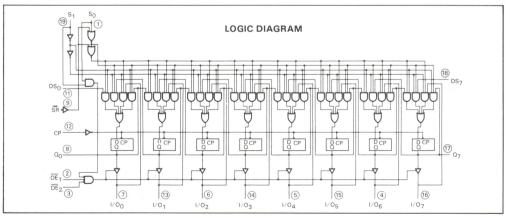
The output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial Temperature Ranges.

SN54LS323 SN74LS323

8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY





FUNCTIONAL DESCRIPTION The logic diagram and truth table indicate the functional characteristics of the SN54LS/74LS323 Universal Shift/Storage Register. This device is similar in operation to the SN54LS/74LS299 except for synchronous reset. A partial list of the common features are described below:

- 1. They use eight D-type edge-triggered flip-flops that respond only to the LOW-to-HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control (S₀, S₁) and data inputs (DS₀, DS₇, I/O₀-I/O₇) may be stable at least a setup time prior to the positive transition of the Clock Pulse.
- 2. When $S_0 = S_1 = 1$, $I/O_0 I/O_7$ are parallel inputs to flip-flops $Q_0 Q_7$ respectively, and the outputs of $Q_0 Q_7$ are in the high impedance state regardless of the state of \overline{OE}_1 or \overline{OE}_2 .

An important unique feature of the SN54LS/74LS323 is a fully Synchronous Reset that requires only to be stable at least one setup time prior to the positive transition of the Clock Pulse.

TRUTH	TABLE	

			INPL	JTS				RESPONSE
SR	S ₁	S ₀	ŌĒ1	ŌĒ2	СР	DS ₀	DS7	
L L	X X H	X X H	H X X	X H X	7 7 7	X X X	X X	Synchronous Reset; Q ₀ = Q ₇ = LOW I/O voltage undetermined
L	L X	X L	L	L L	7	X X	X X	Synchronous Reset; Q ₀ = Q ₇ = LOW I/O voltage LOW
Н	L L	Н	X L	X L	7	D.	X X	Shift Right; $D\rightarrow Q_0$; $Q_0\rightarrow Q_1$; etc. Shift Right; $D\rightarrow Q_0$ & I/O_0 ; $Q_0\rightarrow Q_1$ & I/O_1 ; etc.
Н	Н	L	X L	X L	7	X X	D ′	Shift Left; $D \rightarrow Q_7$; $Q_7 \rightarrow Q_6$; etc. Shift Left; $D \rightarrow Q_7 \& I/O_7$; $Q_7 \rightarrow Q_6 \& I/O_6$; etc.
Н	Н	Н	X	Х	T	Х	×	Parallel Load I/O _n →Q _n
Н	L L	L	H X	Х	X X	X	X X	Hold; I/O Voltage Undetermined
Н	L	L	L	L	Х	Х	Х	Hold; I/O _n = Q _n

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

GUARANTEED OPERATING RANGES

SYMBOL	PARAMET	ER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage		54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperate	ure Range	54 74	-55 0	25 25	125 70	°C
Іон -	Output Current — High	Ω ₀ , Ω ₇	54,74		-	-0.4	mA
lor	Output Current — Low	Ω ₀ , Ω ₇ Ω ₀ , Ω ₇	54 74			4.0 8.0	mA
ГОН	Output Current — High	1/0 ₀ —1/0 ₇ 1/0 ₀ —1/0 ₇	54 74			-1.0 -2.6	mA
lOL	Output Current — Low	I/0 ₀ —I/0 ₇ I/0 ₀ —I/0 ₇	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETE	· D		LIMITS		UNITS	TECT	CONDITIONS	
STIVIBUL	PARAIVIETE	:n	MIN	TYP	MAX	UNITS	IESI	CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for	
. /	1	54		×	0.7			nput LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	$V_{CC} = MIN, I_{II}$	$_{N} = -18 \text{ mA}$	
VOH	Output HIGH Voltage	54	2.4	3.2		V	VCC = MIN, IC	u = MAX	
-011	1/00-1/07	74	2.4	3.1		V	100)n	
VOH	Output HIGH Voltage	54	2.5	3.4		V	V _{CC} = MIN, I _C	M = MAX	
	Ω ₀ ,Ω ₇	74	2.7	3.4		V	VCC - WINA, 1C	DH — IVIAA	
	Output LOW Voltage	54,74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN,	
VOL	1/00-1/07	74		0.35	0.5	V	I _{OL} = 24 mA V _{IN} = V _{IL} or V _{II} per Truth Table		
	Output LOW Voltage	54,74			0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN,	
VOL	Q ₀ -Q ₇	74			0.5	V	I _{OL} = 8.0 mA V _{IN} = V _{IL} or per Truth Tal		
lozh	Output Off Current HIGI I/O ₀ -I/O ₇	Н			40	μΑ	V _{CC} = MAX, V	OUT = 2.4 V	
OZL	Output Off Current LOV 1/0 ₀ -1/0 ₇	V			-400	μΑ	V _{CC} = MAX, V	OUT = 0.4 V	
		Others			20	μΑ			
Ін	Input HIGH Current	S ₀ , S ₁ , I/O ₀ -I/O ₇			40	μΑ	$V_{CC} = MAX, V$	$I_{1N} = 2.7 \text{ V}$	
1111		Others			0.1	mA	V _{CC} = MAX, \	/IN = 7 0 V	
		S ₀ , S ₁			0.2	mA	1000	7.0 V	
		1/00-1/07			0.1	mA	V _{CC} = MAX, \	/ _{IN} = 5.5 V	
IL	Input LOW Current	Others			-0.4	mA	$V_{CC} = MAX, V$	/INI = 0.4 V	
1		S ₀ , S ₁			-0.8	mA	- VCC - WAX, VIIV - 0.4 V		
os	Short Circuit Current	Q ₀ , Q ₇	-20		-100	mA	$V_{CC} = MAX$		
	1/00-1/07		-30		-130	mA	$V_{CC} = MAX$		
lcc	Power Supply Current				53	mA	$V_{CC} = MAX$		

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	DADAMETED		LIMITS		LINUTC	CONDITIONS		
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS		
fMAX	Maximum Clock Frequency	25	35	100	MHz	1 22 1		
^t PHL ^t PLH	Propagation Delay, Clock to Q ₀ or Q ₇		26 22	39 33	ns	$C_L = 15 \text{ pF}$		
tPHL tPLH	Propagation Delay, Clock to I/O ₀ -I/O ₇		25 17	39 25	ns	$C_L = 45 \text{ pF},$		
^t PZH ^t PZL	Output Enable Time		14 20	21 30	ns	$R_L = 667 \Omega$		
^t PHZ ^t PLZ	Output Disable Time		10 10	15 15	ns	$C_L = 5.0 \text{ pF}$		

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

CVAADOL	PARAMETER		LIMITS		LINUTC	TECT COMPITIONS		
SYMBOL		MIN	TYP	MAX	UNITS	TEST CONDITIONS		
tw	Clock Pulse Width HIGH	30			ns			
tW	Clock Pulse Width LOW	10			ns			
:W	Clock Pulse Width LOW	20			ns			
s	Data Setup Time	20			ns	$V_{CC} = 5.0 \text{ V}$		
S	Select Setup Time	35			ns	ACC - 2:0 A		
h	Data Hold Time	0			ns			
h	Select Hold Time	10			ns			
rec	Recovery Time	20			ns			

DEFINITION OF TERMS:

SETUP TIME t_s is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME $\,$ th $\,$ is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME trec is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.



DESCRIPTION — 1The SN54LS/74LS348 and the SN54LS/74LS848 are eight input priority encoders which provide the 8-line to 3-line function.

The outputs (AO-A2) and inputs (O-7) are active low. The active low input which has the highest priority (input 7 has the highest) is represented on the outputs (output AO is the lowest bit). An example would be if inputs 1, 2 and 4 were low, then a binary 4 would be represented on the outputs.

The GS (Group Signal) output is active low when any of the inputs are low. It serves to indicate when any of the inputs are active.

A0, A1 and A2 are three-state outputs. This allows for up to 64 line expansion without the need for special external circuitry.

A logical one on the Enable Input (EI) forces AO, A1 and A2 to the disabled state and outputs GS and EO to the high state. A high on all data inputs (0–7) together with a low on the EI input disables outputs AO, A1, and A2 and forces output GS to the high state and output EO to the low state.

Use of the El input in conjunction with the EO output provides for the capability of having priority encoding of n input signals.

The LS848 has special internal circuitry providing for a greatly reduced negative going glitch on the GS (Group Signal) output and on a reduced tendency for the AO, A1 and A2 outputs to become momentarily enabled. Both of these occurrences happen when the El input goes from a logical one to a logical zero and all data inputs (O-7) are held at logical ones. The internal glitch reduction circuitry does add an additional fan-in of one on all data inputs (compared to that of the LS348).

FUNCTION TABLE

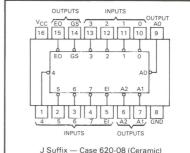
			11	NPL	JTS					ΟU	TPU	TS	
ΕI	0	1	2	3	4	5	6	7	A2	Α1	AO	GS	ΕO
Н	Х	Х	Х	X	Х	Х	X	Х	Z	Z	Z	Н	Н
L	Н	Н	Н	Н	Н	Н	Н	H	Z	Z	Z	Н	L
L	Х	X	Χ	Χ	Χ	Χ	Χ	L	L	L	L	L	Н
L	X	Χ	X	Χ	X	X	L	Н	L	L	Н	L	Н
L	X	Χ	Χ	Χ	Χ	L	Н	Н	L	Н	L	L	Н
L	X	Χ	X	Χ	L	Н	Н	Н	L	Н	Н	L	Н
L	X	Χ	Χ	L	Н	Н	Н	Н	Н	L	L	L	Н
L	X	Χ	L	Н	Н	Н	Н	Н	Н	L	Н	L	Н
L	X	L	Н	Н	Н	Н	Н	Н	Н	Н	L	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н

- H = high logic level
- L = low logic level
- X = irrelevant
- Z = high impedance state

SN54LS/74LS348 SN54LS/74LS848

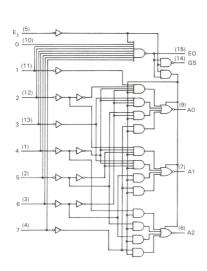
8-INPUT PRIORITY ENCODER

LOW POWER SCHOTTKY

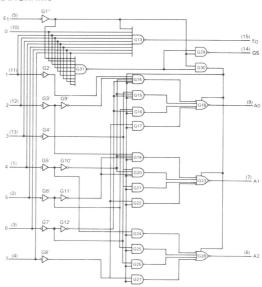


J Suffix — Case 620-08 (Ceramic N Suffix — Case 648-05 (Plastic)

BLOCK DIAGRAMS



SN54LS/74LS348



SN54LS/74LS848

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
VCC	Supply Voltage		54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range		54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High EO, GS		54,74			-0.4	mA
ГОН	Output Current — High A0, A1, A2 A0, A1, A2		54 74			-1.0 -2.6	mA
lOL	Output Current — Low EO, GS		54 74			4.0 8.0	mA
lor	Output Current — Low A0, A1, A2 A0, A1, A2	- 6 -	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST	CONDITIONS	
STIVIBUL	PARAIVIETER		MIN	TYP	MAX	UNITS	IEST	CONDITIONS	
√IH	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for	
		54			0.7	V		put LOW Voltage for	
VIL	Input LOW Voltage	74	9		0.8	V	All Inputs		
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = MIN$, $I_{IN} = -18 \text{ mA}$		
	Output HIGH Voltage AO, A1, A2	54,74	2.4	3.1		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} =$		
Vон	EO, GS	54	2.5	3.5		V	or V _{IL} per Trut		
	EO, GS	74	2.7	3.5		V			
	0	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$v_{CC} = v_{CC} min$,	
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
	Input HIGH Current Input 0, EI — LS348				20	μΑ			
	Input 0 — LS848			40	μΑ	$V_{CC} = MAX, V$	/INI = 2 7 V		
Iн	Other — LS348 Other — LS848				40 60	μA μA		·	
1111	Input 0, EI — LS348				0.1	mA			
	Input 0 — LS848				0.2	mA	$V_{CC} = MAX, V$	/INI = 7.0 V	
	Other — LS348 Other — LS848				0.2 0.3	mA mA		110	
	Input LOW Current Input 0, El — LS348				-0.4	mA			
liL	Input 0 — LS848				-0.8	mA	Vcc = MAX \	/INI = 0.4 \/	
-	Other — LS348 Other — LS848				-0.8 -1.2	mA mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$		
os	Short Circuit Current	EO, GS	-20		-120	mA	$V_{CC} = MAX$	1	
US	Short Girduit Guireilt	A0,A1,A2	-30		-130	mA	·CC — WAX		
СС	Power Supply Current Total, Output HIGH			12	23	mA	V _{CC} = MAX, All Inputs and	Outputs Open	
	Total, Output LOW			13	25		V _{CC} = MAX, II All Others Ope	nputs 7, E1 = GND	

AC CHARACTERISTICS:	$V_{CC} = 5.0 \text{ V}$ $T_A = 25^{\circ}\text{C}$

					LS348 LIMITS			LS848 LIMITS				
SYMBOL	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	TEST CONDITIONS	
^t PLH	1 thru 7	A0, A1, or A2	In-Phase		11	17		12	18	ns	$C_{I} = 45 pF$	
^t PHL		7.10,7.11,01.7.12	output		20	30		20	30			
^t PLH	1 thru 7	A0, A1, or A2	Out-of-Phase		23	35		23	35	ns	$R_L = 667 \Omega$	
^t PHL			output		23	35		23	35			
^t PZH	EI	A0, A1, or A2			25	39		25	39	ns		
^t PZL		7.0,711,01712			24	41		24	41	113		
^t PLH	0 thru 7	EO	Out-of-Phase		11	18		11	18	ns		
^t PHL			output		26	40		26	40	110		
^t PLH	0 thru 7	GS	In-Phase		38	55		38	55	ns	$C_{I} = 15 pF$	
^t PHL	o una /	00	output		9.0	21		9.0	21	110	OL TO PI	
tPLH	EI	GS	In-Phase		11	17		11	17	ns	$R_{I}=2.0 k\Omega$	
tPHL			output		14	36		14	36	110	11L 2.0 KI	
^t PLH	EI	EO	In-Phase		17	21		17	21	ns		
^t PHL			output		25	40		30	45	113		
^t PHZ	EI	A0, A1 or A2			18	27		18	27	ns	$C_{L} = 5.0 \text{ pF}$	
^t PLZ		,			23	35		23	35		$R_L = 667 \Omega$	



DESCRIPTION — The SN54LS/74LS352 is a very high-speed Dual 4-Input Multiplexer with Common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The SN54LS/74LS352 is the functional equivalent of the SN54LS/74LS153 except with inverted outputs.

- INVERTED VERSION OF THE SN54LS/74LS153
- SEPARATE ENABLES FOR EACH MULTIPLEXER
- INPUT CLAMP DIODE LIMIT HIGH SPEED TERMINATION **EFFECTS**

SN54LS352 SN74LS352

DUAL 4-INPUT MULTIPLEXER

LOW POWER SCHOTTKY

PIN NAMES

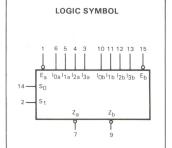
	HIGH	LOW
Common Select Inputs	0.5 U.L.	0.25 U.L.
Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Multiplexer Outputs (note b)	10 U.L.	5(2.5) U.L.
	Enable (Active LOW) Input Multiplexer Inputs	Common Select Inputs 0.5 U.L. Enable (Active LOW) Input 0.5 U.L. Multiplexer Inputs 0.5 U.L.

LOADING (Note a)

NOTES

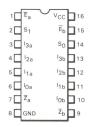
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM \overline{E}_a I_{Oa} 6 5 (4) (14) 10 (11) 12 (13) 15 3 2 V_{CC} = Pin 16 GND = Pin 8 = Pin Numbers



 $V_{CC} = Pin 16$ GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The SN54LS/74LS352 is a Dual 4-Input Multiplexer. It selects two bits of data from up to four sources under the control of the common Select Inputs (S₀, S₁). The two 4-input multiplexer circuits have individual active LOW Enables (\overline{E}_a , \overline{E}_b) which can be used to strobe the outputs independently. When the Enables (\overline{E}_a , \overline{E}_b) are HIGH, the corresponding outputs (\overline{Z}_a , \overline{Z}_b) are forced HIGH.

The logic equations for the outputs are shown below.

$$\begin{split} \overline{Z}_{a} &= \overline{E}_{a} \bullet (I_{\underline{O}a} \bullet \overline{S}_{1} \bullet \overline{S}_{0} + I_{1a} \bullet \overline{S}_{1} \bullet S_{0} + I_{2a} \bullet S_{1} \bullet \overline{S}_{0} + I_{3a} \bullet S_{1} \bullet S_{0}) \\ \overline{Z}_{b} &= \overline{E}_{b} \bullet (I_{\underline{O}b} \bullet \overline{S}_{1} \bullet \overline{S}_{0} + I_{1b} \bullet \overline{S}_{1} \bullet S_{0} + I_{2b} \bullet S_{1} \bullet \overline{S}_{0} + I_{3b} \bullet S_{1} \bullet S_{0}) \end{split}$$

The SN54LS/74LS352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The SN54LS/74LS352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT	INPUTS		INF	PUTS (a o	rb)		ОUТРUТ
s ₀	s ₁	E	10	11	12	13	Z
×	X	Н	X	X	×	Х	Н
L	L	L	L	X	×	×	н
L	L	L	н	×	×	×	L
Н	L	L	×	L	×	×	н
н	L	L	×	Н	X	×	L
L	н	L	×	×	L	×	н
L	н	L	×	×	Н	×	L
н	Н	L	X	×	×	L	н
Н	Н	L	×	×	×	Н	L

H = HIGH Voltage Level

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

L = LOW Voltage Level

X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMETER			LIMITS		LINUTC	TEST CONDITIONS		
SYMBOL	PARAMETER	1	MIN	TYP	MAX	UNITS	IEST	CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for	
		54			0.7			put LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Voltag	ge		-0.65	-1.5	V	$V_{CC} = MIN$, $I_{IN} = -18 \text{ mA}$		
		54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} =		
Vон	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Trut	h Table	
		54,74		0.25	0.4	V		$V_{CC} = V_{CC} MIN,$	
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	V _{CC} = MAX, V	/ _{IN} = 2.7 V	
lН	Input HIGH Current				0.1	mA	V _{CC} = MAX, V	/ _{IN} = 7.0 V	
IIL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V	/IN = 0.4 V	
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$		
lcc	Power Supply Current	Supply Current			10	mA	V _{CC} = MAX		

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

CVAADOL	DADAMETED		LIMITS		UNITS	CONDITIONS		
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS			
^t PLH ^t PHL	Propagation Delay, Select to Output		19 25	29 38	ns	Fig. 1 or 2		
^t PLH ^t PHL	Propagation Delay, Enable to Output		16 21	24 32	ns	Fig. 2	$V_{CC} = 5.0 V$ $C_{L} = 15 pF$	
tPLH tPHL	Propagation Delay, Data to Output		13 17	20 26	ns	Fig. 1		

AC WAVEFORMS

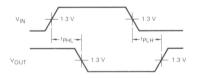


Fig. 1

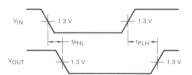


Fig. 2



DESCRIPTION — The LSTTL/MSI SN54LS/74LS353 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (E₀) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.

- INVERTED VERSION OF SN54LS/74LS253
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION **EFFECTS**

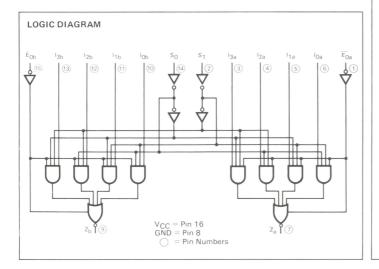
SN54LS353 SN74LS353

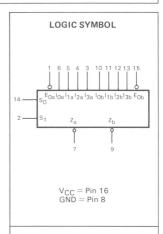
DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

PIN NAMES		LOADING	G (Note a)
		HIGH	LOW
S ₀ , S ₁	Common Select Inputs	0.5 U.L.	0.25 U.L.
Multiplexer A Ē _{Oa} I _{Oa} —I _{3a} Z̄ _a	Output Enable (Active LOW) Input Multiplexer Inputs Multiplexer Output (Note b)	0.5 U.L. 0.5 U.L. 65(25)U.L.	0.25 U.L. 0.25 U.L. 15(7.5) U.L.
Multiplexer B \bar{E}_{Ob} $ _{Ob}$ — $ _{3b}$ \bar{Z}_{b}	Output Enable (Active LOW) Input Multiplexer Inputs Multiplexer Output (Note b)	0.5 U.L. 0.5 U.L. 65(25)U.L.	0.25 U.L. 0.25 U.L. 15(7.5) U.L.

a 1 TTL Unit Load (U.L.) = $40~\mu$ A HiGH-/1 6 mA LOW. b. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HiGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges





CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix - Case 648-05 (Plastic)

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

 $\label{eq:FUNCTIONAL DESCRIPTION} The SN54LS/74LS353 contains two identical 4-input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (SQ, S1). The 4-input multiplexers have individual Output Enable (EQa, EQb) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.$

The logic equations for the outputs are shown below:

$$\begin{split} & \overline{Z_a} \!=\! \overline{\overline{E}_{0a} \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 \!+\! I_{1a} \bullet \overline{S}_1 \bullet S_0 \!+\! I_{2a} \bullet S_1 \bullet \overline{S}_0 \!+\! I_{3a} \bullet S_1 \bullet S_0)} \\ & \overline{Z_b} \!=\! \overline{\overline{E}_{0b} \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 \!+\! I_{1b} \bullet \overline{S}_1 \bullet S_0 \!+\! I_{2b} \bullet S_1 \bullet \overline{S}_0 \!+\! I_{3b} \bullet S_1 \bullet S_0)} \end{split}$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELI			DATA	INPUTS		OUTPUT ENABLE	ОИТРИТ
s ₀	s ₁	10	11	12	13	Ē ₀	z
X	×	Х	×	×	Х	н	(Z)
L	L	L	×	×	X	L	н
L	L	н	×	×	×	L	L
н	L	×	L	×	×	L	н
н	L	×	Н	×	×	L	L
L	Н	×	×	L	×	L	н
L	Н	×	×	Н	×	L	L
н	Н	×	×	×	L	L	н
Н	Н	X	X	X	н	L	L

H = HIGH Level

L = LOW Level

X = Immaterial

(Z) = High Impedance (off)

Address inputs S_0 and S_1 are common to both sections.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54 74			-1.0 -2.6	mA
loL	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	. PARAMETER		LIMITS			UNITS	TEST CONDITIONS		
STIVIBUL			MIN	TYP	MAX	UNITS	IEST	CONDITIONS	
VIH	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs			
	54				0.7		Guaranteed Input LOW Voltage for		
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$			
		54	2.4	3.4		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{II}$		
VOH	H Output HIGH Voltage		2.4	3.1		V	or V _{IL} per Trut	h Table	
VOL	Output LOW Voltage	54,74		0.25	0.4	V	I _{OL} = 12 mA	$V_{CC} = V_{CC} MIN,$	
	$Q_A - Q_H$	74		0.35	0.5	V	$I_{OL} = 24 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
lozh	Output Off Current HIGH			20	μΑ	V _{CC} = MAX, V _{OUT} = 2.7 V			
lozL	Output Off Current LOW			-20	μΑ	V _{CC} = MAX, V _{OUT} = 0.4 V			
					20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$		
lн	Input HIGH Current			0.1	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$			
IIL	Input LOW Current			-0.4	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$			
los	Short Circuit Current	-30		-130	mA	V _{CC} = MAX			
lcc	Power Supply Current Total, Output 3-State				14	- mA	V _{CC} = MAX		
'CC	Total, Output LOW			12	ACC - MAY				

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
^t PLH ^t PHL	Propagation Delay, Data to Output		11 13	25 20	ns	Fig. 1	
t _{PLH} t _{PHL}	Propagation Delay, Select to Output	×	20 21	45 32	ns	Fig. 1 or 2	$C_{\rm I} = 15 \rm pF$
^t PZH	Output Enable Time to HIGH Level		11	23	ns	Figs. 4, 5	5 - 10 p.
tPZL	Output Enable Time to LOW Level		15	23	ns	Figs. 3, 5	
^t PLZ	Output Disable Time from LOW Level		12	27	ns	Figs. 3, 5	$C_{I} = 5.0 pF$
^t PHZ	Output Disable Time from HIGH Level		27	41	ns	Figs. 4, 5	- C 0.0 p.

3 - STATE WAVEFORMS

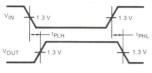
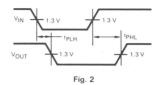


Fig. 1



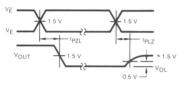


Fig. 3

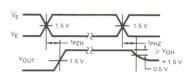
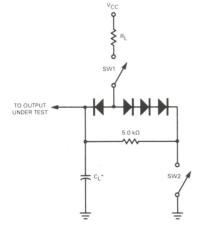


Fig. 4

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance.

Fig. 5

SWITCH POSITIONS

SYMBOL	SW1	SW2
tPZH	Open	Closed
tPZL	Closed	Open
tPLZ	Closed	Closed
tPHZ	Closed	Closed



DESCRIPTION — These devices are high speed hex buffers with 3-state outputs. They are organized as single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable (E) is LOW.

When the Output Enable (E) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

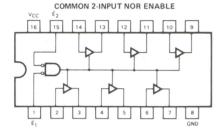
J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

SN54LS/74LS365A SN54LS/74LS366A SN54LS/74LS367A SN54LS/74LS368A

3-STATE HEX BUFFERS

LOW POWER SCHOTTKY

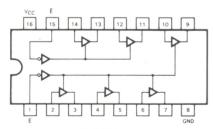
SN54LS/74LS365A HEX 3-STATE BUFFER WITH



TRUTH TABLE

11	NPUT	OUTDUT	
Ē ₁	Ē ₂	D	OUTPUT
L	L	L	L
L	L	Н	Н
Н	X	X	(Z)
X	Н	Х	(Z)

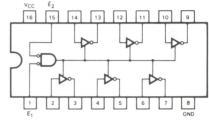
SN54LS/74LS367A HEX 3-STATE BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INP	UTS	OUTDUT
Ē	D	OUTPUT
L	L	L
L	Н	Н
Н	X	(Z)

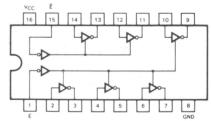
SN54LS/74LS366A HEX 3-STATE INVERTER BUFFER WITH COMMON 2-INPUT NOR ENABLE



TRUTH TABLE

11	NPUT	01170117			
Ē ₁	Ē₂	D	OUTPUT		
L	L	L	Н		
L	L	Н	L		
Н	X	X	(Z)		
X	Н	X	(Z)		

SN54LS/74LS368A HEX 3-STATE INVERTER BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INP	UTS	OUTPUT
Ē	D	OUTPUT
L	L	Н
L	Н	L
Н	Χ	(Z)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54 74			-1.0 -2.6	mA
loL	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMBOL	PARAMETER			LIMITS		UNITS	TEST COMPITIONS		
SYMBOL	PARAMETER		MIN TYP MAX		MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
	1 0 0 0 0 0	54			0.7	.,	Guaranteed Input LOW Voltage for		
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
		54	2.4	3.4		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH}$		
VOH	Output HIGH Voltage	74	2.4	3.1		V	or V _{IL} per Truth Table		
	0	54,74		0.25	0.4	V	$I_{OL} = 12 \text{ mA} V_{CC} = V_{CC} \text{ MIN},$		
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 24 mA V _{IN} = V _{IL} or V _{IH} per Truth Table		
OZH	Output Off Current HIGH				20	μΑ	$V_{CC} = MAX$, $V_{OUT} = 2.4 V$		
OZL	Output Off Current LOW				-20	μΑ	$V_{CC} = MAX$, $V_{OUT} = 0.4 V$		
Ін	Input HIGH Current				20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$		
'IH	Impat man canent				0.1	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$		
liL	Input LOW Current E Inputs				-0.4	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$		
	D Inputs				-20	μΑ	V _{CC} = MAX, V _{IN} = 0.5 V Either, E Input at 2 V		
					-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V Both E Inputs at 0.4 V		
los	Short Circuit Current		-40		-225	mA	$V_{CC} = MAX$		
	Power Supply Current LS365A, 367A				24	mA	V _{CC} = MAX		
cc	LS366A, 368A				21	IIIA	ACC — IAINY		

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0$ V

		LIMITS							
SYMBOL PARAMETER		LS365A/LS		367A LS3		LS366A/LS368A		UNITS	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
tPLH tPHL	Propagation Delay		10 9.0	16 22		7.0 12	15 18	ns	$C_L = 45 pF$,
^t PZH ^t PZL	Output Enable Time		19 24	35 40		18 28	35 45	ns	R _L = 667 Ω
^t PHZ ^t PLZ	Output Disable Time			30 35			32 35	ns	$C_L = 5.0 \text{ pF}$



DESCRIPTION — The SN54LS/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flipflops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedence state

The SN54LS/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54LS/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

- EIGHT LATCHES IN A SINGLE PACKAGE
- 3-STATE OUTPUTS FOR BUS INTERFACING
- HYSTERESIS ON LATCH ENABLE
- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED POSITIVE EDGE-TRIGGERED CLOCK
- HYSTERESIS ON CLOCK INPUT TO IMPROVE NOISE MARGIN
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION **EFFECTS**

PIN NAMES

		HIGH	LOW
D ₀ -D ₇	Data Inputs	0.5 U.L.	0.25 U.L.
LE	Latch Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
CP OE	Clock (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
OE	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
00-07	Outputs (Note b)	65(25)U.L.	15 (7.5) U.L.

1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

b. The Output LOW drive factor is 7.5 U.L. for Military and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

TRUTH TABLE

	LS373										
Dn	Dn LE ŌĒ										
Н	Н	L	Н								
L	Н	L	L								
X	X	Н	Z*								

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

7 = High Impedence

*Note: Contents of flip-flops unaffected by the state of the Output Enable input (OE)

SN54LS/74LS373 SN54LS/74LS374

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS:

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

LOW POWER SCHOTTKY

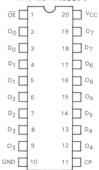
CONNECTION DIAGRAM DIP (TOP VIEW)

SN54LS/74LS373



CONNECTION DIAGRAM DIP (TOP VIEW)

SN54LS / 74LS374



J Suffix — Case 732-03 (Ceramic) N Suffix — Case 738-01 (Plastic)

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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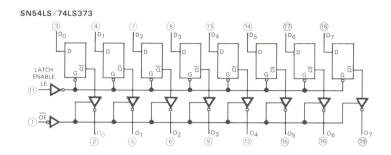
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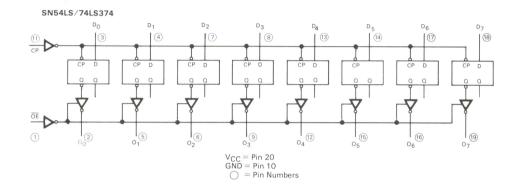
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LOADING (Note a)

LOGIC DIAGRAMS





GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54 74			-1.0 -2.6	mA
IOL	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS	
STIVIBUL			MIN	TYP	MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for
		54			0.7	.,		put LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltage	;		-0.65	-1.5	V	V _{CC} = MIN, I _I	N = -18 mA
		54	2.4	3.4		V		OH = MAX, VIN = VIH
VOH	Output HIGH Voltage	74	2.4	3.1		V	or V _{IL} per Trut	th Table
		54,74		0.25	0.4	V	I _{OL} = 12 mA V _{CC}	
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 24 mA	V _{IN} = V _{IL} or V _{IH} per Truth Table
lozh	Output Off Current HIGH				20	μΑ	V _{CC} = MAX,	V _{OUT} = 2.4 V
lozL	Output Off Current LOW				-20	μΑ	V _{CC} = MAX,	V _{OUT} = 0.4 V
					20	μΑ	V _{CC} = MAX, V	V _{IN} = 2.7 V
lΗ	Input HIGH Current				0.1	mA	V _{CC} = MAX, V	/ _{IN} = 7.0 V
IL	Input LOW Current				-0.4	mA	$V_{CC} = MAX, V_{IN} = 0.4 V$	
los	Short Circuit Current		-30		-130	mA	V _{CC} = MAX	
lcc	Power Supply Current				40	mA	V _{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

				LIM	ITS					
SYMBOL	PARAMETER	LS373		LS374			UNITS	TEST CONDITIONS		
		MIN	TYP	MAX	MIN	TYP	MAX			
fMAX	Maximum Clock Frequency				35	50		MHz		
^t PLH ^t PHL	Propagation Delay, Data to Output		12 12	18 18				ns	$C_L = 45 \text{ pF},$	
^t PLH ^t PHL	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	$R_L = 667 \Omega$	
^t PZH ^t PZL	Output Enable Time		15 25	28 36		20 21	28 28	ns		
^t PHZ ^t PLZ	Output Disable Time		12 15	20 25		12 15	20 25	ns	$C_L = 5.0 pF$	

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

			LIM			
SYMBOL	PARAMETER	LS373		LS374		UNITS
		MIN	MAX	MIN	MAX	
tw	Clock Pulse Width	15		15		ns
t _S	Setup Time	5.0		20		ns
th	Hold Time	20		0		ns

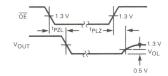
DEFINITION OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

LE The total output

Fig. 1

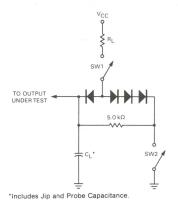


OE 1.3 V 2 1.3 V VOH

Fig. 2

Fig. 3

AC LOAD CIRCUIT

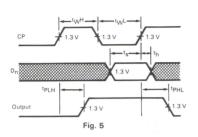


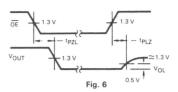
SWITCH POSITIONS

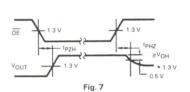
SYMBOL	SW1	SW2		
tpzH	Open	Closed		
tPZL	Closed	Open		
tpLZ	Closed	Closed		
tpHZ	Closed	Closed		

Fig. 4

AC WAVEFORMS

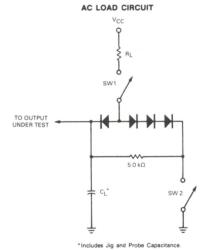






SWITCH POSITIONS

SYMBOL	SW1	SW2
[†] PZH	Open	Closed
†PZL	Closed	Open
tPLZ	Closed	Closed
^t PHZ	Closed	Closed





DESCRIPTION — The SN54LS/74LS375 is a 4-Bit D-Type Latch for use as temporary storage for binary information between processing limits and input/output or indicator units. When the Enable (E) is HIGH, information present at the D input will be transferred to the Q output and, if E is HIGH, the Q output will follow the input. When E goes LOW, the information present at the D input prior to its setup time will be retained at the Q outputs.

TRUTH TABLE (Each latch)

tn	t _{n+1}
D	Q
Н	Н
L	L

NOTES:

 $t_{\rm n}=$ bit time before enable negative-going transition $t_{\rm n+1}=$ bit time after enable negative-going transition

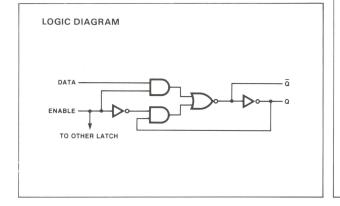
LOADING (Note a)

PIN NAMES

	HIGH	LOW
Data Inputs	0.5 U.L.	0.25 U.L.
Enable Input Latches 0, 1	2.0 U.L.	1.0 U.L.
Enable Input Latches 2, 3	2.0 U.L.	1.0 U.L.
Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.
Complimentary Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.
	Enable Input Latches 0, 1 Enable Input Latches 2, 3 Latch Outputs (Note b)	Data Inputs 0.5 U.L. Enable Input Latches 0, 1 2.0 U.L. Enable Input Latches 2, 3 2.0 U.L. Latch Outputs (Note b) 10 U.L.

NOTES:

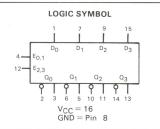
- a. 1 Unit Load (U.L.) = $40 \mu A HIGH/1.6 mA LOW$.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.



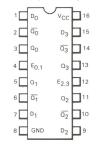
SN54LS375 SN74LS375

4-BIT D LATCH

LOW POWER SCHOTTKY



CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

NOTE

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

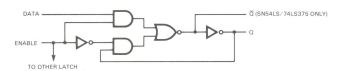
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DADAMASTED		LIMITS			UNITS	TEST CONDITIONS	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST	CONDITIONS
VIH	Input HIGH Voltage		2.0			V 7	Guaranteed Input HIGH Voltag	
		54			0.7	.,		put LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltage	je		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$	
		54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{OH}$ or V_{IL} per Truth Table	
VOH	Output HIGH Voltage	74	2.7	3.5		V		
		54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table
lн	Input HIGH Current	D Input E Input			20 80	μΑ	V _{CC} = MAX, V	7 _{IN} = 2.7 V
	mpat man dansin	D Input E Input			0.1 0.4	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
IIL	Input LOW Current	D Input E Input			-0.4 -1.6	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$	
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	x * *
lcc	Power Supply Current				12	mA	V _{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

			LIMITS			
SYMBOL PARAMETER	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
^t PLH ^t PHL	Propagation Delay, Data to Q		15 9.0	27 17	ns	
^t PLH ^t PHL	Propagation Delay, Data to $\overline{\mathbb{Q}}$		12 7.0	20 15	ns	V _{CC} = 5.0 V
^t PLH ^t PHL	Propagation Delay, Enable to Q		15 14	27 25	ns	C _L = 15 pF
tPLH tPHL	Propagation Delay, Enable to $\overline{\mathbb{Q}}$		16 7.0	30 15	ns	

LOGIC DIAGRAM



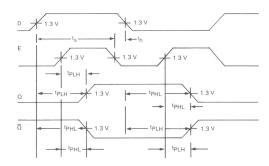
GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lor	Output Current — Low	54 74			4.0 8.0	mA

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	DADAMETER	LIMITS			UNITS	TEST CONDITIONS
	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
tw	Enable Pulse Width	20			ns	
t _S	Setup Time	20			ns	$V_{CC} = 5.0 V$
th	Hold Time	. 0			ns	

AC WAVEFORMS



DEFINITION OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

 $HOLD\ TIME\ (t_h) - is\ defined\ as\ the\ minimum\ time\ following\ the\ clock\ transition\ from\ LOW-to-HIGH\ that\ the\ logic\ level\ must\ be\ maintained\ at\ the\ input\ in\ order\ to\ ensure\ continued\ recognition.\ A\ negative\ HOLD\ TIME\ indicates\ that\ the\ correct\ logic\ level\ may\ be\ released\ prior\ to\ the\ clock\ transition\ from\ LOW-to-HIGH\ and\ still\ be\ recognized.$



DESCRIPTION — The SN54LS/74LS377 is an 8-bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

The SN54LS/74LS378 is a 6-Bit Register with a buffered common enable. This device is similar to the SN54LS/74LS174, but with common Enable rather than common Master Reset.

The SN54LS/74LS379 is a 4-Bit Register with buffered common Enable. This device is similar to the SN54LS/74LS175 but features the common Enable rather than common Master Reset.

- 8-BIT HIGH SPEED PARALLEL REGISTERS
- POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS
- FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS
- TRUE AND COMPLEMENT OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

SN54LS/74LS377 SN54LS/74LS378 SN54LS/74LS379

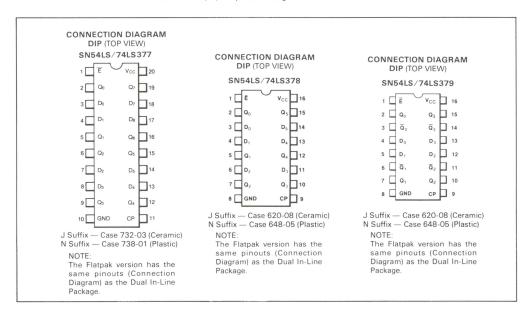
OCTAL D FLIP-FLOP WITH ENABLE; HEX D FLIP-FLOP WITH ENABLE; 4-BIT D FLIP-FLOP WITH ENABLE

LOW POWER SCHOTTKY

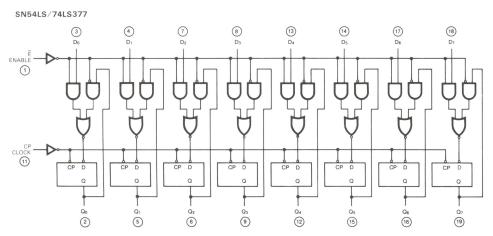
PIN NAMES		LOADING (Note a)		
		HIGH	LOW	
Ē	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.	
D_0-D_3	Data Inputs	0.5 U.L.	0.25 U.L.	
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.	
$\overline{\sigma}^0 - \overline{\sigma}^3$	True Outputs (Note b)	10 U.L.	5(2.5) U.L	
$\overline{Q}_0 - \overline{Q}_3$	Complemented Outputs (Note b)	10 U.L	5(2.5) U.L	

NOTES:

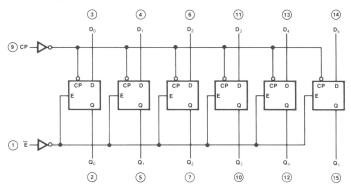
- a. 1 TTL Unit Load (U.L.) = $40 \mu A HIGH/1.6 mA LOW$
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

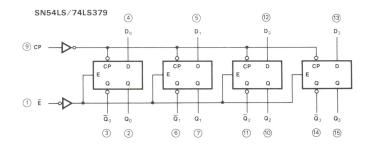


LOGIC DIAGRAMS



SN54LS/74LS378





GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMDOL	DARAMETER		LIMITS			UNITS	TEST CONDITIONS	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
\vee_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
		54			0.7	.,	Guaranteed Input LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltag	е		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$	
		54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH}	
VOH	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
	Output LOW Voltage	54,74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN},$	
VOL		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table	
					20	μΑ	$V_{CC} = MAX$, $V_{IN} = 2.7 V$	
lН	Input HIGH Current				0.1	mA	$V_{CC} = MAX$, $V_{IN} = 7.0 V$	
IIL	Input LOW Current				-0.4	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$	
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX	
lcc	Power Supply Current	LS377 LS378 LS379			28 22 15	mA	V _{CC} = MAX, NOTE 1	

Note: With all inputs open and GND applied to all data and enable inputs, I_{CC} is measured after a momentary GND, then $4.5\,\mathrm{V}$ is applied to clock.

AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST COMPITIONS	
		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
fMAX	Maximum Clock Frequency	30	40		MHz		
^t PLH ^t PHL	Propagation Delay, Clock to Output		17 18	27 27	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$	

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS
STIVIBUL	PA	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t₩	Any Pulse Wid	20			ns		
t _S	Data Setup Time		20			ns	
t_	Enable Setup Inactive — State		10			ns	$V_{CC} = 5.0 V$
t _S	Time	Active — State	25			ns	
th	Any Hold Time		5.0			ns	

DEFINITION OF TERMS:

 $SETUP\ TIME\ (t_S) -- is\ defined\ as\ the\ minimum\ time\ required\ for\ the\ correct\ logic\ level\ to\ be\ present\ at\ the\ logic\ input\ prior\ to\ the\ clock\ transition\ from\ LOW-to-HIGH\ in\ order\ to\ be\ recognized\ and\ transferred\ to\ the\ outputs.$

 $HOLD\,TIME\,(t_h)-is\,defined\,as\,the\,minimum\,time\,following\,the\,clock\,transition\,from\,LOW-to-HIGH\,that\,the\,logic\,level\,must\,be\,maintained\,at\,the\,input\,in\,order\,to\,ensure\,continued\,recognition.\,A\,negative\,HOLD\,TIME\,indicates\,that\,the\,correct\,logic\,level\,may\,be\,released\,prior\,to\,the\,clock\,transition\,from\,LOW-to-HIGH\,and\,still\,be\,recognized.$

TRUTH TABLE

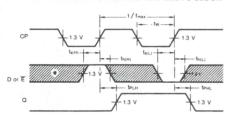
Ē	СР	D _n	Qn	\overline{Q}_n
н		×	No Change	No Change
L		Н	Н	L
L		L	L	Н

- L = LOW Voltage Level
- H = HIGH Voltage Level
- X = Immaterial

AC WAVEFORMS

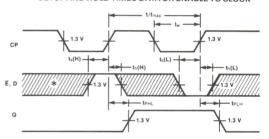
SN54LS/74LS377

CLOCK TO OUTPUT DELAYS CLOCK PULSE WIDTH, FREQUENCY, SETUP AND HOLD TIMES DATA OR ENABLE TO CLOCK



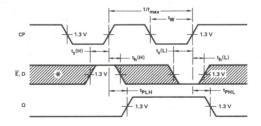
SN54LS/74LS378

CLOCK TO OUTPUT DELAYS CLOCK PULSE WIDTH, FREQUENCY, SETUP AND HOLD TIMES DATA OR ENABLE TO CLOCK



SN54LS/74LS379

CLOCK TO OUTPUT DELAYS CLOCK PULSE WIDTH, FREQUENCY, SETUP AND HOLD TIMES DATA, ENABLE TO CLOCK



^{*}The shaded areas indicate when the input is permitted to change for predictable output performance.



DESCRIPTION — The SN54LS/74LS385 is a general-purpose adder/subtractor which is useful as a companion part to the SN54LS/74LS384 two's-complement multiplier. The LS385 contains four independent adder/subtractor elements with common clock and clear.

Each of four independent sum (Σ) outputs reflects the respective A and B input and is controlled by the S/\overline{A} pin.

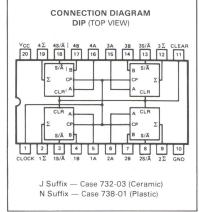
When low, the clear input asynchronously resets the sum flip-flop low and the carry flip-flop either high in the subtract mode or low in the add mode. The clock is positive-edge triggered and controls the sum and carry flip-flops.

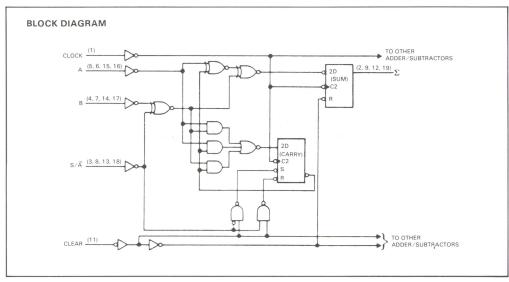
- FOUR SYNCHRONOUS ELEMENTS IN A SINGLE 20-PIN PACKAGE
- INDEPENDENT TWO'S-COMPLEMENT ADDITION/SUBTRACTION
- BUFFERED CLOCK AND DIRECT CLEAR INPUTS

SN54LS385 SN74LS385

QUADRUPLE SERIAL ADDERS/SUBTRACTORS

LOW POWER SCHOTTKY





FUNCTION TABLE

SELECTED		INP	UT	S		INTERNAL CA	RRY D INPUT	OUTPUT
FUNCTION	CLEAR	S/Ā	Α	В	СГОСК	BEFORE #	AFTER †	AFTER #
Clear	L	L	Х	X	Х	L	L	L
Clear	L	Н	X	Χ	X	Н	Н	L
	Н	L	L	L	4	L	L	L
	Н	L	L	L	*	Н	L	Н
	Н	L	L	Н	+	L	L L	Н
Add	Н	L	L	Н	+	Н	Н	L
	Н	L	Н	L		L	L	Н
	Н	L	Н	L	†	Н	Н	L
	Н	L	Н	Н	+	L	Н	L
	Н	L	Н	Н	†	Н	Н	Н
	Н	Н	L	L	+	L	L	Н
	Н	Н	L	L	+	Н	Н	L
	Н	Н	L	Н		L	L	L
Subtract	Н	Н	L	Н	†	Н	L	Н
	Н	Н	Н	L	†	L	Н	L
	Н	Н	Н	L	+	Н	Н	Н
	Н	Н	Н	Н	+	L	L	Н
	Н	Н	Н	Н	4	Н	Н	L

GUARANTEED OPERATING RANGES

00/111/1111						
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ЮН	Output Current — High	54,74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

H = high level, L = low level, X = irrelevant,

♦ = transition from low to high level at the clock input

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS	
SYMBOL	PARAMETER	PANAMETER			MAX	UNITS	TEST CONDITIONS	
VIH	Input HIGH Voltage		2.0	1.2		V	Guaranteed Input HIGH Voltage for All Inputs	
		54			0.7	.,		put LOW Voltage for
V _{IL}	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltag	e		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$	
		54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} =$	
Vон	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Trut	h Table
		54,74		0.25	0.4	V		$V_{CC} = V_{CC} MIN,$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	$V_{IN} = V_{IL}$ or V_{IH} per Truth Table
					20	μΑ	V _{CC} = MAX, V	$v_{1N} = 2.7 \text{ V}$
ΙΗ	Input HIGH Current				0.1	mA	V _{CC} = MAX, V	_{IN} = 7.0 V
IIL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V	'IN = 0.4 V
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
lcc	Power Supply Current				75	mA	V _{CC} = MAX	

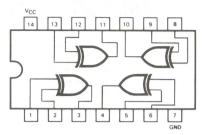
AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

CVMDOL	PARAMETER	LIMITS			UNITS	TECT COMPITIONS	
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
fMAX	Maximum Clock Frequency	30	40		MHz		
^t PLH ^t PHL	Propagation Delay, Clock to Σ		14 18	22 27	ns	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 15 \text{ pF}$	
^t PHL	Propagation Delay Clear to Σ		18	30	ns	CL — 19 pF	

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST COMPITIONS	
	PARAIVIETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t₩	Clock Pulse Width	16			ns		
t _S	Setup Time	10			ns	$V_{CC} = 5.0 \text{ V}$	
th	Hold Time	0			ns		





J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

SN54LS386 SN74LS386

QUAD 2-INPUT EXCLUSIVE-OR GATE

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CONDITIONS	
STIVIBUL	PARAIVIETER	FANAIVIETEN		TYP	MAX	UNITS		
V_{IH}	Input HIGH Voltage		2.0	9 =		V	Guaranteed In All Inputs	put HIGH Voltage for
		54			0.7		Guaranteed In	put LOW Voltage for
V_{IL}	Input LOW Voltage	74		0.8) V	V All Inputs		
VIK	Input Clamp Diode Voltag	je		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$	
		54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
VOH	Output HIGH Voltage	74	2.7	3.5	-	V		
		54,74		0.25	0.4	V		$V_{CC} = V_{CC}MIN$
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	VIN = VIL or VIH per Truth Table
					40	μΑ	V _{CC} = MAX, V	$v_{IN} = 2.7 \text{ V}$
lН	Input HIGH Current				0.2	mA	V _{CC} = MAX, V	_{IN} = 7.0 V
I _I L	Input LOW Current				-0.8	mA	V _{CC} = MAX, V	1N = 0.4 V
los	Short Circuit Current		-20		-100	mA	V _{CC} = MAX	
lcc	Power Supply Current				10	mA	V _{CC} = MAX	

AC CHARACTERISTICS: $T_A = 25$ °C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX	ONITS	TEST CONDITIONS	
^t PLH ^t PHL	Propagation Delay, Other Input LOW		12 10	23 17	ns	V _{CC} = 5.0 V	
^t PLH ^t PHL	Propagation Delay, Other Input HIGH		20 13	30 22	ns	$C_L = 15 pF$	



DESCRIPTION — The SN54LS/74LS390 and SN54LS/74LS393 each contain a pair of high-speed 4-stage ripple counters. Each half of the LS390 is partitioned into a divide-by-two section and a divide-by-five section, with a separate clock input for each section. The two sections can be connected to count in the 8.4.2.1 BCD code or they can count in a biquinary sequence to provide a square wave (50% duty cycle) at the final output.

Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In both the 'LS390 and the LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.

- DUAL VERSIONS OF LS290 AND LS293
- LS390 HAS SEPARATE CLOCKS ALLOWING $\div 2, \, \div 2.5, \, \div 5$
- INDIVIDUAL ASYNCHRONOUS CLEAR FOR EACH COUNTER
- TYPICAL MAX COUNT FREQUENCY OF 50 MHZ
- INPUT CLAMP DIODES MINIMIZE HIGH SPEED TERMINATION EFFECTS

PIN NA	MES	LOADING (Note a)			
		HIGH	LOW		
CP	Clock (Active LOW going edge)				
_	Input to +16 (LS393)	0.5 U.L.	. 1.0 U.L.		
CPO	Clock (Active LOW going edge)				
	Input to ÷2 (LS390)	0.5 U.L.	1.0 U.L.		
CP ₁	Clock (Active LOW going edge)				
	Input to ÷5 (LS390)	0.5 U.L.	1.5 U.L.		
MR	Master Reset (Active HIGH) Input	0.5 U.L.	0.25 U.L.		
00 - 03	Flip-Flop outputs (Note b)	10 U.L.	5(2.5) U.L.		

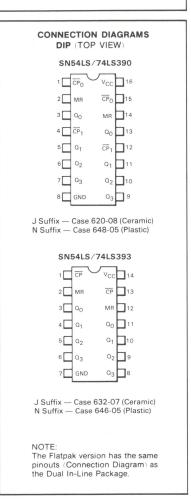
NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54LS/74LS390 SN54LS/74LS393

DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER

LOW POWER SCHOTTKY

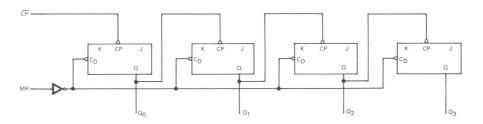


FUNCTIONAL DESCRIPTION—Each half of the SN54LS/74LS393 Operates in the Modulo16 binary sequence, as indicated in the \div 16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

Each half of the 'LS390 contains a $\div 5$ section that is independent except for the common MR function. The $\div 5$ section operates in 4.2.1 binary sequence, as shown in the $\div 5$ Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a $\div 10$ function having a 50% duty cycle output, connect the input signal to \overline{CP}_1 and connect the Q3 output to the \overline{CP}_0 input; the Q0 output provides the desired 50% duty cycle output. If the input frequency is connected to \overline{CP}_0 and the Q0 output is connected to \overline{CP}_1 , a decade divider operating in the 8.4.2.1 BCD code is obtained, as shown in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signals derived from combinations of 'LS390 outputs are also subject to decoding spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.

SN54LS/74LS390 LOGIC DIAGRAM (one half shown)

SN54LS/74LS393 LOGIC DIAGRAM (one half shown)



 $\begin{array}{c} \text{SN54LS/74LS390 BCD} \\ \text{TRUT\underline{H}} \text{TABLE} \\ \text{(Input on \overline{CP}_0; Q_0 \overline{CP}_1)} \end{array}$

	1.0	0.						
	OUNT 03 02 01 00							
	α ₀	02	03	COUNT				
-	L	L	L	0				
	Н	L	L	1				
	L	L	L	2				
	Н	L	L	3				
	L	н	L	4				
	Н	Н	L	5				
	L	Н	L	6				
	Н	Н	L	7				
	L	L	Н	8				
	Н	L	Н	9				
HLHLHL	-	L H H	LLLH	3 4 5 6 7 8				

SN54LS/74LS390 ÷ 5 TRUTH TABLE (Input on CP₁)

COUNT	Ol			
COUNT	03	02	01	
0	L	L	, L	-
1	L	L	Н	
2	L	Н	L	
3	L	Н	Н	
4	Н	L	L	_

SN54LS/74LS393 TRUTH TABLE

COUNT		OUT	PUTS		
COUNT	03	02	01	σ_0	
0	L	L	L	L	-
1	L	L	L	Н	
2	L	L	Н	L	
3	L	L	Н	Н	
4	L	Н	L	F.	
5	L	Н	L	Н	- "
6	L	,н	Н	L	
7	L	Н	Н	Н	-
8	Н	L	L	L	
9	Н	L	L	Н	
10	Н	L	Н	L	
11	Н	L	Н	Н	
12	Н	Н	L	L	
13	Н	Н	L	Н	
14	Н	Н	Н	L	
15	Н	Н	Н	н	_

H = HIGH Voltage Level L = LOW Voltage Level

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74			-0.4	mA
loL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST	CONDITIONS	
STIVIBUL	PARAIVIETER		MIN	TYP	MAX	UNITS	IEST	CONDITIONS	
VIH	Input HIGH Voltage		2.0	*		V	Guaranteed Input HIGH Voltage fo All Inputs		
		54			0.7		Guaranteed In	put LOW Voltage for	
VIL	Input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
		54	2.5	3.5		V	$V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{II}$ or V_{IL} per Truth Table		
Vон	Output HIGH Voltage	74	2.7	3.5		V			
		54,74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN,		
VOL	Output LOW Voltage	74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	V _{IN} = V _{IL} or V _{IH} per Truth Table	
					20	μΑ	V _{CC} = MAX, V	/ _{IN} = 2.7 V	
IH	Input HIGH Current				0.1	mA	V _{CC} = MAX, V	/ _{IN} = 7.0 V	
		MR			-0.4	mA			
lii.	Input LOW Current	CP, CPO			-1.6	mA	$V_{CC} = MAX, V$	$V_{CC} = MAX$, $V_{IN} = 0.4 V$	
'IL	input corr outlett	CP ₁			-2.4	mA	1		
os	Short Circuit Current		-20		-100	mA	V _{CC} = MAX		
lcc	Power Supply Current				26	mA	V _{CC} = MAX		

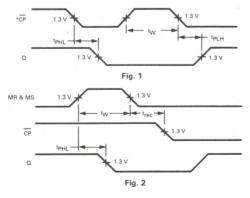
AC CHARACTERISTICS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

SYMBOL	DADAM	PARAMETER		LIMITS		LINUTC	TECT CONDITIONS
STIMBOL	PARAM	EIER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
fMAX	Maximum Clock Free CP ₀ to Q ₀	quency	25	35		MHz	
fMAX	Maximum Clock Free	quency	12.5	20		MHz	
tPLH tPHL	Propagation Delay, CP to Q ₀	LS393		12 13	20 20	ns	al al
tPLH tPHL	\overline{CP}_0 to Ω ₀	LS390		12 13	20 20	ns	
tPLH tPHL	CP to Q3	LS393		40 40	60 60	ns	$C_L = 15 \text{ pF}$
^t PLH ^t PHL	$\overline{\text{CP}}_0$ to Ω_2	LS390		37 39	60 60	ns	
^t PLH ^t PHL	\overline{CP}_1 to Q1	LS390		13 14	21 21	ns	
^t PLH ^t PHL	$\overline{\text{CP}}_1$ to Ω_2	LS390		24 26	39 39	ns	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
^t PLH ^t PHL	CP ₁ to Q ₃	LS390		13 14	21 21	ns	
^t PHL	MR to Any Input	LS390/393		24	39	ns	

AC SETUP REQUIREMENTS: $T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$

0)/44001	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
SYMBOL	PARAME	IEK	MIN	TYP	MAX	UNITS	TEST CONDITIONS
tw	Clock Pulse Width	LS393	20			ns	
tw	CP _O Pulse Width	LS390	20			ns	
tw	CP ₁ Pulse Width	LS390	40			ns	$V_{CC} = 5.0 V$
tw	MR Pulse Width	LS390/393	20			ns	
trec	Recovery Time	LS390/393	25			ns	

AC WAVEFORMS



^{*}The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Table.



DESCRIPTION — The SN54LS/74LS395 is a 4-Bit Register with 3-state outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset (MR) input overrides the synchronous operations and clears the register. An active HIGH Output Enable (OE) input controls the 3-state output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

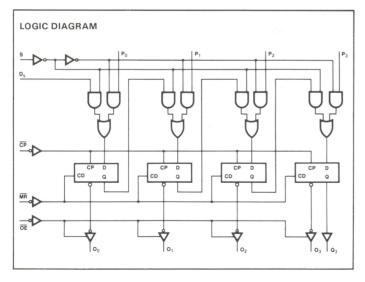
- SHIFT LEFT OR PARALLEL 4-BIT REGISTER
- 3-STATE OUTPUTS

• INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION **EFFECTS**

PIN NAN	MES	LOADING	(Note a)
		HIGH	LOW
Po-P3	Parallel Inputs	0.5 U.L.	0.25 U.L.
DS	Serial Data Input	0.5 U.L.	0.25 U.L.
D _S S CP	Mode Select Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active LOW) Input	0.5 U.L.	0.25 U.L.
MR OE	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
OE	Output Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
00-03	3-State Register Outputs	65(25) U.L.	15(7.5) U.L.
Q3	Register Output	10 U.L.	5 (2.5) U.L.

NOTES

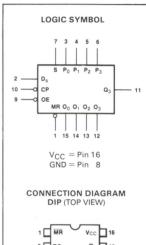
- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.



SN54LS395 SN741S395

4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY





J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

NOTE:

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The SN54LS/74LS395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel (Pn) input or from the preceding stage. When the Select input is HIGH, the Pn inputs are enabled. A LOW signal on the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse (CP) input. Signals on the P_{n} , D_{S} and S inputs can change when the Clock is in either state, provided that the recommended set-up and hold times are observed. When the S input is LOW, a CP HIGH-LOW transition transfers data in Q_{0} to Q_{1} , Q_{1} to Q_{2} , and Q_{2} to Q_{3} . A left-shift is accomplished by connecting the outputs back to the P_{n} inputs, but offset one place to the left, i.e., Q_{3} to P_{2} , Q_{2} to P_{1} and P_{2} , with P_{3} acting as the linking input from another package.

When the $\overline{\text{OE}}$ input is HIGH, the output buffers are disabled and the Q_0 — Q_3 outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54,74		c	-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TECT	CONDITIONS
STIVIBUL	PANAIVIETER		MIN	TYP	MAX	UNITS	IEST	CONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed In All Inputs	put HIGH Voltage for
· /		54			0.7	V		put LOW Voltage for
VIL	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltag	je		-0.65	-1.5	V	V _{CC} = MIN, III	N = −18 mA
		54	2.5	3.5		V	V _{CC} = MIN, I _C	$_{\text{DH}} = \text{MAX}, V_{\text{IN}} = V_{\text{I}}$
VOH	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Truth Table	
		54,74		0.25	0.4	V		V _{CC} = V _{CC} MIN,
VOL	Output LOW Voltage	. 74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table	V _{IN} = V _{IL} or V _{IH} per Truth Table
lozh	Output Off Current HIGH				20	μΑ	V _{CC} = MAX, \	1 ₀ = 2.4 V
lozL	Output Off Current LOW				-20	μΑ	V _{CC} = MAX, \	₀ = 0.4 V
					20	μΑ	V _{CC} = MAX, \	/ _{IN} = 2.7 V
lΗ	Input HIGH Current				-0.1	mA	V _{CC} = MAX, \	$I_{IN} = 7.0 \text{ V}$
IIL	Input LOW Current				-0.4	mA	V _{CC} = MAX, \	/IN = 0.4 V
los	Short Circuit Current		-20		-100	mA	$V_{CC} = MAX$	
lcc	Power Supply Current Total, Output HIGH				31	mA	V _{CC} = MAX, 0	$\overline{DE} = GND, \overline{CP} = GND$
	Total, Output LOW				34	mA	V _{CC} = MAX, 0 momentary 3.0	

AC CHARACTERISTICS: TA = 25°C

SYMBOL	PARAMETER		LIMITS			TEST COMPITIONS
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
fMAX	Maximum Input Clock Frequency	30	45		MHz	
^t PHL	Propagation Delay, Clear to Output		22	35	ns	
^t PLH ^t PHL	Propagation Delay, Low to High Propagation Delay, High to Low		15 25	30 30	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
[†] PZH [†] PZL	Output Enable Time		15 17	25 25	ns	1
^t PLZ ^t PHZ	Output Disable Time		12 11	20 17	ns	$C_L = 5.0 \text{ pF}$

AC SETUP REQUIREMENTS: $T_A = 25$ °C

CVAADOL	PARAMETER	LIMITS			UNITS	TECT COMPITIONS			
SYMBOL PARAMET		MIN	TYP	MAX	UNITS	TEST CONDITIONS			
tw	Clock Pulse Width	16			ns				
t _S	Setup Time, Mode Select	40			ns	3.24 3.24 1.54 1.54 1.55 1.55 1.55 1.55 1.55 1.5			
t _S	Setup Time, All Others	20			ns	V _{CC} = 5.0 V			
th	Data Hold Time	10			ns				

MODE SELECT — TRUTH TABLE

Operation Made		Inputs @ t _n					Outputs @ t _{n+1}					
Operating Mode	MR	CP	S	Ds	Pn	00	01	02	03			
Asynchronous Reset Shift, SET First Stage	L H	×	X L	X	X	L H	L O _{0n}	L O _{1n}	L O _{2n}			
Shift, RESET First Stage Parallel Load	H	~	L H	L X	X P _n	P ₀	O _{0n} P ₁	O _{1n} P ₂	O _{2n}			

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

 $NOTE: \\ When \ \overline{OE} \ is \ HIGH, outputs \ O_0-O_3 \ are \ in the \ high \ impedance \ state; however, this does not affect other operations or the \ O_3 \ output.$

 $[\]mathsf{t}_{n,\ n+1} = \mathsf{time}$ before and after CP HIGH-to-LOW transition

TYPES SN54ALS160 THRU SN54ALS163 SN74ALS160 THRU SN74ALS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}
Input voltage
Operating free-air temperature range: SN54ALS160 thru SN54ALS163
SN74ALS160 thru SN74ALS163
Storage temperature range – 65 °C to 150 °C

recommended operating conditions

				SN	THRU	60	SN	174ALS1 THRU	160	UNIT
				SN	154ALS	63	SN	174ALS1	163	Oleil
				MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input vol	tage		2			2			V
V_{IL}	Low-level input vol	tage				0.8			0.8	V
Іон	High-level output v	oltage				-0.4			-0.4	mA
loL	Low-level output co	urrent				4			8	mA
4	Clock frequency	'ALS160, 'ALS1	62	0		30	0		30	МН
fclock	Clock frequency	'ALS161, 'ALS1	63	0		30	0		30	IVIH
		CLK High		18			15			
t_{w}	Pulse duration	CLK Low		15			15			ns
		'ALS160, 'ALS1	61 CLR low	18			16			1
		A, B, C, D		15			15			
		END ENT	'ALS160, 'ALS161	20			20			1
	Setup time	ENP, ENT	'ALS162, 'ALS163	20			20			1
tsu	before CLK†	'ALS160, 'ALS1	61 CLR inactive	15			15			ns
		'ALS162, 'ALS1	CLR Low	25			25			1
		ALSTOZ, ALST	CLR high (inactive)	15			15			1
th	Hold time, all synch	nronous inputs afte	r CLK†	0			0			ns
ТА	Operating free-air to	emperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P	PARAMETER	TEST CONDITIONS			54ALS1 THRU 54ALS1		SN74ALS160 THRU SN74ALS163			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
VIK		$V_{CC} = 4.5 V$,	$I_{\parallel} = -18 \text{ rnA}$			- 1.5			- 1.5	V
Voн			$I_{OH} = -0.4 \text{ mA}$	V _{CC}	-2	- ×				V
VOH			$I_{OH} = -0.4 \text{ mA}$				VCC	-2		
1/		$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
VOL		V _{CC} = 4.5 V,	I _{OL} = 8 mA					0.35	0.5	ľ
l _l	LOAD, CLK or ENT	V _C C = 5.5 V,	V ₁ = 7 V			0.2			0.2	mA
"I	All other	vCC = 5.5 v,	V - 7 V			0.1			0.1.	l ''''
lux	LOAD, CLK or ENT	$V_{CC} = 5.5 V$,	V1 - 0 4 V	-		40			40	μА
IH	All other	vCC = 5.5 v,	V = 0.4 V			20			20	μΑ.
IIL		$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.2			-0.2	mA
10*		$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	-30		-112	-30		-112	mA
ICCL		$V_{CC} = 5.5 V$				16			16	mA
I _{ССН}		V _{CC} = 5.5 V				15.5			15.5	mA

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_{A} = 25 \, ^{\circ}\text{C}.$

 $^{^*}$ The current produced by grounding the outputs is approximately twice that produced with 2.25 V on the outputs.

TYPES SN54ALS160 AND SN54ALS162 SN74ALS160 AND SN74ALS162 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

'ALS160 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = \text{MIN to MAX}$ $0.5054 \text{ ALS} 160$ $0.5054 \text{ ALS} 161$ $0.5054 \text{ ALS} 161$				
			MIN	MAX	MIN	MAX		
4	'Al	S160	30		30		MHz	
fmax	'ALS	S161	30		30	30		
tPLH	CLK	RCO	8	25	8	23		
^t PHL	CLK		7	20	7	20	ns	
^t PLH	CLK	Any Q	4	22	4	22	ns	
^t PHL	CLK	Ally C	6	28	6	28	ns	
^t PLH	ENT	RCO	5	20	5	20	ns	
[†] PHL	ENT	NCO NCO	4	16	4	16	ns	
[†] PHL	CLR	Any Q	8	28	8	28	ns	
^t PHL	CLR	RCO	11	35	11	30	ns	

'ALS162 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = \text{MIN to MAX}$ $SN54ALS162 \qquad SN74ALS162$ $SN54ALS163 \qquad SN74ALS163$				
	x		MIN	MAX	MIN	MAX	
	'AL	S162	30		30		MHz
fmax	'AL	30		30		IVITIZ	
^t PLH	CLK	RCO	8	25	8	23	ns
^t PHL	CLK	hCO	7	20	7	20	ns
^t PLH	CLK	Any Q	4	22	4	22	ns
[†] PHL	CLK	Any Q	6	28	6	28	ns
^t PLH	ENT	RCO	5	20	5	20	
^t PHL	EINT	NCO ,	4	16	4	16	ns

See next page for 161 and 163.

TYPES SN54ALS161 AND SN54ALS163 SN74ALS161 AND SN74ALS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

'ALS161 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)		C _L = 50 pl R _L = 500 s T _A = MIN SN54ALS160 SN54ALS161		SN54ALS161 SN74ALS161		UNIT
			MIN	MAX	MIN	MAX		
f	'AL	S160	30		30		MHz	
fmax	'AL	S161	30		30		IVITIZ	
t _{PLH}	CLK	RCO	. 8	25	8	23	ns	
t _{PHL}	CLK		7	20	7	20	1115	
^t PLH	CLK	Any Q	4	22	4	22	ns	
^t PHL	CLK	Ally G	6	26	6	26	115	
^t PLH	ENT	RCO	5	20	5	20	ns	
^t PHL	LIVI	1100	4	16	4	16	1 115	
tPHL	CLR	Any Q	8	28	8	28	ns	
tPHL	CLR	RCO	11	31	11	28	ns	

'ALS163 switching characteristics

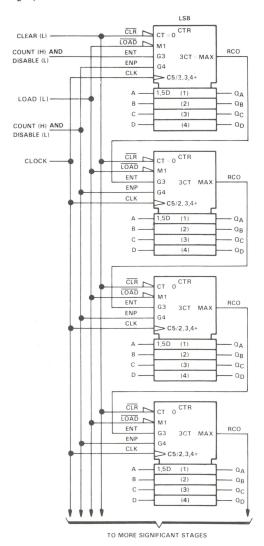
PARAMETER	FROM (INPUT)	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		C _L = 50 pF R _L = 500 S T _A = MIN 1 SN54ALS162		ALS162	UNIT
,	'AL	S162	30		30		
fmax	'AL	S163	30		30		MHz
^t PLH	CLK	RCO	8	25	8	23	ns
^t PHL	CLK	NCO .	7	20	7	20	115
^t PLH	CLK	Any Q	4	22	4	22	ns
[†] PHL	CLK	Ally d	6	28	6	28	115
[†] PLH	ENT	RCO	5	20	5	20	ns
^t PHL	LIVI	1100	4	16	4	16] ''s

TYPES SN54ALS160 THRU SN54ALS163 SN74ALS160 THRU SN74ALS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'ALS160 and 'ALS162 will count in BCD and the 'ALS161 and 'ALS163 will count in binary. Virtually any count mode (modulo-N, N₁-to-N₂, N₁-to-maximum) can be used with this fast look-ahead circuit.





TYPES SN54ALS190, SN54ALS191, SN74ALS190, SN74ALS191 SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

- Single Down/Up Count Control Line
- Look-Ahead Circuitry Enhances Speed of Cascaded Counters
- Fully Synchronous in Count Modes
- Asynchronously Presettable with Load Control

	(TO	P VIEW)	
В	\Box 1	U ₁₆	VCC
Q_B	2	15	Α
Q_A	3	14	CLK
CTEN	4	13	RCO
D/\overline{U}	□ 5	12	MAX/MIN
QC	6	11 🗍	LOAD
QD	7	10	C
GND	[8	9	D

descriptions

The 'ALS190 and 'ALS191 are synchronous, reversible up/down counters. The 'ALS190 is a 4-bit decade counter and the 'ALS191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input (\overline{CTEN}) is low. A high at \overline{CTEN} inhibits counting. The direction of the count is determined by the level of the down/up (D/\overline{U}) input. When D/\overline{U} is low, the counter counts up and when D/\overline{U} is high, it counts down.

J Suffix—Case 620-08 (Ceramic) N Suffix—Case 648-05 (Plastic)

These counters feature a fully independent clock circuit. Changes at the control inputs $(\overline{\text{CTEN}})$ and D/\overline{U} that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The CLK, D/\overline{U} , and LOAD inputs are buffered to lower the drive requirement, which significantly reduces the loading on, or current required by, clock drivers, etc., for long parallel words.

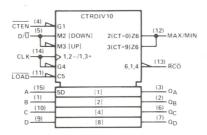
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The SN54ALS190 and SN54ALS191 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74ALS190 and SN74ALS191 are characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

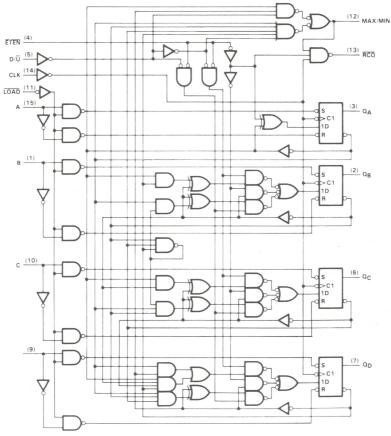
Portions of this data sheet are reprinted with permission from the Texas Instruments 1983 ALS/AS Logic Circuits Data Book.

TYPES SN54ALS190, SN74ALS190 SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS

'ALS190 logic symbol



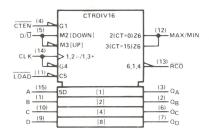
'ALS190 logic diagram (positive logic)



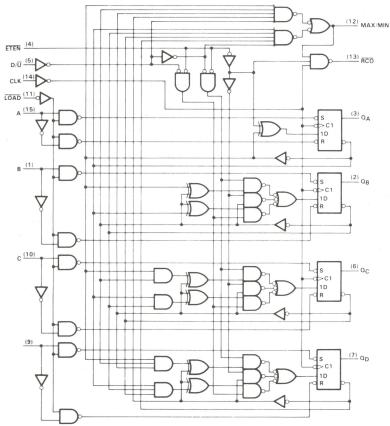
Pin numbers shown are for J and N packages.

TYPES SN54ALS191, SN74ALS191 SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

'ALS191 logic symbol



'ALS191 logic diagram (positive logic)



Pin numbers shown are for J and N packages.

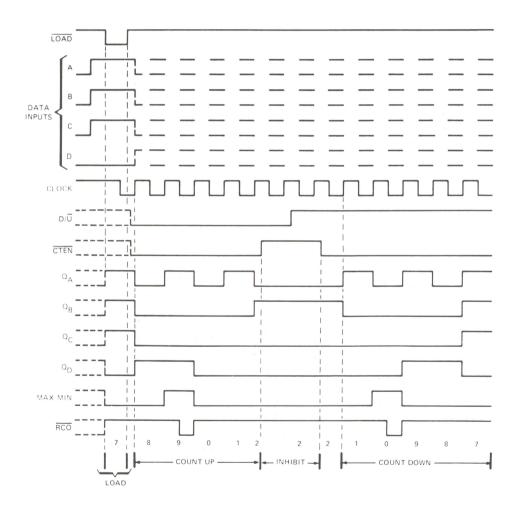
TYPES SN54ALS190, SN74ALS190 SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS

typical load, count, and inhibit sequences

'ALS190

Illustrated below is the following sequence:

- 1. Load (preset) to BCD seven.
- 2. Count up to eight, nine (maximum), zero, one, and two.
- 3. Inhibit.
- 4. Count down to one, zero (minimum), nine, eight, and seven.



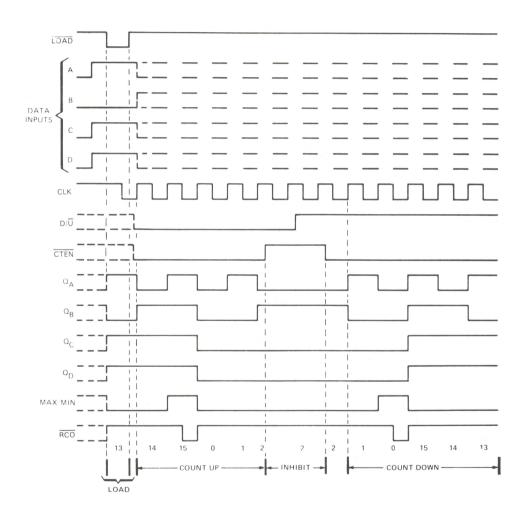
TYPES SN54ALS191, SN74ALS191 SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

typical load, count, and inhibit sequences

'ALS191

Illustrated below is the following sequence:

- 1. Load (preset) to binary thirteen.
- 2. Count up to fourteen, fifteen (maximum), zero, one, and two.
- 3. Inhibit.
- 4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



TYPES SN54ALS190, SN54ALS191, SN74ALS190, SN74ALS191 SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		
Input voltage		
Operating free-air temperature range:	SN54ALS190, SN54ALS191	
	SN74ALS190, SN74ALS191	
Storage temperature range		- 65 °C to 150 °C

recommended operating conditions

			-	54ALS1			74ALS1		UNI.
			MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input volt	age	2			2			V
VIL	Low-level input volta			0.8			0.8	V	
ГОН	High-level output cu	rrent			-0.4			-0.4	mA
la.	Low-level output cu	rent .			4				m.A
IOL	Low-level output cu	rrent						8	1117
4	Clock frequency	'ALS190	0		25	0		25	МН
fclock	Clock frequency	'ALS191	0		25	0		25	IVII
		CLK high	20			20			
tw	Pulse duration	CLK low	20			20			ns
		LOAD low	25			25			
		Data before LOAD†	20			20			
	C	CTEN before CLK†	20			20			
t _{su}	Setup time	D/U before CLK†	20	~		20	•		ns
		LOAD inactive before CLK†	20			20			
-		Data after LOAD†	0			0			
^t h	Hold time	CTEN after CLK†	0			0			ns
		D/Ū after CLK↑	0			0			
Тд	Operating free-air te	mperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

					54ALS			74ALS1		UNIT
ΡΔΙ	RAMETER	TEST CONDITIONS		SN	SN54ALS191			SN74ALS191		
1.0	AMETER			MIN	TYP:	MAX	MIN	TYP:	MAX	
V_{IK}		$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.5			- 1.5	V
Voн			$I_{OH} = -0.4 \text{ mA}$	VCC	-2					V
νОН			$I_{OH} = -0.4 \text{ mA}$				V _{CC}	-2		
VOL		$V_{CC} = 4.5 V$,	IOL = 4 mA		0.25	0.4		0.25	0.4	V
V () L		V _{CC} = 4.5 V,	IOL = 8 mA					0.35	0.5]
I.	CTEN	$V_{CC} = 5.5 V$	V _I = 7 V			0.1			0.1	^
li .	All others	VCC = 5.5 V,	V = 7 V			0.1			0.1	mA
Local	CTEN	\/ E E \/	V 27V			20			20	
ΊΗ	All others	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
L.,	CTEN	\/ E E \/	V - 0 4 V			-0.2			-0.2	
IIL	All others	$V_{CC} = 5.5 V,$	V _I = 0.4 V			- 0.1			- 0.1	mA
10*		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	-30		-112	mA
ICC		V _{CC} = 5.5 V,	All inputs at 0 V			17.5			17.5	mA

[‡]All typical values are at V_{CC} = 5 V, T_A = 25 °C. *The current produced by grounding the outputs is approximately twice that produced with 2.25 V on the outputs.

TYPES SN54ALS190, SN54ALS191, SN74ALS190, SN74ALS191 SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54ALS190 SN54ALS191		SN74ALS190 SN74ALS191		
			fmax	'ALS190		25	
'ALS191		25			25		
^t PLH	LOAD	Any Q	8	45	8	45	ns
^t PHL			8	35	8	35	
^t PLH	A, B, C, D	Any Q	4	28	4	26	ns
tPHL			4	37	4	35	
^t PLH	CLK	RCO	5	17	5	16	ns
^t PHL			5	15	5	14	
^t PLH	CLK	Any Q	3	25	3	25	ns
[†] PHL			3	28	3	28	
^t PLH	CLK	MAX/MIN	8	35	. 8	35	ns
^t PHL	OEK .	MICANIANIA	8	25	8	20	115
^t PLH	D/Ū	RCO	15	44	15	40	ns
t _{PHL}	5,0		10	34	10	32	
^t PLH	D/Ū	MAX/MIN	8	28	8	26	ns
^t PHL			8	28	8	26	
^t PLH	CTEN	RCO	4	17	4	17	ns
^t PHL			4	16	4	16	



TYPES SN54ALS192, SN54ALS193, SN74ALS192, SN74ALS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

- Look-Ahead Circuitry Enhances Cascaded Counters
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear

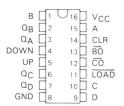
description

The 'ALS192 and 'ALS193 are synchronous, reversible up/down counters. The 'ALS192 is a 4-bit decade counter and the 'ALS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

(TOP VIEW)



J Suffix—Case 620-08 (Ceramic) N Suffix—Case 648-05 (Plastic)

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs. The clock, count, and load inputs are buffered to lower the drive requirements. This significantly reduces the loading on clock drivers, etc., for long parallel words.

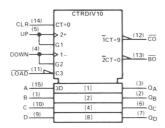
These counters were designed to be cascaded without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output (\overline{CO}) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN54ALS192 and SN54ALS193 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $\,^{\circ}\text{C}$. The SN74ALS192 and SN74ALS193 are characterized for operation from 0 $\,^{\circ}\text{C}$ to 70 $\,^{\circ}\text{C}$.

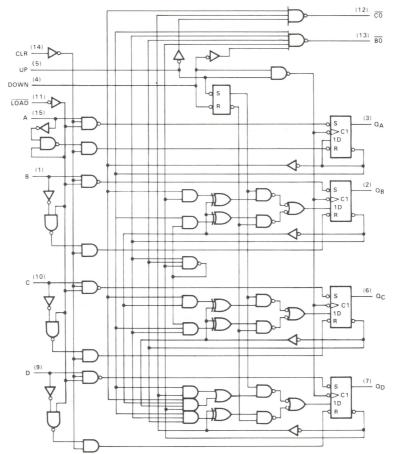
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TYPES SN54ALS192, SN74ALS192 SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS (DUAL CLOCK WITH CLEAR)

'ALS192 logic symbol

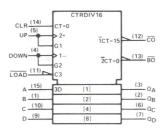


'ALS192 logic diagram (positive logic)

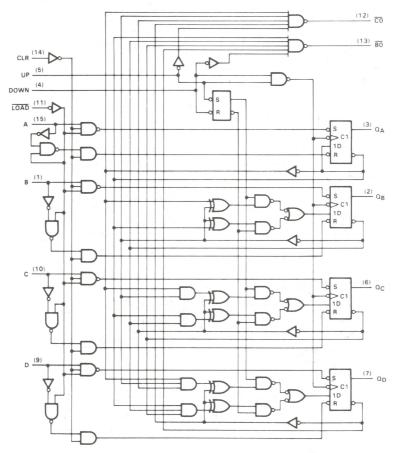


Pin numbers shown are for J and N packages

'ALS193 logic symbol



'ALS193 logic diagrams (positive logic)



Pin numbers shown are for J and N packages

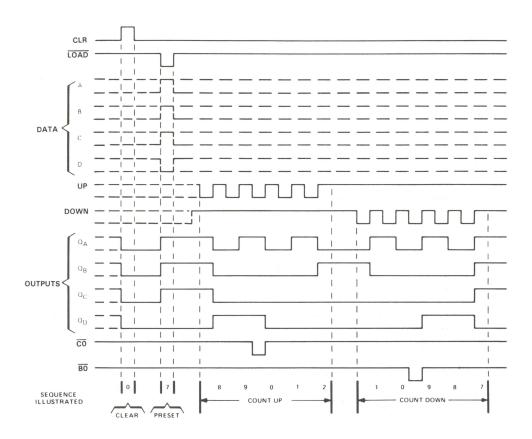
TYPES SN54ALS192, SN74ALS192 SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS (DUAL CLOCK WITH CLEAR)

typical clear, load, and count sequence

'ALS192

Illustrated below is the following sequence:

- 1. Clear outputs to zero.
- 2. Load (preset) to BCD seven.
- 3. Count up to eight, nine, carry, zero, one, and two.
- 4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

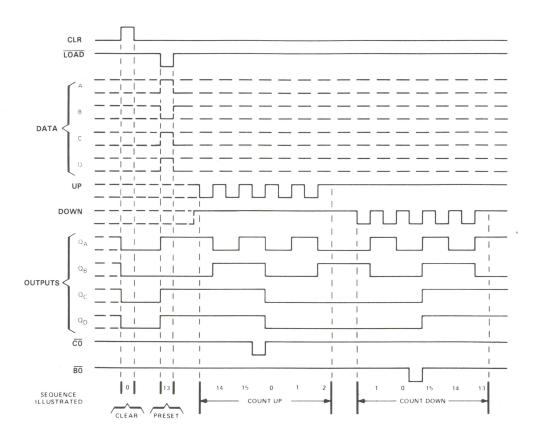
TYPES SN54ALS193, SN74ALS193 SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS (DUAL CLOCK WITH CLEAR)

typical clear, load, and count sequences

'ALS193

Illustrated below is the following sequence:

- 1. Clear outputs to zero.
- 2. Load (preset) to binary thirteen.
- 3. Count up to fourteen, fifteen, carry, zero, one, and two.
- 4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

TYPES SN54ALS192, SN54ALS193, SN74ALS192, SN74ALS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		
Input voltage	* * * * * * * * * * * * * * * * * * * *	
Operating free-air temperature range:	SN54ALS192, SN54ALS193	55 °C to 125 °C
	SN74ALS192, SN74ALS193	
Storage temperature range		GE 0C += 1 EO 0C

recommended operating conditions

				154ALS1 154ALS1				SN74ALS192 SN74ALS193		
			MIN	NOM	MAX	MIN	NOM	MAX		
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	· V	
V_{IH}	High-level input vo	oltage	2			2			V	
VIL	Low-level input voltage				0.8			0.8	V	
ЮН	High-level output	current			-0.4			-0.4	mA	
lOL	Low-level output	current			4			8	mA	
4	Clash for succession	'ALS192	0		25	0		25		
fclock	Clock frequency	'ALS193	0		25	0		25	MHz	
		CLR high	20			20			ns	
		TOAD low	25			25				
t _w	Pulse duration	Up or Down high	20			20				
		Up or Down low	20			20				
		Data before LOAD†	20			20				
t _{su}	Setup time	CLR inactive before Up1 or Down1	5			5			ns	
		LOAD inactive before Upt or Downt	15			15				
		Data after LOAD†	0			0				
th	Hold time	Up high after Down†	0			0			ns	
		Down high after Upf	0			0			1	
TA	Operating free-air	temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				_						
			SN54ALS192 SN54ALS193		SN74ALS192 SN74ALS193			UNIT		
PAF	RAMETER	TEST CONDITIONS		MIN		MAX	MIN	TYP‡	MAX	01111
VIK		V _{CC} = 4.5 V,	I _I = -18 mA			- 1.5			- 1.5	V
Vон			$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2						V
∨ОН			$I_{OH} = -0.4 \text{ mA}$				V _{CC} -	2		· ·
1/		VCC = 4.5 V,	IOL = 4 mA		0.25	0.4		0.25	0.4	V
VOL		V _{CC} = 4.5 V,	I _{OL} = 8 mA					0.35	0.5	v
I.	Up, Down	\/ F F \/	$= 5.5 \text{ V}, \qquad \text{V}_{1} = 7 \text{ V}$			0.1			0.1	^
Ч	All others	VCC = 5.5 V,				0.1			0.1	mA
Local	Up, Down	Vcc = 5.5 V,	$V_1 = 2.7 V$			20			20	_
ΊΗ	All others	VCC = 5.5 V,	V = 2.7 V			20			20	μА
	Up, Down	V F F V	V 04V			- 0.1			- 0.1	
IIL	All others	$V_{CC} = 5.5 V,$	$V_{\parallel} = 0.4 V$			-0.1			-0.1	mA
10*		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	-30		-112	mA
lcc		$V_{CC} = 5.5 V$,	See Note 1			17			17	mA

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 \,^{\circ}\text{C}$.

^{*}The current produced by grounding the outputs is approximately twice that produced with 2.25 V on the outputs.

NOTE 1: I_{CC} is measured with the clear and load inputs gounded, and all other inputs at 4.5 V.

TYPES SN54ALS192, SN54ALS193, SN74ALS192, SN74ALS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54	$V_{CC} = 4.5$ $C_{L} = 50 \text{ pl}$ $R_{L} = 500 \text{ s}$ $T_{A} = MIN$ $ALS192$ $ALS193$	to MAX	ALS192 ALS193	UNIT
			MIN	MAX	MIN	MAX	
fmax	'AL	S192	25		25		
	'AL	S193	25		25		MHz
^t PLH	Up CO	00	4	18	4	18	ns
tPHL	Ор	CO	5	18	5	18	1115
t _{PLH}	Down	ВО	4	18	4	18	ns
tPHL	Down	ьо	5	18	5	18	115
tPLH		Any Q	4	35	4	33	ns
t _{PHL}	Up or Down	Any Q	4	35	4	33	IIS
^t PLH	LOAD	Any Q	8	48	8	45	
^t PHL	LOAD	Any Q	8	35	8	35	ns
t _{PHL}	CLR	Any Q	5	30	5	30	ns



TYPES SN54ALS240, SN54ALS241 SN74ALS240, SN74ALS241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{\mathbb{G}}$ (active-low output control) inputs, and complementary \mathbb{G} and $\overline{\mathbb{G}}$ inputs. These devices feature high fan-out and improved fan-in.

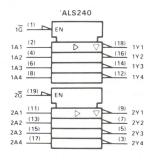
The SN54' family is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

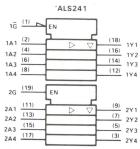
(TO	(TOP VIEW)								
1G 1 1A1 2 2Y4 3 1A2 4 2Y3 5 1A3 6 2Y2 7	P VIEW) 20 19 18 17 16 15 14	V _{CC} 2G/2G* 1Y1 2A4 1Y2 2A3 1Y3							
2Y2	14] 13] 12] 11]	1Y3 2A2 1Y4 2A1							

*2G for 'ALS240 or 2G for 'ALS241

J Suffix—Case 732-03 (Ceramic) N Suffix—Case 738-01 (Plastic)

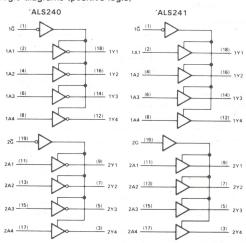
logic symbols





Pin numbers shown are for J and N packages.

logic diagrams (positive logic)



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TYPES SN54ALS240, SN54ALS241, SN74ALS240, SN74ALS241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 \vee
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS240, SN54ALS241	– 55 °C to 125 °C
SN74ALS240, SN74ALS241	0 °C to 70 °C
Storage temperature range	65 °C to 150 °C

recommended operating conditions

		SN	154ALS2	240	SN	74ALS2	240	
		SN	154ALS2	241	SN74ALS241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
1	Uinh lavel autout auront			- 12				^
Іон	High-level output current						- 15	mA
lo:	Low-level output current			12				
IOL	Low-level output current				24	mA		
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CONDITIONS			SN54ALS240 SN54ALS241		SN74ALS240 SN74ALS241			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
VIK		V _{CC} = 4.5 V,	$I_{\parallel} = -18 \text{ mA}$			- 1.5			- 1.5	V
		V _{CC} = 4.5 V,	IOH = -3 mA	2.4	3.2		2.4	3.2	-	
Vон		V _{CC} = 4.5 V,	IOH = -12 mA	2						V
		V _{CC} = 4.5 V,	I _{OH} = -15 mA				2			
1/		V _{CC} = 4.5 V,	IOL = 12 mA		0.25	0.4		0.25	0.4	V
VOL		V _{CC} = 4.5 _V ,	I _{OL} = 24 mA					0.35	0.5	ľ
lozh		V _{CC} = 5.5 V,	V _O = 2.7 V			20			20	μА
OZL		V _{CC} = 5.5 V,	V _O = 0.4 V			- 20			- 20	μΑ
ll		V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
lΗ		V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μА
ΊL		$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			-0.1	mA
10*		$V_{CC} = 5.5 V,$	V _O = 2.25 V	-30		-112	-30		-112	mA
			Outputs high			11.5			11.5	
	'ALS240		Outputs low			22			22	
lcc		V00 - 5 5 V	Outputs disabled			25			25	
	'ALS241	V _{CC} = 5.5 V	Outputs high			11.5			11.5	mA
			Outputs low			23			23	
			Outputs disabled			27			27	

 $[\]pm$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

^{*}The current produced by grounding the outputs is approximately twice that produced with 2.25 V on the outputs.

TYPES SN54ALS240, SN54ALS241, SN74ALS240, SN74ALS241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

'ALS240 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R1 = 500 \Omega$ $R2 = 500 \Omega$ $T_A = MIN \text{ to}$ $LS240$ MAX	MAX	ALS240 MAX	UNIT
tPLH		V	3	12	3	10	
tPHL	A	Y	2	11	2	9	ns
[†] PZH	G	V	5	22	5	20	
^t PZL	9	4	5	30	5	28	ns
^t PHZ	G	V	2	15	2	13	ns
^t PLZ	9	· ·	3	21	3	17	113

'ALS241 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	3	$\begin{array}{c} V_{CC} = 4.5 \text{ V to 5} \\ C_{L} = 50 \text{ pF,} \\ R1 = 500 \Omega, \\ R2 = 500 \Omega, \\ T_{A} = \text{MIN to MAX} \\ \text{SN54ALS241} \qquad \text{S} \end{array}$		ALS241	UNIT
			MIN	MAX	MIN	MAX	
t _{PLH}		Υ	3	14	3	12	
tPHL	Α	Y	3	13	3	10	ns
^t PZH	1G	V	7	25	7	21	
†PZL		4	7	25	7	21	ns
[†] PHZ	1G	V	2	18	2	16	ns
[†] PLZ		'	3	26	3	20	115
[†] PZH	2 G	· · · · · · · · · · · · · · · · · · ·	7	25	7	21	ns
^t PZL	1 20	'	7	25	7	21	115
^t PHZ	2G	ν	2	18	2	16	ns
^t PLZ	25	<u>'</u>	3	26	3	20	115



TYPES SN54ALS242, SN54ALS243, SN74ALS242, SN74ALS243, QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- 2-Way Asynchronous Communication Between Data Buses
- P-N-P Inputs Reduce Loading

description

These four-data-line transceivers are designed for asynchronous two-way communications between data buses. The SN74' devices can be used to drive terminated lines down to 100 ohms.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

(TOP VIEW)

ĞАВ	1	U 14		VCC
NC	2	13		GBA
A1	3	12		NC
A2	4	11		B1
А3	5	10		B2
A4	□6	9		В3
GND	\prod_{7}	8	П	B4

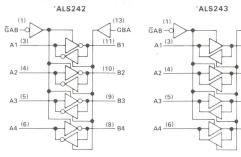
J Suffix-Case 632-07 (Ceramic) N Suffix-Case 646-05 (Plastic)

logic symbol

'ALS242 GBA GBA EN1 EN1 $\overline{\mathsf{G}}\mathsf{A}\mathsf{B}$ GAB EN2 EN2 B1 A1 10) R2 A2 B3 A3 B4 A4 B4

'ALS243

logic diagrams (positive logic)



Pin numbers shown are for J and N packages

FUNCTION TABLE

INP	UTS	'ALS242	'ALS243	
GAB	GBA	AL3242	AL3243	
L	L	Ā to B	A to B	
Н	Н	B̄ to A	B to A	
Н	L	Isolation	Isolation	
		Latch A and B	Latch A and B	
L	Н	$(A = \overline{B})$	(A = B)	

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- GBA

(10) B2

(<u>9)</u> B3

(8) B4

TYPES SN54ALS242, SN54ALS243, SN74ALS242, SN74ALS243 QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage: All inputs
I/O ports
Operating free-air temperature range: SN54ALS242, SN54ALS243 – 55 °C to 125 °C
SN74ALS242, SN74ALS243 0 °C to 70 °C
Storage temperature range

recommended operating conditions

		SN	154ALS2	242	SN	74ALS2	242		
		SN	SN54ALS243		SN74ALS243			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	Oldii	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
V _{IL}	Low-level input voltage			0.8			0.8	V	
	Ular land and an install			- 12				mA	
ЮН	High-level output current						- 15	I IIIA	
				12				^	
OL	Low-level output current						24	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST	CONDITIONS	1	154ALS2 154ALS2			174ALS2 174ALS2		UNIT	
	* *			MIN	TYP‡	MAX	MIN	TYP‡	MAX	Oldii	
VIK		$V_{CC} = 4.5 V,$	$I_{I} = -18 \text{ mA}$			-1.5			- 1.5	V	
		V _{CC} = 4.5 V,	10H = -3 mA	2.4	3.2		2.4	3.2			
Vон		$V_{CC} = 4.5 V$,	$I_{OH} = -12 \text{ mA}$	2						V	
		V _{CC} = 4.5 V,	I _{OH} = -15 mA				2			-	
		$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4		
v_{OL}		V _{CC} = 4.5 V,	I _{OL} = 24 mA					0.35	0.5	V	
	Control inputs	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA	
I ₁	A or B ports	V _{CC} = 5.5 V,	V _I = 5.5 V			0.1			0.1	MA	
	Control inputs	V F F V	$V_i = 2.7 V$		100	20			20	μА	
ΙН	A or B ports▲	vCC = 5.5 v,				20			20		
	Control inputs	\/ E E \/	V: - 0 4 V			⊣0.1			- 0.1	mA	
IIL	A or B ports▲	$V_{CC} = 5.5 V,$	V = 0.4 V			-0.1			-0.1	mA	
10*		$V_{CC} = 5.5 V,$	V _O = 2.25 V	-30		-112	-30		-112	mA	
			Outputs high			19			19		
	'ALS242		Outputs low			25			25		
1		V _{CC} = 5.5 V	Outputs disabled			25			25	mA	
ICC		VCC - 5.5 V	Outputs high			19			19		
	'ALS243		Outputs low			25			25		
			Outputs disabled			27			27	1	

 $[\]pm$ All typical values are at VCC = 5 V, TA = 25 °C.

^{*}The current produced by grounding the outputs is approximately twice that produced with 2.25 V on the outputs.

 $[\]blacktriangle For I/O$ ports, the parameters $I_{\mbox{\scriptsize IH}}$ and $I_{\mbox{\scriptsize IL}}$ include the off-state output current.

TYPES SN54ALS242, SN54ALS243, SN74ALS242, SN74ALS243 QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

'ALS242 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_1 = 500 \text{ s}$ $R_2 = 500 \text{ s}$ $T_A = MIN \text{ s}$	=, Ω, Ω,		UNIT
=			SN54	ALS242	SN74ALS242		1
			MIN	MAX	MIN	MAX	1
^t PLH	A or B	B or A	3	15	3	1.1	ns
tPHL		BOLA	2	14	2	10	l lis
tPZH	GAB	В	4	24	4	22	ns
tPZL	GAB	JAB	7	32	7	30	- ns
^t PHZ	GAB	В	2	18	2	16	ns
tPLZ	GAB	Ь	4	28	4	25	1 115
^t PZH	GBA	A	4	24	4	22	ns
^t PZL	GDA	^	7	32	7	30	1 115
^t PHZ	GBA	A	2	18	2	16	ns
^t PLZ	GDA	^	4	28	4	25	1 115

'ALS243 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_1 = 500 \text{ s}$ $R_2 = 500 \text{ s}$ $T_A = MIN \text{ s}$	=, Ω, Ω,		UNIT
			SN54/	ALS243	SN74ALS243		1
			MIN	MAX	MIN	MAX	
tPLH	A or B	B or A	4	15	4	11	ns
^t PHL	AOFB	BOIA	4	15	4	11	115
^t PZH	GAB	В	7	25	7	23	ns
tPZL	GAB	В	7	26	7	24	1 115
^t PHZ	GAB	В	2	20	2	18	ns
tPLZ	GAB	В	4	30	4	25	1 115
^t PZH	GBA	Α	7	25	7	23	ns
tPZL	GDA	^	7	26	7	24	1 115
^t PHZ	GBA	A	2	20	2	18	ns
tPLZ	J. GDA	^	4	30	4	25	1 115



TYPES SN54ALS244, SN74ALS244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ALS240, and 'ALS241, these devices provide the choice of selected combinations of inverting outputs, symmetrical \overline{G} (active-low input control) inputs, and complementary G and \overline{G} inputs.

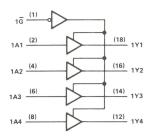
The SN54ALS244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS244 is characterized for operation from 0°C to 70°C.

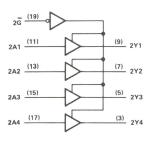
(TOP VIEW)

1G	1.	U 20	Vcc
1A1	2	19	$2\overline{G}$
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1
	_		

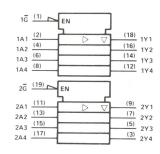
J Suffix—Case 732-03 (Ceramic) N Suffix—Case 738-01 (Plastic)

logic diagram (positive logic)





logic symbol



Pin numbers shown are for J and N packages.

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TYPES SN54ALS244, SN74ALS244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
Input voltage	
Voltage applied to a disabled 3-state output	
Operating free-air temperature range: SN54ALS244	
SN74ALS244	
Storage temperature range - 65 °C to 150 °C	

recommended operating conditions

			SN54ALS244			SN74ALS244		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-leve! input voltage			0.8			0.8	V
				- 12				
ЮН	High-level output current						- 15	mA
				12				
lOL	Low-level output current						24	mA
ТД	Operating free-air temperature	- 55	-	125	0	1.8	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SN54ALS244			SN74ALS244			UNIT
PARAMETER	TEST CON	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNI	
VIK	$V_{CC} = 4.5 V$	$I_{I} = -18 \text{ mA}$			- 1.5			- 1.5	V
	$V_{CC} = 4.5 V$,	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		
VoH	$V_{CC} = 4.5 V$	$I_{OH} = -12 \text{ mA}$	2						\ \
	$V_{CC} = 4.5 V_{,}$	I _{OH} = -15 mA				2			
	$V_{CC} = 4.5 V.$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5	
lozh	$V_{CC} = 5.5 V$,	V _O = 2.7 V			20			20	μA
lozL	V _{CC} = 5.5 V,	V _O = 0.4 V			- 20			- 20	μA
l ₁	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	m
lн	V _{CC} = 5.5 V,	V _I = 2.7 V			20			2.0	μA
IL	$V_{CC} = 5.5 V$,	V _! = 0.4 V			-0.1			- 0.1	m
10*	$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		- 112	- 30		- 112	m
lcc		Outputs high			11.5			11.5	
	$V_{CC} = 5.5 V$	Outputs low		,	23			23	m
		Outputs disabled			27			27	1

[‡]All typical values are at V $_{CC}~=~5$ V, $T_{A}~=~25\,^{o}C.$

^{*}The current produced by grounding the outputs is approximately twice that produced with 2.25 V on the outputs.

TYPES SN54ALS244, SN74ALS244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

switching characteristics

	FROM	то		$V_{CC} = 4.5$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega$		٧,	W	
PARAMETER	PARAMETER (INPUT)	NPUT) (OUTPUT)		R2 = 500Ω , $T_A = MIN \text{ to MAX}$ $SN54ALS244 \qquad SN74ALS244$				
			MIN	MAX	MIN	MAX	1	
tPLH		V	3	14	3	11		
tPHL	A	Y	3	13	3	10	ns	
^t PZH	G	Y	7	25	7	21		
tPZL		7	7	25	7	21	ns	
^t PHZ	G	Y	2	15	2	14	ns	
t _{PLZ}	G G	•	3	22	3	17	115	



TYPES SN54ALS245, SN74ALS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines Directly
- P-N-P Inputs Reduce DC Loading

description

These octal bus transceivers are designed for synchronous twoway communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input (\overline{G}) can be used to disable the device so that the buses are effectively isolated.

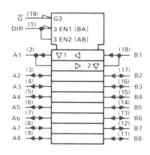
The SN54ALS245 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS245 is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

(TOP VIEW)

DIR	1	U 20		Vcc
A1 [2	19		G
A2 [3	18		B1
A3 [4	17		B2
A4 [5	16		В3
A5 [6	15		B4
A6 [7	14		B5
A7 [8	13		B6
A8 [9	12		B7
GND [10	11	П	B8

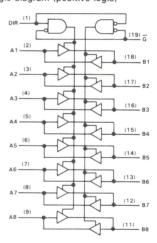
J Suffix—Case 732-03 (Ceramic) N Suffix—Case 738-01 (Plastic)

logic symbol



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



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TYPES SN54ALS245, SN74ALS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
Input voltage: All inputs	7 V
I/O ports	
Operating free-air temperature range:	SN54ALS245
	SN74ALS245
Storage temperature range	- 65 °C to 150 °C

recommended operating conditions

		SN	SN54ALS245		SN			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			- 12				mA
OH	riigii-level output current						- 15	mA
1	Low lovel extent extent			12				
lor	Low-level output current						24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAD	AMETER	TECT	CONDITIONS	SN	54ALS2	245	SN	74ALS2	45	UNIT
PAH	AMETER	l IEST	CONDITIONS	MIN	TYP‡	MAX	MIN	TYP:	MAX	UNII
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			- 1.5			- 1.5	V
		V _{CC} = 4.5 V,	IOH = -3 mA	2.4	3.2		2.4	3.2		
Vон		V _{CC} = 4.5 V,	IOH = -12 mA	2						V
		V _{CC} = 4.5 V,	IOH = -15 mA				2			
		$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL		V _{CC} = 4.5 V,	I _{OL} = 24 mA					0.35	0.5	V
	Control inputs	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
Ц	A or B ports	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1	mA
1	Control inputs	Vcc = 5.5 V,	V: - 2.7.V			20			20	_
ΊН	A or B ports▲	vCC = 5.5 v,	V = 2.7.V			20			20	μА
	Control inputs	Vcc = 5.5 V,	V ₁ = 0.4 V			-0.1			- 0.1	mA
IIL	A or B ports▲	VCC = 5.5 V,	V = 0.4 V			-0.1			0.1	mA
10*		$V_{CC} = 5.5 V$,	V _O = 2.25 V	-30		-112	-30		-112	mA
			Outputs high			35			35	
Icc		$V_{CC} = 5.5 V$	Outputs low			45			45	mA
			Outputs disabled			47.5			47.5	

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

^{*}The current produced by grounding the outputs is approximately twice that produced with 2.25 V on the outputs.

 $[\]Delta For I/O$ ports, the parameters $I_{\mbox{\footnotesize{IH}}}$ and $I_{\mbox{\footnotesize{IL}}}$ include the off-state output current.

TYPES SN54ALS245, SN74ALS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

switching characteristics

				VCC = 4.5	V to 5.5	٧,	
				$C_{L} = 50 p$	F,	. 14	
				R1 = 500	Ω,		
PARAMETER	FROM	то		× .	UNIT		
PARAMETER	(INPUT)	(OUTPUT)		$T_A = MIN \text{ to } MAX$			UNIT
			SN54ALS245		SN74ALS245		.13
			MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	3	16	3	12	ns
t _{PHL}	7 7018	8017	3	14	3	12	115
^t PZH	G	A or B	7	20	8	17	ns
t _{PZL}	3	2 01 5	10	22	10	20	115
^t PHZ	G	A or B	3	16	3	14	ns
tPLZ	7 3	7 01 0	4	23	4	20	115

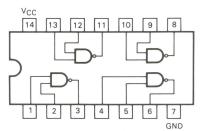
SCHOTTKY TTL



FAST Data Sheets



Advance Information QUAD 2-INPUT NAND GATE



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

MC54F00 MC74F00

QUAD 2-INPUT NAND GATE

FAST™ SCHOTTKY TTL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage*	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 O	25 25	125 70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70° C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMETER			LIMITS		LINUTC	TECT OF	MIDITIONIC		
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CC	V _{CC} = MIN, I _{IN} = -18 mA I _{OH} = -1.0 mA I _{OH} = -1.0 mA V _{CC} = MIN V _{CC} = MIN V _{CC} = MIN V _{CC} = MIN V _{CC} = MIN V _{CC} = MAX, V _{IN} = 2.7 V V _{CC} = MAX, V _{IN} = 7.0 V V _{CC} = MAX, V _{IN} = 0.5 V V _{CC} = MAX, V _{OUT} = 0 V		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpu	it HIGH Voltage		
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage			
VIK	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA			
V	Output HICH Voltage	54	2.5		*	V	I _{OH} = -1.0 mA			
VOH	Output HIGH Voltage	74	2.7			V	I _{OH} = -1.0 mA	ACC - MIIIA		
VOL	Output LOW Voltage				0.5	V	I _{OL} = 20 mA V _{CC} = MIN			
lu.	Input HIGH Current				20	μΑ	V _{CC} = MAX, V _{IN}	= 2.7 V		
lΗ	input nigh current				0.1	mA	V _{CC} = MAX, V _{IN}	= 7.0 V		
IIL	Input LOW Current				-0.6	mA	V _{CC} = MAX, V _{IN}	= 0.5 V		
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{CC} = MAX, V _{OI}	JT = 0 V		
Inc	Power Supply Current Total, Output HIGH				2.8	mA	V _{CC} = MAX, V _{IN} = GND			
ICC	Total, Output LOW				10.2	mA	I _{OH} = -1.0 mA I _{OH} = -1.0 mA V _{CC} = MIN V _{CC} = MAX, V _{IN} = 2.7 V V _{CC} = MAX, V _{IN} = 7.0 V V _{CC} = MAX, V _{IN} = 0.5 V V _{CC} = MAX, V _{OUT} = 0 V			

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

		54	74F	54	4F	7.	4F	
SYMBOL	PARAMETER			$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$		T _A = 0°C to 70°C		UNITS
		V _{CC} = +5.0 V C _L = 50 pF		V _{CC} = 5.0 V ± 10% C _L = 50 pF		V _{CC} = 5.0 V ± 5% C _L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	2.4	5.0	2.0	7.0	2.4	6.0	ns
tPHL	Propagation Delay	2.0	4.3	1.5	6.5	2.0	5.3	ns

AC TEST CIRCUIT

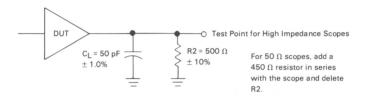
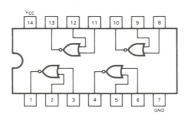


Fig. 1



Advance Information QUAD 2-INPUT NOR GATE



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

MC54F02 MC74F02

QUAD 2-INPUT NOR GATE

FAST™ SCHOTTKY TTL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage*	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ІОН	Output Current — High	54, 74			-1.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMBOL	DADAMETED			LIMITS		UNITS	TEST OF	MIDITIONIC	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	IOH = -1.0 mA IOH = -1.0 mA VCC = MIN VCC = MIN		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage		
VIL	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage		
VIK	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA		
	0	54	2.5			V	I _{OH} = -1.0 mA		
VOH	Output HIGH Voltage	74	2.7			V	I _{OH} = -1.0 mA	ACC = MIN	
VOL	Output LOW Voltage				0.5	V	I _{OL} = 20 mA V _{CC} = MIN		
Local	I				20	μА	V _{CC} = MAX, V _{IN}	= 2.7 V	
lН	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _{IN}	= 7.0 V	
IIL	Input LOW Current				-0.6	mA	V _{CC} = MAX, V _{IN}	= 0.5 V	
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V		
l	Power Supply Current Total, Output HIGH				5.6	mA	V _{CC} = MAX, V _{IN} = GND		
ICC	Total, Output LOW				13	mA	V _{CC} = MAX, V _{IN}	= Note 3	

NOTES:

- 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.
- 3. Measured with one input high, one input low for each gate.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

		54/74F		5-	4F	7	4F	
SYMBOL	PARAMETER	T _A =	+25°C	T _A = -55°($T_A = -55^{\circ}C \text{ to } +125^{\circ}C$		C to 70°C	LIMITO
STIVIBUL	FANAIVIETER	V _{CC} = +5.0 V		$V_{CC} = 5.0 V \pm 10\%$		V _{CC} = 5.0 V ± 5%		UNITS
		C _L = 50 pF		CL=	50 pF	C _L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	2.5	5.5	2.5	7.5	2.5	6.5	ns
tPHL	Propagation Delay	2.0	4.3	1.5	6.5	2.0	5.3	ns

AC TEST CIRCUIT

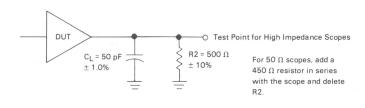
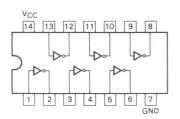


Fig. 1

MOTOROLA SCHOTTKY TTL DEVICES



Advance Information HEX INVERTER



J Suffix — Case 632-07 (Ceramic) N Suffix - Case 646-05 (Plastic)

MC54F04 MC74F04

HEX INVERTER FAST™ SCHOTTKY TTL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
Vcc	Supply Voltage*	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 O	25 25	125 70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMETER			LIMITS		UNITS	TEST CO	ONDITIONS	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS Guaranteed Input HIGH Voltage Guaranteed Input LOW Voltage $V_{CC} = MIN, I_{IN} = -18 \text{ mA}$ $I_{OH} = -1.0 \text{ mA}$ $I_{OH} = -1.0 \text{ mA}$ $I_{OL} = 20 \text{ mA}$ $V_{CC} = MIN$ $V_{CC} = MIN$ $V_{CC} = MIN$		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage		
VIL	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage		
VIK	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA		
1/	0	54	2.5			V	I _{OH} = -1.0 mA		
VOH	Output HIGH Voltage	74	2.7			V	I _{OH} = -1.0 mA	ACC = IMIIM	
VOL	Output LOW Voltage				0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
Local	I				20	μΑ	V _{CC} = MAX, V _{IN}	= 2.7 V	
lН	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _{IN}	= 7.0 V	
IIL	Input LOW Current				-0.6	mA	V _{CC} = MAX, V _{IN}	= 0.5 V	
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{CC} = MAX, V _O	UT = 0 V	
1	Power Supply Current Total, Output HIGH				4.2	mA	V _{CC} = MAX, V _{IN}	= GND	
ICC	Total, Output LOW				15.3	mA	V _{CC} = MAX, V _{IN}	= Open	

NOTES:

- 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second. This document contains information on a new product. Specifications and information herein

are subject to change without notice.

		54/	74F	54	54F		4F	
SYMBOL	PARAMETER	T _A = -	+25°C			TA = 0°0	C to 70°C	UNITS
STWIBOL	FANAIVIETEN	V _{CC} = +5.0 V		V _{CC} = 5.0 V ± 10%		$V_{CC} = 5.0 V \pm 5\%$		UNITS
		C _L = 50 pF		C _L = 50 pF		C _L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	2.4	5.0	2.0	7.0	2.4	6.0	ns
tPHL	Propagation Delay	2.0	4.3	1.5	6.5	2.0	5.3	ns

AC TEST CIRCUIT

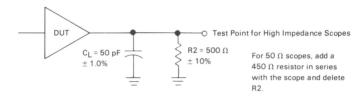
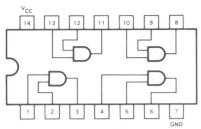


Fig. 1



Advance Information OUAD 2-INPUT AND GATE



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

MC54F08 MC74F08

QUAD 2-INPUT AND GATE

FAST™ SCHOTTKY TTL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage*	54 74	4.5 4.75	5.0 5.0	5.5 5.25	٧
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70° C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMETER			LIMITS		LIMITO	TEST OF	MIDITIONS
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CC	NDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Volta	
VIL	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltag	
VIK	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} =	-18 mA
V	0	54	2.5			V	I _{OH} = -1.0 mA	V BAINI
VOH	Output HIGH Voltage	74	2.7			V	I _{OH} = -1.0 mA	VCC = MIN
VOL	Output LOW Voltage				0.5	V	I _{OL} = 20 mA V _{CC} = MIN	
l	Innut MICH Correct				20	μΑ	V _{CC} = MAX, V _{IN}	= 2.7 V
lΗ	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _{IN}	= 7.0 V
IIL	Input LOW Current				-0.6	mA	V _{CC} = MAX, V _{IN}	= 0.5 V
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V	
Leave	Power Supply Current Total, Output HIGH				8.3	mA	V _{CC} = MAX, V _{IN} = Open	
ICC	Total, Output LOW				12.9	mA	V _{CC} = MAX, V _{IN}	= GND

NOTES:

- 1. For conditions shown as MIN or MAX, use the appropiate value specified under recommended operating conditions for the applicable device type.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

	2 2 2 3 3 3	54/74F		54	F	7	4F	
SYMBOL	PARAMETER		+25°C	T _A = -55°C to +125°C		T _A = 0°C to 70°C		UNITS
	TANAMETER		V _{CC} = +5.0 V C _L = 50 pF		V ± 10% 50 pF	V _{CC} = 5.0 V ± 5% C _L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	3.0	5.6	2.5	7.5	3.0	6.6	ns
tPHL	Propagation Delay	2.5	5.3	2.0	7.5	2.5	6.3	ns

AC TEST CIRCUIT

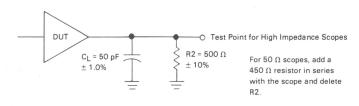
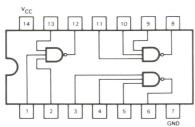


Fig. 1



Advance Information TRIPLE 3-INPUT NAND GATE



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

MC54F10 MC74F10

TRIPLE 3-INPUT NAND GATE

FAST™ SCHOTTKY TTL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
Vcc	Supply Voltage*	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70° C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CO	NDITIONS
STIVIBUL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CC	MUITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpu	it HIGH Voltage
VIL	Input LOW Voltage				0.8	V	Guaranteed Inpu	it LOW Voltage
VIK	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} =	-18 mA
\/o	Output HIGH Voltage	54	2.5			V	I _{OH} = -1.0 mA	VCC = MIN
VOH	Output high voitage	74	2.7			V	$I_{OH} = -1.0 \text{ mA}$	ACC - MIIM
VOL	Output LOW Voltage				0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
į	Input HIGH Current				20	μΑ	V _{CC} = MAX, V _{IN}	= 2.7 V
lН	input high current				0.1	mA	V _{CC} = MAX, V _{IN}	= 7.0 V
IIL	Input LOW Current				-0.6	mA	V _{CC} = MAX, V _{IN}	= 0.5 V
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V	
	Power Supply Current Total, Output HIGH				2.1	mA	V _{CC} = MAX, V _{IN} = GND	
ICC	Total, Output LOW				7.7	mA	V _{CC} = MAX, V _{IN}	

NOTES

- 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

		54/74F T _A = +25°C V _{CC} = +5.0 V C _I = 50 pF		54	4F	74		
SYMBOL	PARAMETER			V _{CC} = 5.0	to +125°C V ± 10% 50 pF	$T_A = 0^{\circ}C \text{ to } 70^{\circ}C$ $V_{CC} = 5.0 \text{ V} \pm 5\%$ $C_1 = 50 \text{ pF}$		UNITS
				-	· ·		· · · · · · · · · · · · · · · · · · ·	
		MIN	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	2.4	5.0	2.0	7.0	2.4	6.0	ns
tPHL	Propagation Delay	2.0	4.3	1.5	6.5	2.0	5.3	ns

AC TEST CIRCUIT

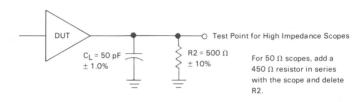
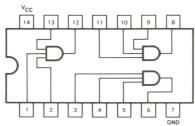


Fig. 1



Advance Information TRIPLE 3-INPUT AND GATE



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

MC54F11 MC74F11

TRIPLE 3-INPUT AND GATE

FAST™ SCHOTTKY TTL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage*	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
IOL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CO	NDITIONS
STIVIBOL	FARAMETER		MIN	TYP	MAX	UNITS	1231 00	MUITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Inpu	it HIGH Voltage
VIL	Input LOW Voltage				0.8	V	Guaranteed Inpu	it LOW Voltage
VIK	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} =	-18 mA
\/a	Output HICH Valtage	54	2.5			V	I _{OH} = -1.0 mA	\/ NAINI
VOH	Output HIGH Voltage	74	2.7			V	I _{OH} = -1.0 mA	V _{CC} = MIN
VOL	Output LOW Voltage				0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I	Input HIGH Current				20	μА	V _{CC} = MAX, V _{IN}	= 2.7 V
lН	input high current				0.1	mA	V _{CC} = MAX, V _{IN}	= 7.0 V
IIL	Input LOW Current				-0.6	mA	V _{CC} = MAX, V _{IN}	= 0.5 V
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V	
la-	Power Supply Current Total, Output HIGH				6.2	mA	V _{CC} = MAX, V _{IN} = Open	
ICC	Total, Output LOW				9.7	mA	V _{CC} = MAX, V _{IN}	= GND

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SYMBOL	PARAMETER	54/74F TA = +25°C VCC = +5.0 V C ₁ = 50 pF		V _{CC} = 5.0	C to +125°C O V ± 10%	74F T _A = 0°C to 70°C V _{CC} = 5.0 V ± 5% C _L = 50 pF		UNITS
		MIN	MAX	C _L =	MAX	MIN	MAX	
tPLH	Propagation Delay	3.0	5.6	2.5	7.5	3.0	6.6	ns
tPHL	Propagation Delay	2.5	5.5	2.0	7.5	2.5	6.5	ns

AC TEST CIRCUIT

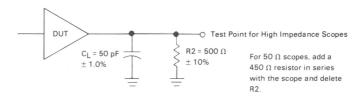
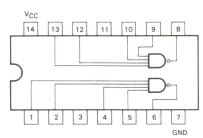


Fig. 1



Advance Information DUAL 4-INPUT NAND GATE



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

MC54F20 MC74F20

DUAL 4-INPUT NAND GATE

FAST™ SCHOTTKY TTL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
Vcc	Supply Voltage*	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
lOL	Output Current — Low	54, 74			20	mA

 $^{^*74}$ F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TEST CO	NDITIONS	
STIVIBUL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CC	INDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpu	t HIGH Voltage	
VIL	Input LOW Voltage				0.8	V	Guaranteed Inpu	t LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} =	-18 mA	
	0	54	2.5			V	I _{OH} = -1.0 mA	\/ BAIN	
VOH	Output HIGH Voltage	74	2.7			V	I _{OH} = -1.0 mA	V _{CC} = MIN	
VOL	Output LOW Voltage				0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
I	Innut IIICH Current				20	μΑ	V _{CC} = MAX, V _{IN}	= 2.7 V	
lН	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _{IN}	= 7.0 V	
IIL	Input LOW Current				-0.6	mA	V _{CC} = MAX, V _{IN}	= 0.5 V	
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V		
laa	Power Supply Current Total, Output HIGH				1.4	mA	V _{CC} = MAX, V _{IN} = GND		
ICC	Total, Output LOW				5.1	mA	V _{CC} = MAX, V _{IN}	= Open	

NOTES:

- 1. For conditions shown as MIN or MAX, use the appropiate value specified under recommended operating conditions for the applicable device type.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

		54/74F T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		54	4F	7,	4F	
SYMBOL	PARAMETER			$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0 \text{ V} \pm 10\%$		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 5%		UNITS
				C _L = 50 pF		C _L = 50 pF		
		MIN	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	2.4	5.0	2.0	7.0	2.4	6.0	ns
tPHL	Propagation Delay	2.0	4.3	1.5	6.5	2.0	5.3	ns

AC TEST CIRCUIT

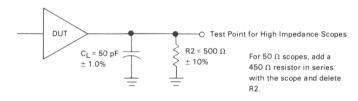
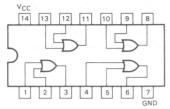


Fig. 1



Advance Information QUAD 2-INPUT OR GATE



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

MC54F32 MC74F32

QUAD 2-INPUT OR GATE

FASTTM SCHOTTKY TTL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage*	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТД	Operating Ambient Temperature Range	54 74	-55 O	25 25	125 70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
lOL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range and will meet the specifications of 54ALS devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX	UNITS	TEST CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
VIL	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA	
Vон	Output HIGH Voltage	54, 74	2.5			V	I _{OH} = -1.0 mA	VCC = MIN
		74	2.7			V	I _{OH} = -1.0 mA	ACC - MILIA
VOL	Output LOW Voltage				0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
ΊΗ	Input HIGH CUrrent				20	μΑ	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
IIL	Input LOW Current				-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V	
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V	
Icc	Power Supply Current Total, Output HIGH Total, Output LOW				9.2	mA mA	V _{CC} = MAX, V _{IN} = GND V _{CC} = MAX, V _{IN} = Open	

NOTES:

- 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SYMBOL	PARAMETER	54/74F T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		54F T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		74F T _A = 0°C to 70°C V _{CC} = 5.0 V ± 5% C _L = 50 pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	3.0	5.6	3.0	7.5	3.0	6.6	ns
tPHL	Propagation Delay	3.0	5.3	2.5	7.5	3.0	6.3	ns

AC TEST CIRCUIT

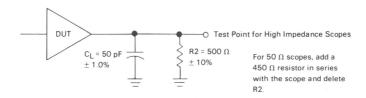
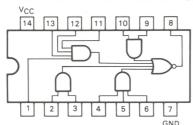


Fig. 1



Advance Information

4-2-3-2-INPUT AND-OR-INVERT GATE



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

MC54F64 MC74F64

4-2-3-2-INPUT AND-OR-INVERT GATE

FAST™ SCHOTTKY TTL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage*	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 O	25 25	125 70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
lOL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70° C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMADOL	DADAMETER			LIMITS		LINUTC	TEST CONDITIONS	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CC	NUTTONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltag	
VIL	Input LOW Voltage				0.8	V	Guaranteed Inpu	ıt LOW Voltage
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
1/	0	54	2.5			V	I _{OH} = -1.0 mA	\/
VOH	Output HIGH Voltage	74	2.7			V	I _{OH} = -1.0 mA	V _{CC} = MIN
VOL	Output LOW Voltage				0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
l	Innut HICH Current				20	μΑ	V _{IN} = 2.7 V	Vcc = MAX
lН	Input HIGH Current				0.1	mA	V _{IN} = 7.0 V	ACC - INIXX
IIL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
Leve	Power Supply Current Total, Output HIGH				2.8	mA	V _{IN} = GND	V _{CC} = MAX
ICC	Total, Output LOW				4.7	mA	V _{IN} = *	VCC - IVIAX

NOTES:

- 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.
- * I_{CCL} is measured with all inputs of one gate open and remaining inputs grounded.

FAST is a trademark of Fairchild Camera and Instrument Corporation.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

AC CHARACTERISTICS

	YMBOL PARAMETER		54/74F T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		1F	7		
SYMBOL					to +125°C V ± 10% 50 pF	T _A = 0°C to 70°C V _{CC} = 5.0 V ± 5% C _L = 50 pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	2.5	6.0	2.5	8.0	2.5	7.0	ns
tPHL	Propagation Delay	2.0	4.5	1.5	6.5	2.0	5.5	ns

AC TEST CIRCUIT

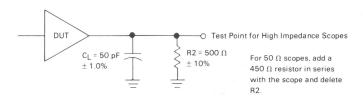


Fig. 1

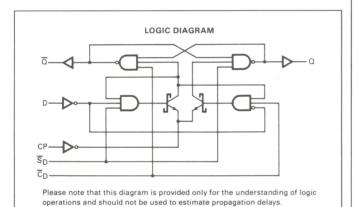
MOTOROLA SCHOTTKY TTL DEVICES



Advance Information

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The MC54F/74F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q,\overline{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.



TRUTH TABLE

(= 6	icii naii	,
INPUT	OUTF	PUTS
@ t _n	@ t _n	i i 1
D	Q	Q
L	L	Н
l H	Н	L

Asynchronous Inputs:

LOW Input to \overline{S}_D sets Q to HIGH level LOW Input to \overline{C}_D sets Q to LOW level Clear and Set are indepedent of clock Simultaneous LOW on \overline{C}_D and \overline{S}_D makes both Q and \overline{Q} HIGH

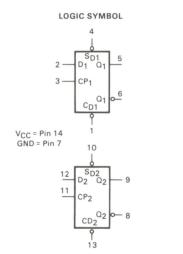
$$\begin{split} & \text{H} = \text{HIGH Voltage Level} \\ & \text{L} = \text{LOW Voltage Level} \\ & \text{t}_n = \text{Bit time before clock pulse} \\ & \text{t}_n + \text{1} = \text{Bit time after clock pulse} \end{split}$$

FAST is a trademark of Fairchild Camera and Instrument Corporation
This document contains information on a new product. Specifications and information herein
are subject to change without notice.

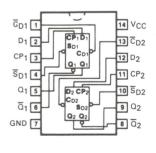
MC54F74 MC74F74

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

FAST™ SCHOTTKY TTL



CONNECTION DIAGRAM



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER	14 (17) 44	MIN	TYP	MAX	UNIT
1/	Complex Value = *	54	4.50	5.0	5.50	
VCC	Supply Voltage*	74	4.75	5.0	5.25	V
_	0 4	54	-55	25	125	
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ГОН	Output Current — High	54, 74	7		-1.0	mA
lOL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DARAMETER			LIMITS		LINUTC	TEST CONDITIONS		
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST C	UNDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp	ut HIGH Voltage	
VIL	Input LOW Voltage				0.8	V	Guaranteed Inp	ut LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
	0	54	2.5	3.4		V	I _{OH} = -1.0 mA	V/ 84181	
Vон	Output HIGH Voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	V _{CC} = MIN	
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
ler e	Inner IIICII Comment				20	μΑ	V _{IN} = 2.7 V	.,	
ΙΗ	Input HIGH Current				100	μА	V _{IN} = 7.0 V	V _{CC} = MAX	
IIL	Input LOW Current (CP and D Inputs)				-0.6	mA	V _{IN} = 0.5 V	Vcc = MAX	
'IL	$(\overline{C}_D \text{ and } \overline{S}_D \text{ Inputs})$				-1.8	mA	VIIV 0.0 V	VCC IVIAX	
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX	
Icc	Power Supply Current			10.5	16	mA	V _{CP} = 0 V	V _{CC} = MAX	

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

			54/74F		5-	54F		4F	
	SYMBOL PARAMETER		T _Δ = +25°C			to +125°C	T _A = 0 to +70°C		
SYMBOL			CC = +5.0	V	VCC = 5.0	0 V ±10%	V _{CC} = 5.	0 V ±5%	UNITS
			C _L = 50 pF			C _L = 50 pF		C _L = 50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}	Maximum Clock Frequency	100	125		100		100		MHz
tPLH tPHL	Propagation Delay CP_n to Q_n or \overline{Q}_n	3.8 4.4	5.3 6.2	6.8 8.0	3.8 4.4	8.5 10.5	3.8 4.4	7.8 9.2	ns
tPLH tPHL	Propagation Delay $\overline{\mathbb{C}}_{Dn}$ or $\overline{\mathbb{S}}_{Dn}$ to \mathbb{Q}_n or $\overline{\mathbb{Q}}_n$	3.2 3.5	4.6 7.0	6.1 9.0	3.2 3.5	8.0 11.5	3.2 3.5	7.1 10.5	ns

AC OPERATING REQUIREMENTS

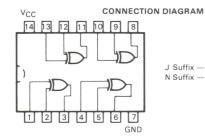
AC OF	HATTING REGOTHERING								
			54/74F		5	4F	7	4F	
SYMBOL	MBOL PARAMETER		TA = +25°			to +125°C			UNITS
OTWIDOL	TANAMETER	\	CC = +5.0) V	V _{CC} = 5.	0 V ±10%	V _{CC} = 5.	0 V ±5%	014110
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _s (H)	Set up Time, HIGH or LOW	2.0			3.0		2.0		
t _S (L)	D _n to CP _n	3.0			4.0		3.0		ns
th (H)	Hold Time, HIGH or LOW	1.0			2.0		1.0		
th (L)	D _n to CP _n	1.0		,	2.0		1.0		
t _w (H)	CP _n Pulse Width, HIGH	4.0			4.0		4.0		
$t_{W}(L)$	or LOW	5.0			6.0		5.0		ns
t _W (L)	CDn or SDn Pulse Width LOW	4.0			4.0		4.0		ns
trec	Recovery Time \overline{C}_{Dn} or \overline{S}_{Dn} to CP	2.0			3.0		2.0		ns



MC54F86 MC74F86

Advance Information

QUAD 2-INPUT EXCLUSIVE-OR GATE



J Suffix — Case 632-07 (Ceramic) N Suffix — Case 646-05 (Plastic) QUAD 2-INPUT EXCLUSIVE-OR GATE

FAST™ SCHOTTKY TTL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
	C	54	4.50	5.0	5.50	.,
vCC	V _{CC} Supply Voltage*		4.75	5.0	5.25	V
_		54	-55	25	125	
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
IOL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DARAMETER			LIMITS		LINUTC	TEST CONDITIONS	
STIVIBUL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CO	SMOITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Inp	ut HIGH Voltage
VIL	Input LOW Voltage				0.8	V	Guaranteed Inp	ut LOW Voltage
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN,
	0	54	2.5	3.4		V	I _{OH} = -1.0 mA	
VOH	Output HIGH Voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	V _{CC} = MIN
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I	Input HIGH Current				20	μΑ	V _{IN} = 2.7 V	\/ B4A\/
lН	input nigh current				100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX
IIL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
1	D			15	23	mA	Inputs LOW	\/
ICC	Power Supply Current			18	28		Inputs HIGH	V _{CC} = MAX

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

AC CHARACTERISTICS

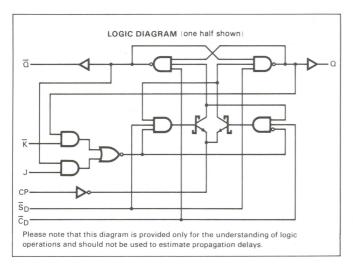
			54/74F			54F		4F	
			T _A = +25°	С	T _A = -55	to +125°C	TA = 0	to +70°C	
SYMBOL	PARAMETER	\	CC = +5.0	V	V _{CC} = 5.	0 V ±10%	V _{CC} = 5	.0 V ±5%	UNITS
		į.	C _L = 50 pF			C _L = 50 pF		C _L = 50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	3.0	4.0	5.5	3.0	7.0	3.0	6.5	
tPHL	(Other Input LOW)	3.0	4.2	5.5	3.0	7.0	3.0	6.5	ns
tPLH	Propagation Delay	3.5	5.3	7.0	3.5	8.5	3.5	8.0	20
^t PHL	(Other Input HIGH)	3.0	4.7	6.5	3.0	8.0	3.0	7.5	ns



Advance Information

DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

 $\begin{array}{l} \textbf{DESCRIPTION} - \text{The MC54F/74F109 consists of two high-speed,} \\ \text{completely independent transition clocked } J\overline{K} \text{ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform.} \\ \text{The } J\overline{K} \text{ design allows operation as a D flip-flop (refer to 'F74 data sheet) by connecting the J and } \overline{K} \text{ inputs together.} \\ \end{array}$



TRUTH TABLE

INF	PUTS	OUTPUTS
(0	0 t _n	@ t _{n + 1}
J	ĸ	Q Q
L L H	ILI	No Change L H H L
Н	L	Toggles

Asynchronous Inputs:

LOW Input to \overline{S}_D sets Q to HIGH level LOW Input to \overline{C}_D sets Q to LOW level Clear and Set are indepedent of clock Simultaneous LOW on \overline{C}_D and \overline{S}_D makes both Q and \overline{O} HIGH

 t_{Π} = Bit time before clock pulse t_{Π} + 1 = Bit time after clock pulse H = HIGH Voltage Level L = LOW Voltage Level

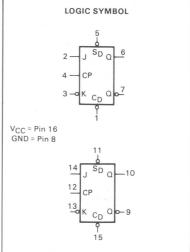
FAST is a trademark of Fairchild Camera and Instrument Corporation

This document contains information on a new product. Specifications and information herein are subject to change without notice.

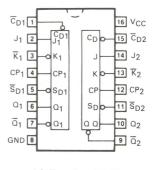
MC54F109 MC74F109

DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

FAST™ SCHOTTKY TTL



CONNECTION DIAGRAM



J Suffix — Case 620-08

(Ceramic)

N Suffix — Case 648-05 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage*	54 74	4.50 4.75	5.0 5.0	5.50 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 O	25 25	125 70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
IOL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

				LIMITS					
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CO	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpu	ut HIGH Voltage	
VIL	Input LOW Voltage				0.8	V	Guaranteed Inpu	ut LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
V		54	2.5	3.4		V	I _{OH} = -1.0 mA	\/ NAINI	
VOH	Output HIGH Voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	VCC = MIN	
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
loca	Input HIGH Current				20	μΑ	V _{IN} = 2.7 V	VCC = MAX	
lН	Input high current				100	μΑ	V _{IN} = 7.0 V	VCC - IVIAX	
IIL	Input LOW Current (J, K and CP Inputs)				-0.6	mA	V _{IN} = 0.5 V	VCC = MAX	
-12	$(\overline{C}_D \text{ and } \overline{S}_D \text{ Inputs})$				-1.8	mA	-114	100 1111	
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX	
Icc	Power Supply Current			11.7	17	mA	V _{CP} = 0 V	V _{CC} = MAX	

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	V _{CC} = +5.0 V			T _A = -55 t V _{CC} = 5.0	4F to +125°C O V ±10%	74F T _A = 0 to +70°C V _{CC} = 5.0 V ±5% C _L = 50 pF		UNITS
		CL = 50 pF CL = 50 MIN TYP MAX MIN			MAX	MIN	MAX		
f _{max}	Maximum Clock Frequency	90	125		90		90		MHz
tPLH tPHL	Propagation Delay CP_n to Q_n or \overline{Q}_n	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	9.0 10.5	3.8 4.4	8.0 9.2	ns
tPLH tPHL	Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to \overline{Q}_{n}	3.2 3.5	5.2 7.0	7.0 9.0	3.2 3.5	9.0 11.5	3.2 3.5	8.0 10.5	ns

AC OPERATING REQUIREMENTS

70 01 5	AIIIIO IIEGOIIIEIIIEII								
SYMBOL	PARAMETER	54/74F TA = +25°C VCC = +5.0 V			54F T _A = -55 to +125°C V _{CC} = 5.0 V ±10%		V _{CC} = 5.0 V ±5%		UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _S (H) t _S (L)	Set up Time, HIGH or LOW J_n or \overline{K}_n to CP_n	3.0 3.0			3.0		3.0		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW J_n or \overline{K}_n to CP_n	1.0 1.0			1.0 1.0		1.0		110
t _W (H)	CP _n Pulse Width, HIGH or LOW	4.0 5.0			4.0 5.0		4.0 5.0		ns
t _W (L)	C _{Dn} or S _{Dn} Pulse Width LOW	4.0			4.0		4.0		ns
t _{rec}	Recovery Time \overline{C}_{Dn} or \overline{S}_{Dn} to CP	2.0			2.0		2.0		ns



MC54F138 MC74F138

Advance Information

1-OF-8 DECODER/DEMULTIPLEXER

DESCRIPTION — The MC54F/74F138 is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three F138 devices or to a 1-of-32 decoder using four F138s and one inverter.

DEMULTIPLEXING CAPABILITY

A₂

 $\overline{0}_{7}$

 $\overline{0}_{6}$

2

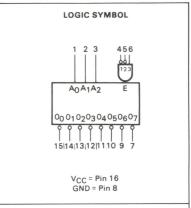
- MULTIPLE INPUT ENABLE FOR EASY EXPANSION
- ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

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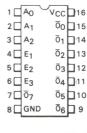
This document contains information on a new product. Specifications and information herein are subject to change without notice.

1-OF-8 DECODER/ DEMULTIPLEXER

FAST™ SCHOTTKY TTL



CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

NOTE

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

MC54F/74F138

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage*	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
lOL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMETED			LIMITS		LINUTC	TEGT	CALDITIONIC		
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CO	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp	ut HIGH Voltage		
VIL	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage			
VIK	Input Clamp Diode Voltag	е			-1.2	V	V _{CC} = MIN, I _{IN} =	-18 mA		
.,	0	54	2.5			V	I _{OH} = -1.0 mA			
VOH	Output HIGH Voltage	74	2.7			V	I _{OH} = -1.0 mA	V _{CC} = MIN		
VOL	Output LOW Voltage				0.5	V	I _{OL} = 20 mA	V _{CC} = MIN		
1	1				20	μΑ	V _{CC} = MAX, V _{IN}	= 2.7 V		
lн	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V			
IIL	Input LOW Current				-0.6	mA	V _{CC} = MAX, V _{IN}	= 0.5 V		
IOS	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V			
lcc	Power Supply Current				20	mA	V _{CC} = MAX			

AC CHARACTERISTICS

-			54/	74F	5	4F	7.	4F	
SYMBOL	PARAMETER	LEVELS OF DELAY	T _A = +25°C V _{CC} = +5.0 V C _I = 50 pF		$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0 \text{ V } \pm 10\%$ $C_L = 50 \text{ pF}$		V _{CC} = 5.	C to 70°C 0 V ± 5% 50 pF	UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
tPLH tPHL	Propagation Delay, Address to Output	3	3.5 4.0	7.0	3.5 4.0	12 9.5	3.5 4.0	8.0 9.0	ns ns
tPLH tPHL	Enable to Output E ₁ or E ₂	2	3.5	7.0	3.5 3.0	11 8.0	3.5	8.0 7.5	ns ns
tPLH tPHL	Enable to Output E3	3	4.0 3.5	8.0 7.5	4.0 3.5	12.5 8.5	4.0 3.5	9.0 8.5	ns ns

NOTES:

^{1.} For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

^{2.} Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION — The decoder accepts three binary weighted inputs (A₀, A₁, A₂) and when enabled provides eight mutually exclusive active LOW outputs $\overline{(O_0-O_7)}$. The F138 features three Enable inputs, two active LOW $(\overline{E_1},\overline{E_2})$ and one active HIGH (E₃). All outputs will be HIGH unless $\overline{E_1}$ and $\overline{E_2}$ are LOW and E₃ is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four F138s and one inverter.

The F138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

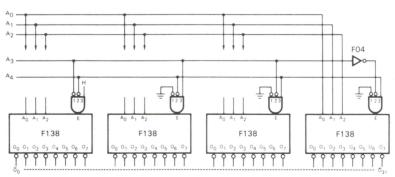
TRUTH TABLE

		INPL	JTS						OUT	PUTS			
Ē ₁	Ē ₂	E3	A ₀	Α1	A ₂	\overline{o}_0	\overline{o}_1	\overline{o}_2	\overline{o}_3	\overline{o}_4	\bar{o}_5	ō ₆	ō ₇
Н	X	X	×	×	×	Н	Н	Н	Н	Н	Н	Н	Н
×	Н	×	×	×	×	н	Н	Н	Н	Н	Н	Н	Н
×	×	L	×	×	×	н	Н	Н	Н	Н	Н	Н	Н
L	L	н	L	L	L	L	Н	н	Н	Н	Н	Н	Н
L	L	н	Н	L	L	н	L	н	Н	Н	Н	Н	Н
L	L	н	L	Н	L	н	Н	L	Н	Н	Н	Н	Н
L	L	н	н	Н	L	н	н	Н	L	Н	Н	Н	Н
L	L	н	L	L	H	н	Н	н	Н	L	Н	Н	Н
L	L	н	н	L	Н	Н	Н	Н	Н	Н	L.	Н	Н
L	L	н	L	Н	Н	н	Н	Н	Н	Н	Н	L	Н
L	L	н	н	Н	Н	н	Н	н	Н	Н	Н	Н	L

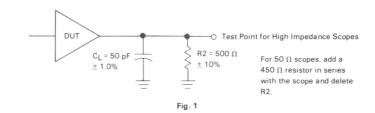
H = HIGH Voltage Level

L = LOW Voltage Level

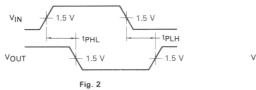
X = Don't Care



AC TEST CIRCUIT



AC WAVEFORMS



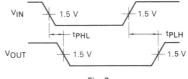


Fig. 3



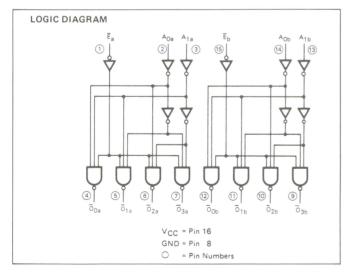
MC54F139 MC74F139

Advance Information

DUAL 1-OF-4 DECODER

DESCRIPTION — The MC54F/74F139 is a high speed Dual 1-of-4 Decoder/Demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW Outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the F139 can be used as a function generator providing all four minterms of two variables.

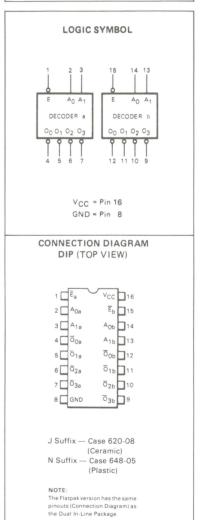
- MULTIFUNCTION CAPABILITY
- TWO COMPLETELY INDEPENDENT 1-OF-4 DECODERS
- ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

DUAL 1-OF-4 DECODER FASTTM SCHOTTKY TTL



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
VCC	Supply Voltage*	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 O	25 25	125 70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMETED			LIMITS		LINUTC	TEST CO	DAIDITIONS	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpu	ut HIGH Voltage	
VIL	Input LOW Voltage				0.8	V	Guaranteed Inpu	ut LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} =	-18 mA	
	0	54	2.5			V	I _{OH} = -1.0 mA		
ΛΟΉ	Output HIGH Voltage	74	2.7			V	I _{OH} = -1.0 mA	V _{CC} = MIN	
VOL	Output LOW Voltage				0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
Lea	Innuit HICH Current				20	μΑ	V _{CC} = MAX, V _{IN} = 2.7 V		
lН	Input HIGH Current	-			0.1	mA	V _{CC} = MAX, V _{IN}	= 7.0 V	
IIL	Input LOW Current				-0.6	mA	V _{CC} = MAX, V _{IN}	= 0.5 V	
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{CC} = MAX, V _O	UT = 0 V	
Icc	Power Supply Current			20	mA	V _{CC} = MAX			

AC CHARACTERISTICS:

		74F		4F	7-		
		+25°C		C to +125°C	T _A = 0°(
SYMBOL PARAMETER	Vcc=	+5.0 V	VCC = 5.0	0 V ±10%	V _{CC} = 5.0 V ± 5% C _L = 50 pF		UNITS
	CL=	50 pF	CL=	50 pF			
	MIN	MAX	MIN	MAX	MIN	MAX	
tPLH Propagation Delay,	3.5	7.0	2.5	9.5	3.0	8.0	ns
tPHL Address to Output	4.0	8.0	3.5	9.5	4.0	9.0	ns
tPLH 5blass Outside	3.5	7.0	3.0	9.0	3.5	8.0	ns
tPHL Enable to Output	3.0	6.5	2.5	8.0	3.0	7.5	ns

NOTES:

^{1.} For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

^{2.} Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION — The F139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0, A_1) and provide four mutually exclusive active LOW outputs $\overline{(0_0-\overline{0}_3)}$. Each decoder has an active LOW Enable (\overline{E}) . When \overline{E} is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application.

Each half of the F139 generates all four miniterms of two variables. These four miniterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

	INPUTS		OUTPUTS					
Ē	A ₀	Α1	\overline{o}_0	\overline{o}_1	\overline{o}_2	\overline{o}_3		
Н	Х	Х	н	н	Н	н		
L	L	L	L	Н	Н	Н		
L	н	L	н	L	Н	Н		
L	L	Н	н	Н	L	Н		
L	н	н	н	Н	Н	L		

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

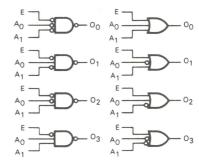
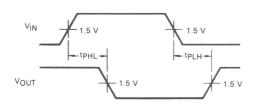


Fig. a

AC WAVEFORMS





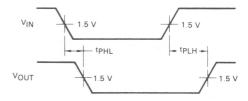


Fig. 2

AC TEST CIRCUIT

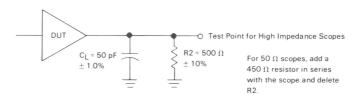


Fig. 3



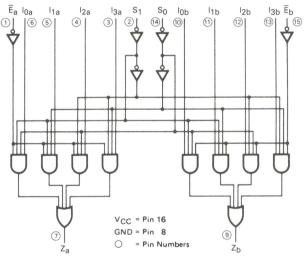
MC54F153 MC74F153

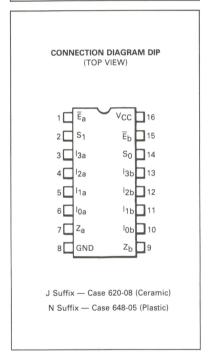
Advance Information

DESCRIPTION — The MC54F/74F153 is a high-speed Dual 4-Input Multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (noninverted) form. In addition to multiplexer operation, the F153 can generate any two functions of three variables.

DUAL 4-INPUT MULTIPLEXER FAST™ SCHOTTKY TTL

LOGIC DIAGRAM





GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
Vcc	Supply Voltage*	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
ТА	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
IOH	Output Current — High	54, 74	_	_	-1.0	mA
lOL	Output Current — Low	54, 74	_	_	20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0°C to 70°C temperature range.

FUNCTIONAL DESCRIPTION

The F153 is a Dual 4-Input Multiplexer. It can select two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1) . The two 4-input multiplexer circuits have individual active LOW Enables $(\overline{E}_a, \overline{E}_b)$ which can be used to strobe the outputs independently. When the Enables $(\overline{E}_a, \overline{E}_b)$ are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW.

The F153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below:

$$\begin{split} Z_{a} &= \overline{E}_{a} \cdot (I_{0a} \cdot \overline{S}_{1} \cdot \overline{S}_{0} + I_{1a} \cdot \overline{S}_{1} \cdot S_{0} + I_{2a} \cdot S_{1} \cdot \overline{S}_{0} + I_{3a} \cdot S_{1} \cdot S_{0}) \\ Z_{b} &= \overline{E}_{b} \cdot (I_{0b} \cdot \overline{S}_{1} \cdot \overline{S}_{0} + I_{1b} \cdot \overline{S}_{1} \cdot S_{0} + I_{2b} \cdot S_{1} \cdot \overline{S}_{0} + I_{3b} \cdot S_{1} \cdot S_{0}) \end{split}$$

The F153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The F153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT	INPUTS		INPUTS (a or b)						
S ₀	s ₁	Ē	10	11	12	13	Z		
X	X	Н	Х	Χ	Χ	X	L		
L	L	L	L	X	X	X	L		
L	L	L	Н	X	X	X	Н		
Н	L	L	X	L	X	X	L		
Н	L	L	X	Н	X	X	Н		
L	Н	L	X	X	L	X	L		
L	Н	L	X	X	Н	X	Н		
Н	Н	L	X	X	X	L	L		
Н	Н	L	Х	Χ	Χ	Н	Н		

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

20 01111111	of the transfer of the state of										
SYMBOL	PARAMETER			LIMITS	3	UNITS	TEST COL	UDITIONS			
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	IEST COI	NDITIONS			
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input I	HIGH Voltage			
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage				
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA, V _{CO}	= MIN			
V	0.44.11(CH.)/-14	54	2.5			V	I _{OL} = -1.0 mA				
VOH	Output HIGH Voltage	74	2.7			V	I _{OL} = -1.0 mA	V _{CC} = MIN			
VOL	Output LOW Voltage				0.5	V	I _{OL} = 20 mA	V _{CC} = MIN			
Less	In the International Contracts				20	μΑ	V _{IN} = 2.7 V, V _{CC} = MAX				
ΙΗ	Input HIGH Current				0.1	mA	$V_{IN} = 7.0 \text{ V, } V_{CC}$	= MAX			
IL	Input LOW Current				-0.6	mA	$V_{IN} = 0.5 \text{ V, } V_{CC}$	= MAX			
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V, V _{CC}	= MAX			
lcc	Power Supply Current				20	mA	V _{IN} = GND, V _{CC} :	= MAX			

NOTES:

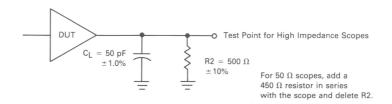
2. Not more than one output should be shorted at a time, nor for more than 1 second.

^{1.} For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device

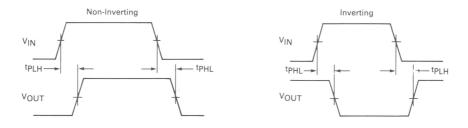
AC CHARACTERISTICS

		54/	74F	54	54F		1F	
		$T_A = +25^{\circ}C$ $V_{CC} = +5.0 \text{ V}$ $C_L = 50 \text{ pF}$		$T_A = -55^{\circ}C$		$T_A = 0^{\circ}C$	UNITS	
SYMBOL	PARAMETER			00	0 V ±10% 50 pF	$V_{CC} = 5.0$ $C_L =$		
		MIN	MAX	MIN	MAX	MIN	MAX	
^t PLH ^t PHL	Propagation Delay S _n to Z _n	5.5 4.0	10.5 9.0	5.0 3.5	14 11	5.5 4.0	12 10.5	ns
^t PLH ^t PHL	Propagation Delay E _n to Z _n	5.0 4.0	9.0 7.0	4.5 3.5	11.5 9.0	5.0 4.0	10.5 8.0	ns
^t PLH ^t PHL	Propagation Delay I _n to Z _n	4.0 3.0	7.0 6.5	3.5 2.5	9.0 8.0	4.0 3.0	8.0 7.5	ns

AC TEST CIRCUIT



PROPAGATION DELAY MEASUREMENTS



NOTES:

- All input waveforms have the following characteristics:
 Low Level = 0 V
 High Level = 3.0 V
 Rise and Fall Times (10% to 90%) = 2.5 ns
- 2. All timing is measured at 1.5 V unless otherwise indicated.

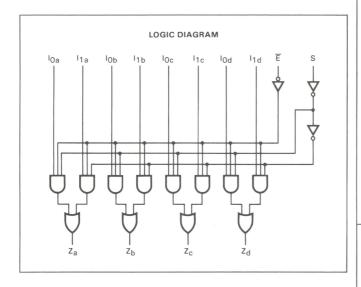


MC54F157 MC74F157

Advance Information

QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The MC54F/74F157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The 'F157 can also be used to generate any four of the 16 different functions to two variables.



TRUTH TABLE

	INP	UTS		OUTPUT
Ē	S	I ₀	l ₁	Z
Н	Х	Х	Х	L
L	Н	X	L	L
L	Н	Х	Н	н
L	L	L	X	L
L	L	Н	Х	н

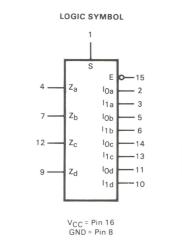
H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

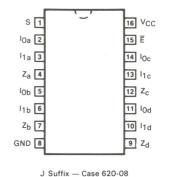
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QUAD 2-INPUT MULTIPLEXER

FAST™ SCHOTTKY TTL



CONNECTION DIAGRAM



(Ceramic)

N Suffix — Case 620-08

(Ceramic)

(Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
	C	54	4.50	5.0	5.50	.,
VCC	Supply Voltage*	74	4.75	5.0	5.25	V
_	O	54	-55	25	125	0.0
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70° C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMETER			LIMITS		LINUTO	TECT OO	IDITIONS
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CON	NUTTIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input	HIGH Voltage
VIL	Input LOW Voltage				0.8	V	Guaranteed Input	LOW Voltage
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN,
1/	0	54	2.5	3.4		V	I _{OH} = -1.0 mA	.,
VOH	Output HIGH Voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	V _{CC} = MIN
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I.e.	Innut IIICH Current				20	μΑ	V _{IN} = 2.7 V	V
lН	Input HIGH Current				100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX
IIL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
Ios	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
Icc	Power Supply Current			15	23	mA	All Inputs = 4.5 V	V _{CC} = MAX

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

			54/74F		5	54F		4F	
		T _A = +25°C			T _A = -55	$T_A = -55 \text{ to } +125^{\circ}\text{C}$		T _A = 0 to +70°C	
SYMBOL	PARAMETER	V	CC = +5.0	V	V _{CC} = 5	$V_{CC} = 5.0 V \pm 10\%$.0 V ±5%	UNITS
			$C_L = 50 pF$		CL=	50 pF	CL=	50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	1
tPLH	Propagation Delay	4.5	10.1	13	3.5	17	4.5	15	
tPHL	S to Z _n	3.5	6.3	8.0	3.5	11.5	3.5	9.0	ns
tPLH	Propagation Delay	5.0	7.6	10	5.0	15	5.0	11.5	
^t PHL	E to Z _n	3.8	5.3	7.0	3.8	8.5	3.8	8.0	ns
tPLH	Propagation Delay	3.8	5.5	7.0	3.5	10	3.8	8.0	
^t PHL	In to Zn	2.5	4.6	5.5	2.5	7.5	2.5	7.0	ns

FUNCTIONAL DESCRIPTION — The F157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input (\overline{E}) is active LOW. When \overline{E} is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The F157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\begin{split} Z_{a} &= \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_{b} = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S}) \\ Z_{c} &= \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_{d} &= \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S}) \end{split}$$

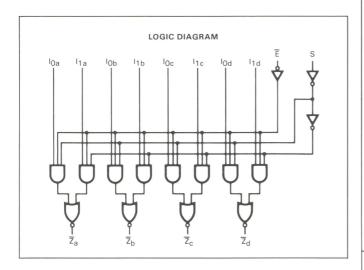
A common use of the F157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The F157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.



Advance Information

QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The MC54F/74F158 is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The 'F158 can also generate any four of the 16 different functions of two variables.



TRUTH TABLE

		_				
	INF	PUTS	;	OUTPUTS		
Ē	S	l ₀	Z			
Н	Х	Х	Х	н		
L	L	L	X	н		
L	L	Н	X	L		
L	Н	Х	L	Н		
L	Н	Х	Н	L		
	_	E S H X L L	E S I0 H X X L L L L H	H X X X X L L X L H X		

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

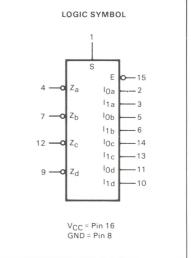
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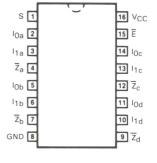
MC54F158 MC74F158

QUAD 2-INPUT MULTIPLEXER

FAST™ SCHOTTKY TTL



CONNECTION DIAGRAM



J Suffix — Case 620-08

(Ceramic)

N Suffix — Case 648-05 (Plastic)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
\/	C	54	4.50	5.0	5.50	.,
VCC	Supply Voltage*	74	4.75	5.0	5.25	V
т.	O	54	-55	25	125	0.0
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ГОН	Output Current — High	54, 74			-1.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAAROL	DADAMETER			LIMITS		LINUTC	TEST OF	ONDITIONS
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CO	ONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Inp	ut HIGH Voltage
VIL	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN,
V	Output HICH Valtage	54	2.5	3.4		V	I _{OH} = -1.0 mA	\/ NAINI
Vон	Output HIGH Voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	V _{CC} = MIN
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
l	Input HIGH Current				20	μΑ	V _{IN} = 2.7 V	Vcc = MAX
ΙΗ	Input high current				100	μΑ	V _{IN} = 7.0 V	ACC - INIXX
IIL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
Icc	Power Supply Current*			10	15	mA	V _{CC} = MAX	

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

			54/74F		5	4F	7	4F	
		T _A = +25°C			$T_A = -55 \text{ to } +125^{\circ}\text{C}$		T _A = 0 to +70°C		
SYMBOL	PARAMETER	V _{CC} = +5.0 V			V _{CC} = 5.	V _{CC} = 5.0 V ±10%		.0 V ±5%	UNITS
		C _L = 50 pF			CL=	50 pF	CL=	50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	4.0	6.4	8.5	4.0	10.5	4.0	9.5	
t _{PHL}	S to Z	4.0	6.9	9.0	4.0	10.5	4.0	10.5	ns
tPLH	Propagation Delay	4.5	6.2	8.0	4.5	9.5	4.5	9.0	
tPHL	E to Zn	3.5	6.4	8.5	3.5	9.5	3.5	9.5	ns
tPLH	Propagation Delay	3.0	4.4	5.9	2.5	8.5	3.0	7.0	
t _{PHL}	In to Z	2.0	3.3	4.5	2.0	6.0	2.0	5.5	ns

 $^{^{*}\}text{I}_{\mbox{\footnotesize{CC}}}$ measured with outputs open and 4.5 V applied to all inputs.

FUNCTIONAL DESCRIPTION — The F158 quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input (\overline{E}) is active LOW. When \overline{E} is HIGH, all of the outputs (\overline{Z}) are forced HIGH regardless of all other inputs. The F158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

A common use of the F158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The F158 can generate four functions of two variables with one variable n common. This is useful for implementing gating functions.



Advance Information

QUAD D FLIP-FLOP

DESCRIPTION — The MC54F/74F175 is a high-speed quad D flipflop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs when LOW.

- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED POSITIVE EDGE-TRIGGERED CLOCK
- ASYNCHRONOUS COMMON RESET
- TRUE AND COMPLEMENT OUTPUT

FUNCTIONAL DESCRIPTION — The F175 consists of four edgetriggered D flip-flops with individual D inputs and Q and Q outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and Q outputs to follow. A LOW input on the Master Reset (MR) will force all Q outputs LOW and Q outputs HIGH independent of Clock or Data inputs. The F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

INPUTS	OUT	PUTS
@ t _n , MR = H	@ 1	in + 1
Dn	Qn	Qn
L	L	Н
Н	Н	L

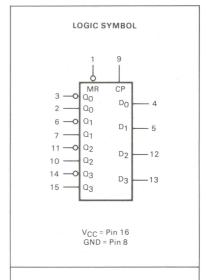
 t_{Π} = Bit time before clock positive-going transition $t_{\Pi}+1$ = Bit time after clock positive-going transition H = HIGH Voltage Level L = LOW Voltage Level

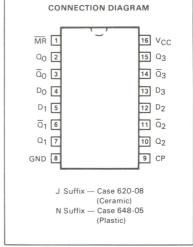
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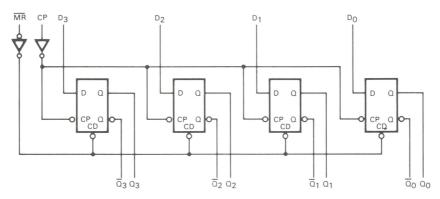
MC54F175 MC74F175

QUAD D FLIP-FLOP
FAST™ SCHOTTKY TTL





LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT			
1/	C	54	4.50	5.0	5.50				
VCC	Supply Voltage*	74	4.75	5.0	5.25	\ \			
_	0 4	54	-55	25	125	°C			
ТД	Operating Ambient Temperature Range	74	0	25	70				
ІОН	Output Current — High	54, 74			-1.0	mA			
loL	Output Current — Low	54, 74			20	mA			

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

OVA A D O I	DARAMETER			LIMITS		LINUTO	TEOT 00	NIDITIONIO		
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CO	NDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpu	Guaranteed Input HIGH Voltage		
VIL	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage			
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN		
V _{OH}	0	54	2.5	3.4		V	I _{OH} = -1.0 mA			
	Output HIGH Voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	V _{CC} = MIN		
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN		
Line	1				20	μΑ	V _{IN} = 2.7 V	V _{CC} = MAX		
lН	Input HIGH Current				100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX		
IIL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX		
los	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX			
ICC	Power Supply Current			22.5	34	mA	D _n = MR = 4.5 V CP =	V _{CC} = Max		

NOTES:

- For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

			54/74F		5-	4F	7	4F	
		1	A = +25°	С	T _A = -55	to +125°C	$T_A = 0 t$	o +70°C	
SYMBOL	PARAMETER	V	CC = +5.0	V	V _{CC} = 5.	0 V ±10%	V _{CC} = 5.	0 V ±5%	UNITS
			$C_L = 50 p$	F	CL =	50 pF	C _L =		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}	Maximum Clock Frequency	100	140		100		100		MHz
tPLH	Propagation Delay	4.0	5.0	6.5	3.5	8.5	4.0	7.5	
tPHL	CP to Q_n or \overline{Q}_n	4.0	6.5	8.5	4.0	10.5	4.0	9.5	ns
tPHL	Propagation Delay MR to Qn	4.5	9.0	11.5	4.5	15	4.5	13	ns
tPLH	$\frac{\text{Propagation Delay}}{\text{MR to }\overline{\Omega}_{\text{N}}}$	4.0	6.5	8.0	4.0	10	4.0	9.0	ns

AC OPERATING REQUIREMENTS

			54/74F		5	4F	74	4F	
SVAIDOL	PARAMETER		T _A = +25°			to +125°C	T _A = 0 t		UNITS
SYMBOL	PARAMETER	V	CC = +5.0	V	V _{CC} = 5.0	V _{CC} = 5.0 V ±10%		$V_{CC} = 5.0 V \pm 5\%$	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _s (H)	Set up Time, HIGH or LOW	3.0			3.0		3.0		
t _S (L)	D _n to CP	3.0			3.0		3.0		ns
th (H)	Hold Time, HIGH or LOW	1.0			1.0		1.0		113
th (L)	D _n to CP	1.0			1.0		1.0		
t _W (H)	CP Pulse Width, HIGH	4.0			4.0		4.0		
$t_{W}(L)$	or LOW	5.0			5.0		5.0		ns
t _W (L)	MR Pulse Width LOW	5.0			5.0		5.0		ns
t _{rec}	Recovery Time MR to CP	5.0			5.0		5.0		ns



MC54F181 MC74F181

Advance Information

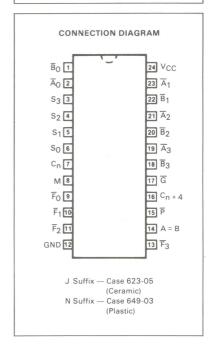
4-BIT ARITHMETIC LOGIC UNIT

DESCRIPTION — The MC54F/74F181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

- PROVIDES 16 ARITHMETIC OPERATIONS ADD, SUBTRACT, COMPARE, DOUBLE, PLUS TWELVE OTHER ARITHMETIC OPERATIONS
- PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES EXCLUSIVE-OR, COMPARE, AND, NAND, OR, NOR, PLUS TEN OTHER LOGIC OPERATIONS
- FULL LOOKAHEAD FOR HIGH-SPEED ARITHMETIC OPERA-TION ON LONG WORDS
- 600 OR 300 MIL WIDE DIP PACKAGES

4-BIT ARITHMETIC LOGIC UNIT

FAST™ SCHOTTKY TTL



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT		
		54	4.50	5.0	5.50	.,		
VCC	Supply Voltage*	74	4.75	5.0	5.25	V		
-	0 11:	54	-55	25	125	0.0		
TA	Operating Ambient Temperature Range	74	0	25	70	°C		
ГОН	Output Current — High	54, 74			-1.0	mA		
Vон	Output Voltage — High A = B output	54, 74			5.5	V		
loL	Output Current — Low	54, 74			20	mA		

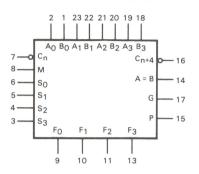
^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

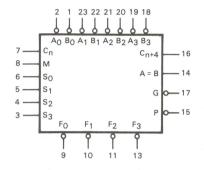
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LOGIC SYMBOLS

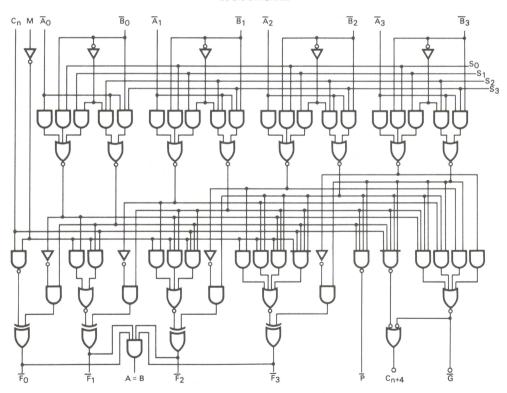
ACTIVE-HIGH OPERANDS





LOGIC DIAGRAM

V_{CC} = Pin 24 GND = Pin 12



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

01/14001	DADAM	-T.C.D			LIMITS		LINUTC	TECT CO	DAIDITIONE	
SYMBOL	PARAME	IER		MIN	TYP	MAX	UNITS	TEST CO	ONDITIONS	
VIH	Input HIGH Voltage			2.0			V	Guaranteed Input HIGH Voltage		
VIL	Input LOW Voltage					0.8	V	Guaranteed Input LOW Voltage		
VIK	Input Clamp Diode V	/oltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
ІОН	Output Current — H			250	μА	V _{OH} = 5.5 V	V _{CC} = MIN, A=B			
VOH	Output HIGH Voltage 54 74			2.5	3.4		V	I _{OH} = -1.0 mA	V _{CC} = MIN	
				2.7	3.4		V	I _{OH} = -1.0 mA		
VOL	Output LOW Voltage	е			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
lu.	Innut HICH Current			20	μΑ	V _{IN} = 2.7 V	V _{CC} = MAX			
lН	Input HIGH Current			100	μΑ	V _{IN} = 7.0 V				
		M Input				-0.6	mA			
lo.	Input LOW Current	A and B	Inputs			-1.8	mA	V _{IN} = 0.5 V	V _{CC} = MAX	
IΙL	Imput LOVV Current	S ₀₋₃ In	puts			-2.4	mA	VIIV - 0.5 V	VCC - MAX	
		C _n Inpu	t			-3.0	mA			
Ios	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX			
Icc	Power Supply Curre	nt			43	65	mA	V _{CC} = MAX		
						-	-			

NOTES

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION — The F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S0–S3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active-HIGH or active—LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the $C_{\Pi}+4$ output, or for carry lookahead between packages using the signals \overline{P} (Carry Propagate) and \overline{G} (Carry Generate). In the Add mode, \overline{P} indicates that \overline{F} is 15 or more, while \overline{G} indicates that \overline{F} is less than zero. \overline{P} and \overline{G} are not affected by carry in. When speed requirements are not stringent, it can be used in a simple Ripple Carry mode by connecting the Carry output ($C_{\Pi}+4$) signal to the Carry input (C_{Π}) of the next unit. For high-speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead car be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four \overline{F} outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active-LOW inputs producing active-LOW outputs or with active-HIGH inputs producing active-HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

AC CHARACTERISTICS

				54/74F		5	4F	7.	4F	
SYMBOL	PARAMET	ER	V	TA = +25°(CC = +5.0 CL = 50 pF	V	T _A = -55 V _{CC} = 5.	to +125°C 0 V ±10% 50 pF	T _A = 0 t V _{CC} = 5	o +70°C .0 V ±5% 50 pF	UNITS
	PATH	MODE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH tPHL	C _n to C _{n + 4}		3.0 3.0	6.4 6.1	8.5 8.0	3.0 3.0	12 11.5	3.0 3.0	9.5 9.0	ns
^t PLH ^t PHL	\overline{A} or \overline{B} to C_{n+4}	Sum	5.0 5.0	10 9.4	13 12	5.0 5.0	18 17	5.0 5.0	14 13	ns
tPLH tPHL	\overline{A} or \overline{B} to C_{n+4}	Dif	5.0 5.0	10.8 10	14 13	5.0 5.0	19.5 18	5.0 5.0	15 14	ns
tPLH tPHL	C _n to F	Any	3.0 3.0	6.7 6.5	8.5 8.5	3.0 3.0	12 12	3.0 3.0	9.5 9.5	ns
tPLH tPHL	\overline{A} or \overline{B} to \overline{G}	Sum	3.0 3.0	5.7 5.8	7.5 7.5	3.0 3.0	10.5 10.5	3.0 3.0	8.5 8.5	ns
tPLH tPHL	\overline{A} or \overline{B} to \overline{G}	Dif	3.0 3.0	6.5 7.3	8.5 9.5	3.0 3.0	12 13.5	3.0 3.0	9.5 10.5	ns
tPLH tPHL	Ā or B to P	Sum	3.0 3.0	5.0 5.5	7.0 7.5	3.0 3.0	10 10.5	3.0 3.0	8.0 8.5	ns
tPLH tPHL	\overline{A} or \overline{B} to \overline{P}	Dif	4.0 4.0	5.8 6.5	7.5 8.5	4.0 4.0	10.5 12	4.0 4.0	8.5 9.5	ns
tPLH tPHL	\overline{A}_i or \overline{B}_i to \overline{F}_i	Sum	3.0 3.0	7.0 7.2	9.0 10	3.0 3.0	12.5 14	3.0 3.0	10 10	ns
tPLH tPHL	\overline{A}_i or \overline{B}_i to \overline{F}_i	Dif	3.0 3.0	8.2 5.0	11 11	3.0 3.0	15.5 15.5	3.0 3.0	12 12	ns
tPLH tPHL	Any \overline{A} or \overline{B} to Any \overline{F}	Sum	4.0 4.0	8.0 7.8	10.5 10	4.0 4.0	15.5 14	4.0 4.0	11.5 11	ns
^t PLH ^t PHL	Any \overline{A} or \overline{B} to Any \overline{F}	Dif	4.5 4.5	9.4 9.4	12 12	4.5 4.5	17 17	4.5 4.5	13 13	ns
tPLH tPHL	Ā or B to F	Logic	4.0 4.0	6.0 6.0	9.0 10	4.0 4.0	12.5 14	4.0 4.0	10 11	ns
tPLH tPHL	\overline{A} or \overline{B} to $A = B$	Dif	11 7.0	18.5 9.8	27 12.5	11 7.0	35 17.5	11 7.0	29 13.5	ns

FUNCTION TABLE

М		SELE			/E-LOW OPERANDS & Fn OUTPUTS	ACTIVE-HIGH OPERANDS & Fn OUTPUTS			
S ₃	S ₂	S ₁	S ₀	LOGIC (M = H)	ARITHMETIC** (M = L) (Cn = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C _n = H)		
L L L	L L L	LHH	LHLH	Ā ĀB Ā + B Logic 1	A minus 1 AB minus 1 AB minus 1 minus 1	Ā A + B ĀB Logic 0	A A + B A + B minus 1		
L L L	1111	LHH	LHLH	A + B B A + B A + B	A plus $(A + \overline{B})$ AB plus $(A + \overline{B})$ A minus B minus 1 $A + \overline{B}$	AB B A (+) B AB	A plus $A\overline{B}$ $(A + B)$ plus $A\overline{B}$ A minus B minus 1 $A\overline{B}$ minus 1		
TITI	L L L	LHH	L H L	ĀB A (+) B B A + B	A plus (A + B) A plus B AB plus (A + B) A + B	A + B B AB	A plus AB A plus B (A + B) plus AB AB minus 1		
HHH	1111	L H H	L H L	Logic 0 AB AB A	A plus A* AB plus A AB minus A A	Logic 1 A + B A + B A	A plus A* (A + B) plus A (A + B) plus A A minus 1		

^{*}Each bit is shifted to the next more significant position. H = HIGH Voltage Level **Arithmetic operations expressed in 2s complement notation. L = LOW Voltage Level



Advance Information

CARRY LOOKAHEAD GENERATOR

DESCRIPTION — The MC54F/74F182 is a high-speed carry lookahead generator. It is generally used with the F181, F381 or 29F01 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

- PROVIDES LOOKAHEAD CARRIES ACROSS A GROUP OF FOUR ALUS
- MULTI-LEVEL LOOKAHEAD HIGH-SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS

TRUTH TABLE

			IN	IPUT	S					OU	TPUT	3	
Cn	Ğ₀	P ₀	₫1	₽ ₁	Ğ₂	\overline{P}_2	G ₃	₽ ₃	C _{n+x}	C _{n+y}	C _{n+z}	G	P
X L X H	H L X	H X X L							LHH				
X X X X H	X H X L X	X H X X L	HHHLXX	H X X L L									
XXXLXXXH	X H H X X L	X X X X X X L	X H H X L X	X H X X X L L	H H H L X X X	H X X X L L							
	X X H X X X L		X H H X X L	X X X X X X L	X H H X L X	X H X X X L L	H H H L X X	H X X X L L				H H H L L L L	
		H X X L		X X X L		X X H X L		X X H L					HHHL

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

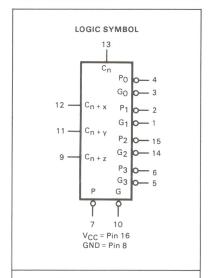
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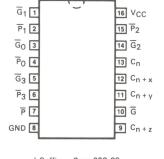
MC54F182 MC74F182

CARRY LOOKAHEAD GENERATOR

FAST™ SCHOTTKY TTL

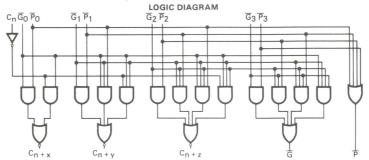


CONNECTION DIAGRAM



J Suffix — Case 620-08

(Ceramic)
N Suffix — Case 648-05
(Plastic)



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	
	0 1 1/1 *	54	4.50	5.0	5.50	V	
V _{CC} Supply Voltage*	Supply Voltage*	74	4.75	5.0	5.25		
т.	O	54	-55	25	125	0.0	
TA	Operating Ambient Temperature Range	74	0	25	70	°C	
ГОН	Output Current — High	54, 74			-1.0	mA	
loL	Output Current — Low	54, 74			20	mA	

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMADO	-	ADAMETER			LIMITS		UNITS	TECT CO	NDITIONS
YMBOL	P	ARAMETER		MIN	TYP	MAX	UNITS	TEST CO	NDITIONS
VIH	Input HIGH V	oltage/		2.0			V	Guaranteed Inpu	t HIGH Voltage
VIL	Input LOW V	oltage				0.8	V	Guaranteed Inpu	t LOW Voltage
VIK	Input Clamp	Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
		Output HIGH Voltage 74		2.5	3.4		V	I _{OH} = -1.0 mA	.,
Vон	Output HIGH			2.7	3.4		V	I _{OH} = -1.0 mA	VCC = MIN
VOL	Output LOW	Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
l	Input HIGH Current					20	μΑ	V _{IN} = 2.7 V	V _{CC} = MAX
ΙН	Input nigh C	urrent			100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX	
		C _n Input				-1.2			
	Input LOW Current	P ₃ Input				-2.4			
IIL		\overline{P}_2 Input \overline{G}_3 , \overline{P}_0 , \overline{P}_1 Inputs \overline{G}_0 , \overline{G}_2 Inputs				-3.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
'IL						-4.8		7114 5.5 7	VCC IVIVOX
						-8.4			
	G ₁ Input					-9.6	1		
los	Output Short Current (Note			-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
Іссн	Power Supply Current (All Outputs HIGH)				18.4	28	mA	\overline{P}_3 , $\overline{G}_3 = 4.5 \text{ V}$ All Other Inputs = GND	V _{CC} = MAX
ICCL	Power Supply Current (All Outputs LOW)			23.5	36	mA	GO, G1, G2 = 4.5 V All Other Inputs = GND	V _{CC} = MAX	

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

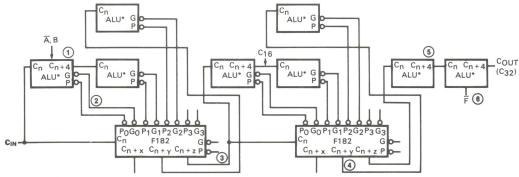
			54/74F		54	4F	74	4F	
SYMBOL	PARAMETER	V	Γ _A = +25°(CC = +5.0 C _L = 50 pF	V	V _{CC} = 5.0	T _A = -55 to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0 to +70°C V _{CC} = 5.0 V ±5% C _L = 50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH tPHL	Propagation Delay C_n to C_{n+x} , C_{n+y} , C_{n+z}	3.0 3.0	6.6 6.8	8.5 9.0	3.0 3.0	10.5 11	3.0 3.0	9.5 10	ns
tPLH tPHL	Propagation Delay \overline{P}_0 , \overline{P}_1 or \overline{P}_2 to C_{n+x} , C_{n+y} , C_{n+z}	2.5 2.0	6.2 3.7	8.0 5.0	2.5 2.0	10.7 6.5	2.5 2.0	9.0 6.0	ns
tPLH tPHL	Propagation Delay \overline{G}_0 , \overline{G}_1 or \overline{G}_2 to C_{n+x} , C_{n+y} , C_{n+z}	2.5 2.0	6.5 3.9	8.5 5.2	2.5 2.0	10.5 6.5	2.5 2.0	9.5 6.0	ns
tPLH tPHL	Propagation Delay P ₁ , P ₂ or P ₃ to G	3.0 3.0	7.9 6.0	10 8.0	3.0 3.0	12.5 9.5	3.0 3.0	11 9.0	ns
tPLH tPHL	Propagation Delay \overline{G}_{n} to \overline{G}	3.0 3.0	8.3 5.7	10.5 7.5	3.0 3.0	12.5 9.5	3.0 3.0	11.5 8.5	ns
^t PLH ^t PHL	Propagation Delay Pn to P	3.0 2.5	5.7 4.1	7.5 5.5	3.0 2.5	11 7.5	3.0 2.5	8.5 6.5	ns

 $FUNCTIONAL\ DESCRIPTION — The F182\ carry\ lookahead\ generator\ accepts\ up\ to\ four\ pairs\ of\ active-LOW\ Carry\ Propagate\ ($\overline{P}_0-\overline{P}_3$)\ and\ Carry\ Generate\ ($\overline{G}_0-\overline{G}_3$)\ signals\ and\ an\ active-HIGH\ Carry\ input\ (C_n)\ and\ provides\ anticipated\ active-HIGH\ carries\ (C_n+_x,\ C_n+_y,\ C_n+_z)\ across\ four\ groups\ of\ binary\ adders.$ The F182\ also\ has\ active-LOW\ Carry\ Propagate\ (\$\overline{P}\$)\ and\ Carry\ Generate\ (\$\overline{G}\$)\ outputs\ which\ may\ be\ used\ for\ further\ levels\ of\ lookahead\ . The\ logic\ equations\ provided\ at\ the\ output\ are:

$$\begin{array}{ll} C_{n+x} = G_0 + P_0 C_n & \overline{G} = \underline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0} \\ C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n & P = \overline{P_3 P_2 P_1 P_0} \\ C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n & \end{array}$$

Also, the F182 can be used with binary ALUs in an active-LOW or active-HIGH input operand mode. The connections (Figure A) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last F181 or F381.

FIGURE A - 32-Bit ALU with Ripple Carry between 16-Bit Lookahead ALUs



*ALUs may be either F181, F381 or 2901A.



UP/DOWN DECADE COUNTER (With Preset and Ripple Clock)

DESCRIPTION — The MC54F/74F190 is a reversible BCD (8421) decade counter featuring synchronous counting and asynchronous presetting. The preset feature allows the F190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- HIGH-SPEED 110 MHz TYPICAL COUNT FREQUENCY
- SYNCHRONOUS COUNTING
- ASYNCHRONOUS PARALLEL LOAD
- CASCADABLE

RC TRUTH TABLE

		INPUT	s	OUTPUT
	CE	TC*	СР	RC
	L	Н	ъ	T.
ı	Н	X	X	Н
	Х	L	Х	Н

*TC is generated internally

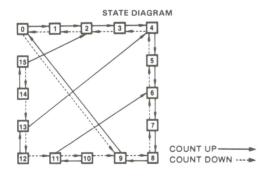
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

MODE SELECT TABLE

	INP	UTS		MODE
PL	PL CE U/D CP		СР	
HHLI	LXH	L X X	x x L	Count Up Count Down Preset (Asyn.) No Change (Hold)



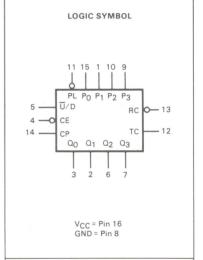
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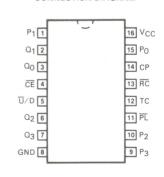
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MC54F190 MC74F190

UP/DOWN DECADE COUNTER
(With Preset and Ripple Clock)

FAST™ SCHOTTKY TTL

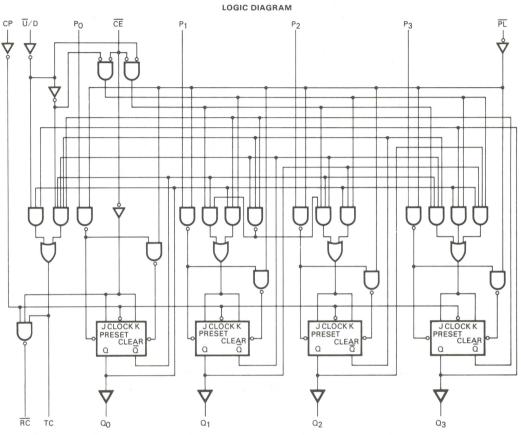




CONNECTION DIAGRAM

J Suffix — Case 620-08 (Ceramic)

N Suffix — Case 648-05 (Plastic)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

PARAMETER		MIN	TYP	MAX	UNIT	
2 1 1/1 *	54	4.50	5.0	5.50		
Supply Voltage*	74	4.75	5.0	5.25	V	
G A T	54	-55	25	125	0.0	
Operating Ambient Temperature Range	74	0	25	70	°C	
Output Current — High	54, 74			-1.0	mA	
Output Current — Low	54, 74			20	mA	
	Supply Voltage* Operating Ambient Temperature Range Output Current — High	Supply Voltage* 54 74 74 Operating Ambient Temperature Range 54 Output Current — High 54, 74	Supply Voltage* 54 4.50 74 4.75 Operating Ambient Temperature Range 54 -55 74 0 Output Current — High 54, 74	Supply Voltage* 54 4.50 5.0 74 4.75 5.0 Operating Ambient Temperature Range 54 -55 25 74 0 25 Output Current — High 54, 74 -74	Supply Voltage* 54 4.50 5.0 5.50 74 4.75 5.0 5.25 Operating Ambient Temperature Range 54 -55 25 125 74 0 25 70 Output Current — High 54, 74 -1.0	

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

FUNCTIONAL DESCRIPTION — The F190 is a synchronous up/down BCD decade counter containing four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations. It has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (\overline{PL}) input is LOW, information present on the Parallel Data inputs (PO-P3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table. A HIGH signal on the \overline{CE} input inhibits counting. When \overline{CE} is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the \overline{U}/D input signal, as indicated in the Mode Select Table. \overline{CE} and \overline{U}/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 9 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until \overline{U}/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is also used internally to enable the Ripple Clock (\overline{RC}) output. The \overline{RC} output is normally HIGH. When \overline{CE} is LOW and TC is HIGH, the \overline{RC} output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters. For a discussion and illustrations of the various methods of implementing multistage counters, please see the F191 data sheet.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

				LIMITS						
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CO	ONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp	ut HIGH Voltage		
VIL	Input LOW Voltage				0.8	V	Guaranteed Inp	Guaranteed Input LOW Voltage		
VIK	Input Clamp Diode Voltage			~	-1.2	V	I _{IN} = -18 mA V _{CC} = MIN			
Vон	Output HIGH Voltage	54	2.5	3.4		V	I _{OH} = -1.0 mA			
		74	2.7	3.4		V	I _{OH} = -1.0 mA	VCC = MIN		
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN		
loca	Input HIGH Current				20	μΑ	V _{IN} = 2.7 V	V _{CC} = MAX		
ΊΗ	input high current				100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX		
ΙΙL	Input LOW Current Other Inputs				-0.6	mA	V _{IN} = 0.5 V	\/ NAAY		
	CE Input				-1.8	MA	VIN - 0.5 V	VCC = MAX		
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX		
Icc	Power Supply Current			38	55	mA	V _{CC} = MAX			

NOTES

- For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

			54/74F		_	4F				
			Γ _A = +25°			to +125°C				
SYMBOL	PARAMETER		CC = +5.0		V _{CC} = 5.0 V ±10%		$V_{CC} = 5.0 V \pm 5\%$		UNITS	
			CL = 50 pl		CL=	C _L = 50 pF		50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
fmax	Maximum Count Frequency	80	110		80		80		MHz	
tPLH	Propagation Delay	3.0	5.5	9.0	3.0	12.5	3.0	10		
t _{PHL}	CP to Q _n	3.0	6.5	10	3.0	14	3.0	11	ns	
tPLH	Propagation Delay	8.0	12.5	16	8.0	22.5	8.0	17	17	
tPHL	CP to TC	5.0	9.5	13	5.0	18	5.0	14	ns	
tPLH	Propagation Delay	4.0	7.0	9.5	4.0	13.5	4.0	10.5		
^t PHL	CP to RC	3.0	5.0	8.0	3.0	11	3.0	9.0	ns	
tPLH	Propagation Delay	3.0	4.6	7.0	3.0	10	3.0	8.0		
^t PHL	CE to RC	3.0	4.5	7.0	3.0	10	3.0	8.0	ns	
tPLH	Propagation Delay	7.0	11	18	7.0	25.5	7.0	19		
^t PHL	Ū/D to RC	5.0	9.0	12	5.0	17	5.0	13	ns	
tPLH	Propagation Delay	3.0	6.0	11	3.0	15.5	3.0	12	20	
^t PHL	Ū∕D to TC	3.0	6.5	11	3.0	15.5	3.0	12	ns	
tPLH	Propagation Delay	3.0	4.6	7.0	3.0	10	3.0	8.0	nc	
tPHL	P _n to Q _n	8.0	13.4	17	8.0	24	8.0	18	ns	
tPLH	Propagation Delay	3.0	6.7	11	3.0	15.5	3.0	12	nc	
t _{PHL}	PL to Ω _n	4.0	7.2	15	4.0	21	4.0	16	ns	

AC OPERATING REQUIREMENTS

			54/74F		5	4F	74	1F	UNITS	
SYMBOL	PARAMETER		TA = +25°			to +125°C				
OTHEOL	TANAMETER.	V	CC = +5.0	V	V _{CC} = 5	$V_{CC} = 5.0 V \pm 10\%$		$V_{CC} = 5.0 V \pm 5\%$		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _S (H)	Set up Time, HIGH or LOW	5.0			5.0		5.0			
t _S (L)	P _n to PL	8.0			8.0		8.0		ns	
t _h (H)	Hold Time, HIGH or LOW	3.0			3.0		3.0			
th (L)	P _n to PL	3.0			3.0		3.0			
t _S (L)	Set up Time LOW CE to CP	10			10		10		ns	
t _h (L)	Hold Time LOW CE to CP	0			0		0		IIS	
t _W (L)	PL Pulse Width, LOW	6.0			6.0		6.0		ns	
t _W (L)	CP Pulse Width LOW	6.0			6.0		6.0		ns	
trec	Recovery Time PL to CP	7.0			7.0		7.0		ns	



UP/DOWN BINARY COUNTER (With Preset and Ripple Clock)

DESCRIPTION — The MC54F/74F191 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous presetting. The preset feature allows the F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- HIGH-SPEED 110 MHz TYPICAL COUNT FREQUENCY
- SYNCHRONOUS COUNTING
- ASYNCHRONOUS PARALLEL LOAD
- CASCADABLE

FUNCTIONAL DESCRIPTION — The F191 is a synchronous up/down 4-bit binary counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load $(\overline{\text{PL}})$ input is LOW, information present on the Parallel Data inputs (P_0-P_3) is loaded into the counter and appears on the Ω outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{\text{CE}}$ input inhibits counting. When $\overline{\text{CE}}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{\text{U}}/\text{D}$ input signal, as indicated in the Mode Select Table $\overline{\text{CE}}$ and $\overline{\text{U}}/\text{D}$ can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

MODE SELECT TABLE

	INP	UTS		MODE
PL	CE	Ū/D	СР	052
HHHH	L X H	L H X	х×ч	Count Up Count Down Preset (Asyn.) No Change (Hold)

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

RC TRUTH TABLE

- 11	NPUT	S	OUTPUT
CE	TC*	СР	RC
L	Н	ъ	T
Н	X	X	Н
X	L	Н	

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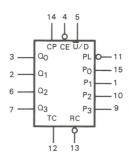
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC54F191 MC74F191

UP/DOWN BINARY COUNTER (With Preset and Ripple Clock)

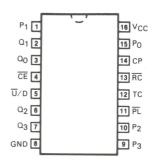
FAST™ SCHOTTKY TTL





V_{CC} = Pin 16 GND = Pin 8

CONNECTION DIAGRAM



J Suffix — Case 620-08 (Ceramic)

N Suffix — Case 648-05 (Plastic)

FUNCTIONAL DESCRIPTION (continued)

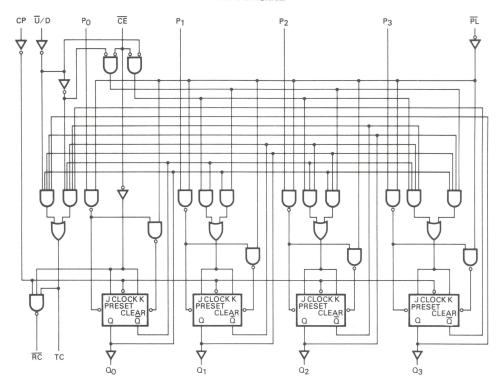
Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 15 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until \overline{U}/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock (\overline{RC}) output. The \overline{RC} output is normally HIGH. When \overline{CE} is LOW and TC is HIGH, the \overline{RC} output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures A and B. In Figure A, each \overline{RC} output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on \overline{CE} inhibits the \overline{RC} output pulse, as indicated in the \overline{RC} Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure B. All clock inputs are driven in parallel and the \overline{RC} outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the \overline{RC} output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure C avoids ripple delays and their associated restrictions. The $\overline{\text{CE}}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures A and B doesn't apply, because the TC output of a given stage is not affected by its own $\overline{\text{CE}}$.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	
V/	C	54	4.50	5.0	5.50		
V _{CC} Su	Supply Voltage*	74	4.75	5.0	5.25	V	
T _A O	0	54	-55	25	125		
	Operating Ambient Temperature Range	74	0	25	70	°C	
ІОН	Output Current — High	54, 74			-1.0	mA	
lOL	Output Current — Low	54, 74			20	mA	

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

FIGURE A - N-Stage Counter Using Ripple Clock

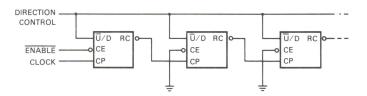


FIGURE B — Synchronous N-Stage Counter Using Ripple Carry/Borrow

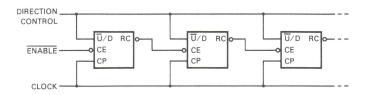
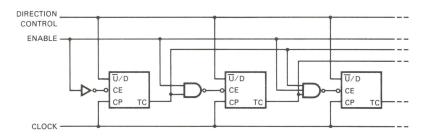


FIGURE C — Synchronous N-Stage Counter with Parallel Gated Carry/Borrow



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

01/14001	BARAMETER			LIMITS		LINUTO	Guaranteed Inp $I_{IN} = -18 \text{ mA}$ $I_{OH} = -1.0 \text{ mA}$ $I_{OH} = -1.0 \text{ mA}$ $I_{OL} = 20 \text{ mA}$	DAIDITIONS	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CO	CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpo	ut HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage I _{IN} = -18 mA		
VIK	Input Clamp Diode Voltage	9			-1.2	V			
	0	54	2.5	3.4		V	I _{OH} = -1.0 mA)/	
VOH	Output HIGH Voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	VCC = MIN	
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
lu.	Innut HICH Current				20	μΑ	V _{IN} = 2.7 V	\/a== 844\	
ΙΗ	Input HIGH Current				100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX	
IIL	Input LOW Current Other Inputs				-0.6	mA	V _{IN} = 0.5 V	Vcc = MAX	
	CE Input				-1.8	mA	VIN - 0.5 V	ACC - INIXX	
Ios	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX	
Icc	Power Supply Current			38	55	mA	V _{CC} = MAX		

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

			54/74F			4F		4F	
			TA = +25°(to +125°C		to +70°C	
SYMBOL	PARAMETER		CC = +5.0			0 V ±10%	$V_{CC} = 5.0 V \pm 5\%$		UNITS
			$C_L = 50 pF$		CL=	50 pF	CL=	50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax	Maximum Count Frequency	80	110		80	2 - 1	80		MHz
tPLH	Propagation Delay	3.0	5.5	9.0	3.0	12.5	3.0	10	
tPHL	CP to Qn	3.0	6.5	10	3.0	14	3.0	11	ns
tPLH	Propagation Delay	8.0	12.5	16	8.0	22.5	8.0	17	
tPHL	CP to TC	5.0	9.5	13	5.0	18	5.0	14	ns
tPLH	Propagation Delay	4.0	7.0	9.5	4.0	13.5	4.0	10.5	
tPHL	CP to RC	3.0	5.0	8.0	3.0	11	3.0	9.0	ns
tPLH	Propagation Delay	3.0	4.6	7.0	3.0	10	3.0	8.0	
^t PHL	CE to RC	3.0	4.5	7.0	3.0	10	3.0	8.0	ns
tPLH	Propagation Delay	7.0	11	18	7.0	25.5	7.0	19	
tPHL.	Ū∕D to RC	5.0	9.0	12	5.0	17	5.0	13	ns
tPLH	Propagation Delay	3.0	6.0	11	3.0	15.5	3.0	12	
^t PHL	Ū∕D to TC	3.0	6.5	11	3.0	15.5	3.0	12	ns
tPLH	Propagation Delay	3.0	4.6	7.0	3.0	10	3.0	8.0	
^t PHL	P _n to Q _n	8.0	13.4	17	8.0	24	8.0	18	ns
tPLH	Propagation Delay	3.0	6.7	11	3.0	15.5	3.0	12	
^t PHL	PL to Q _n	4.0	7.2	15	4.0	21	4.0	16	ns

AC OPERATING REQUIREMENTS

			54/74F		5-	4F	7	4F	
SYMBOL	PARAMETER	T _A = +25°C V _{CC} = +5.0 V			$T_A = -55 \text{ to } +125^{\circ}\text{C}$ $V_{CC} = 5.0 \text{ V} \pm 10\%$				UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _S (H) t _S (L)	Set up Time, HIGH or LOW Pn to PL	5.0 8.0	*.		5.0 8.0	-2 -2, .	5.0 8.0		ns
th (H) th (L)	Hold Time, HIGH or LOW Pn to PL	3.0 3.0			3.0	,	3.0 3.0		113
t _S (L)	Set up Time LOW CE to CP	10			10		10		ns
th (L)	Hold Time LOW CE to CP	0			0		0		110
t _W (L)	PL Pulse Width, LOW	6.0			6.0		6.0		ns
t _W (L)	CP Pulse Width LOW	6.0			6.0		6.0		ns
t _{rec}	Recovery Time PL to CP	7.0			7.0		7.0		ns



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

DESCRIPTION — The MC54F/74F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The F194 is similar in operation to the S195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

- TYPICAL SHIFT FREQUENCY OF 150 MHz
- ASYNCHRONOUS MASTER RESET
- HOLD (DO NOTHING) MODE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS

FUNCTIONAL DESCRIPTION — The F194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S0, S1) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data (P0-P3) and Serial data (DSR, DSL) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset $(\overline{\rm MR})$ overrides all other inputs and forces the outputs LOW.

MODE SELECT TABLE

OPERATING			- 1	NPUTS	3		OUTPUTS			
MODE	MR	S ₁	S ₀	DsR	DsL	Pn	Q ₀	Q ₁	Q ₂	Q ₃
Reset	L	Χ	Х	Х	Х	Х	L	L	L	L
Hold	Н	1	1	Х	Х	Х	qo	q1	q ₂	q 3
Shift Left	ΙΙ	h h	1	×	l h	X	Q1 Q1	q 2 q 2	q 3	Н
Shift Right	нн	I I	h h	l h	X	X	L H	90 90	Q1 Q1	q 2 q 2
Parallel Load	Н	h	h	Х	Х	pn	p ₀	p 1	p ₂	р3

I = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition. h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition, pn \mid qn \mid = Lower case letters indicate the state of the referenced input \mid or output \mid one setup time prior to the LOW-to-HIGH clock transition.

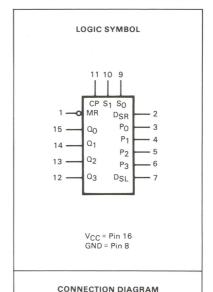
- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial

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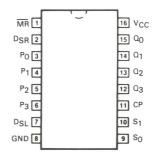
MC54F194 MC74F194

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

FAST™ SCHOTTKY TTL

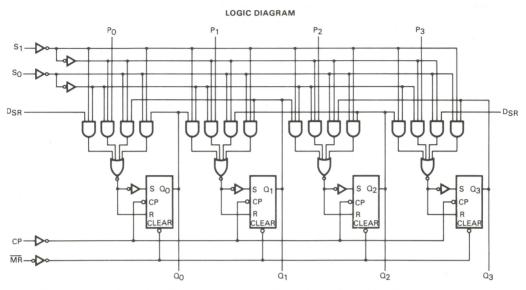


CONNECTION DIAGRAM



J Suffix — Case 620-08 (Ceramic)

N Suffix — Case 648-05 (Plastic)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER	-	MIN	TYP	MAX	UNIT
	0 1 1/1 *	54	4.50	5.0	5.50	V
V_{CC}	Supply Voltage*	74	4.75	5.0	5.25	1 V
-	O A T B	54	-55	25	125	0.0
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ТОН	Output Current — High	54, 74		1	-1.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

			54/74F		54	4F	74F		
		٦	A = +25°	С	T _A = -55	to +125°C	$T_A = 0 \text{ to } +70^{\circ}\text{C}$		
SYMBOL	PARAMETER	V	CC = +5.0	V	VCC = 5.0	0 V ±10%	V _{CC} = 5	$V_{CC} = 5.0 \text{ V} \pm 5\%$	
			CL = 50 pl	-	CL=	50 pF	CL=	50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax	Maximum Shift Frequency	105	150		90		90		MHz
tPLH	Propagation Delay	3.5	5.2	7.0	3.0	8.5	3.5	8.0	
tPHL	CP to Qn	3.5	5.5	7.0	3.0	8.5	3.5	8.0	ns
^t PHL	Propagation Delay MR to Q _n	4.5	8.6	12	4.5	14.5	4.5	14	ns

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DADAMETER			LIMITS		UNITS	TECT O	ONDITIONS		
STIVIBUL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CO	ONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inp	ut HIGH Voltage		
VIL	Input LOW Voltage				0.8	V	Guaranteed Inp	Guaranteed Input LOW Voltage		
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	I _{IN} = -18 mA V _{CC} = MIN		
1./	0	54	2.5	3.4		V	I _{OH} = -1.0 mA			
Vон	Output HIGH Voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	V _{CC} = MIN		
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN		
lu.	Innut HICH Current				20	μΑ	V _{IN} = 2.7 V	V MAY		
ΊΗ	Input HIGH Current				100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX		
IIL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX		
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX		
lcc	Power Supply Current			33	46	mA	S _n , MR, D _{SR} , D _{SL} = 4.5 V P _n = Gnd, CP =	V _{CC} = MAX		

NOTES

- For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC OPERATING REQUIREMENTS

			54/74F		5	4F	74	4F	
CVMADOL	DADAMETER	7	A = +25°(2	T _A = -55	to +125°C		to +70°C	LINUTC
SYMBOL	PARAMETER	V _{CC} = +5.0 V			$V_{CC} = 5.0 V \pm 10\%$		$V_{CC} = 5.0 \text{ V} \pm 5\%$		UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _s (H)	Set up Time, HIGH or LOW	4.0			4.0		4.0		
t _S (L)	Pn or DSR or DSL to CP	4.0			4.0		4.0		ns
th (H)	Hold Time, HIGH or LOW	0	*		1.0		1.0		113
th (L)	Pn or DSR or DSL to CP	0			1.0		1.0		
t _s (H)	Set up Time, HIGH or LOW	8.0			8.0		8.0		
t _S (L)	S _n to CP	8.0			8.0		8.0		ns
th (H)	Hold Time, HIGH or LOW	0			0		0		113
th (L)	S _n to CP	0			0		0		
$t_{W}(H)$	CP Pulse Width HIGH	5.0			5.5		5.5		ns
t _W (L)	MR Pulse Width LOW	5.0			5.0		5.0		ns
t _{rec}	Recovery Time MR to CP	7.0			9.0		8.0		ns



8-INPUT MULTIPLEXER (With 3-State Outputs)

DESCRIPTION — The MC54F/74F251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- MULTIFUNCTIONAL CAPACITY
- ON-CHIP SELECT LOGIC DECODING
- INVERTING AND NON-INVERTING 3-STATE OUTPUTS

FUNCTIONAL DESCRIPTION — This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, So, S1, S2. Both assertion and negation outputs are provided. The Output Enable input (OE) is active LOW. When it is activated, the logic function provided at the output is:

$$\begin{split} Z &= \overline{OE} \cdot (I_0 \cdot \overline{S_0} \cdot \overline{S_1} \cdot \overline{S_2} + I_1 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + I_2 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_4 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_6 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2 +$$

When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by typing the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

TRUTH TABLE

	INP	UTS		OUT	PUTS
ŌĒ	S ₂	S ₁	S ₀	Z	Z
Н	X	Χ	Χ	Z	Z
L	L	L	L	I ₀	10
L	L	L	Н	T ₁	I ₁
L	L	Н	L	Ī ₂	12
L	L	Н	Н	1 ₃	13
L	Н	L	L	Ī4	14
L	Н	L	Н	15	15
L	Н	Н	L	Ī ₅ Ī ₆	16
L	Н	Н	Н	Ī ₇	17

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

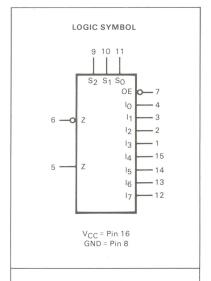
Z = High Impedance

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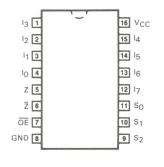
MC54F251 MC74F251

8-INPUT MULTIPLEXER (With 3-State Outputs)

FAST™ SCHOTTKY TTL



CONNECTION DIAGRAM

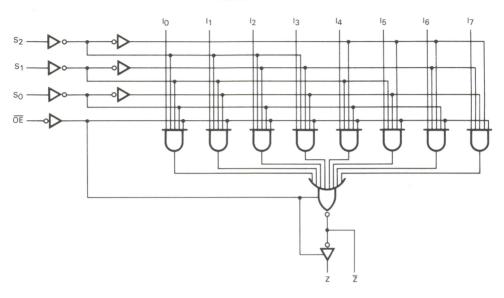


J Suffix — Case 620-08

(Ceramic)

N Suffix — Case 648-05 (Plastic)

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
	C 1 1/1 1/2	54	4.50	5.0	5.50	.,
VCC	Supply Voltage*	74	4.75	5.0	5.25	V
T 0	O A T	54	-55	25	125	
TA	Operating Ambient Temperature Range	74	0	25	70	°C
IOH	Output Current — High	54, 74			-1.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DARAMETER			LIMITS		LINUTO	TEOT O	ONDITIONS	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	I EST CO	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpi	ut HIGH Voltage	
VIL	Input LOW Voltage				0.8	V	Guaranteed Inpi	ut LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA V _{CC} = MIN		
V/	0	54	2.5	3.4	w #	V	I _{OH} = -1.0 mA		
VOH	Output HIGH Voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	V _{CC} = MIN	
VOL	Output LOW Voltage	•		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
l	In a set III CI I Comment				20	μΑ	V _{IN} = 2.7 V	\/	
lН	Input HIGH Current				100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX	
IIL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX	
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX	
		ON		15	22		I _n , S _n = 4.5 V OE = Gnd		
ICC	Power Supply Current	OFF		16	24	mA		V _{CC} = MAX	

NOTES:

- For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
 Not more than one output should be shorted at a time, nor for more than 1 second.

		54/74F						
PARAMETER						, ,		UNITS
.,,								0
	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay S_n to \overline{Z}_n	4.0 3.2	5.9 5.7	8.0 7.5	3.5 3.2	9.5 9.5	4.0 3.2	9.0 8.5	ns
Propagation Delay S _n to Z _n	4.5 5.0	9.6 6.9	13 9.0	3.5 3.0	16.5 10.5	4.5 4.0	14 10	ns
Propagation Delay	3.0 2.0	4.1 3.0	5.7 4.0	2.5 2.0	8.0 6.0	3.0 2.0	7.0 5.0	ns
Propagation Delay I _n to Z	5.5 3.7	7.2 5.1	9.5 6.5	3.5 3.7	11.5 7.5	5.5 3.7	10.5 7.5	ns
Output Enable Time OE to Z	3.0 3.5	5.4 6.4	7.0 8.5	3.0 3.5	9.5 10.5	3.0 3.5	8.0 9.5	ns
Output Disable Time OE to Z	3.0 2.0	5.0 3.2	6.5 4.5	3.0 2.0	8.5 7.5	3.0 2.0	7.5 5.5	ns
Output Enable Time OE to Z	4.0 3.5	6.9 6.0	9.0 8.0	4.0 3.5	10 10	4.0 3.5	10 9.0	ns
Output Disable Time OE to Z	3.0 2.0	4.7 3.5	6.0 4.5	3.0 2.0	7.0 5.5	3.0 2.0	7.0 5.5	ns
	$\begin{array}{c} S_{n} \text{ to } \overline{Z_{n}} \\ \\ \text{Propagation Delay} \\ S_{n} \text{ to } Z_{n} \\ \\ \text{Propagation Delay} \\ I_{n} \text{ to } \overline{Z} \\ \\ \text{Propagation Delay} \\ I_{n} \text{ to } Z \\ \\ \text{Output Enable Time} \\ \overline{OE} \text{ to } \overline{Z} \\ \\ \hline \text{Output Disable Time} \\ \overline{OE} \text{ to } \overline{Z} \\ \\ \hline \text{Output Enable Time} \\ \overline{OE} \text{ to } \overline{Z} \\ \\ \hline \text{Output Enable Time} \\ \hline OE \text{ to } Z \\ \\ \hline \text{Output Disable Time} \\ \hline OUTPUT DISABLE TIME} \\ \hline OUTPUT DISABLE TIME} \\ \hline OUTPUT DISABLE TIME} \\ \hline \hline OUTPUT DISABLE TIME} \\ \hline \hline OUTPUT DISABLE TIME} \\ \hline \hline OUTPUT DISABLE TIME} \\ \hline \hline OUTPUT DISABLE TIME} \\ \hline \hline OUTPUT DISABLE TIME TIME TIME TIME TIME TIME TIME TIM$	$\begin{array}{c c} \text{PARAMETER} & V \\ \hline & MIN \\ \hline \\ \text{Propagation Delay} & 4.0 \\ S_{n} \text{ to } \overline{Z}_{n} & 3.2 \\ \hline \\ \text{Propagation Delay} & 4.5 \\ S_{n} \text{ to } Z_{n} & 5.0 \\ \hline \\ \text{Propagation Delay} & 3.0 \\ I_{n} \text{ to } \overline{Z} & 2.0 \\ \hline \\ \text{Propagation Delay} & 5.5 \\ I_{n} \text{ to } \overline{Z} & 3.7 \\ \hline \\ \text{Output Enable Time} & 3.0 \\ \hline \\ \hline{OE} \text{ to } \overline{Z} & 3.5 \\ \hline \\ \hline \\ \text{Output Enable Time} & 3.0 \\ \hline \\ \hline{OE} \text{ to } \overline{Z} & 2.0 \\ \hline \\ \hline \\ \text{Output Enable Time} & 3.0 \\ \hline \\ \hline{OE} \text{ to } \overline{Z} & 3.5 \\ \hline \\ \hline \\ \text{Output Enable Time} & 4.0 \\ \hline \\ \hline{OE} \text{ to } Z & 3.5 \\ \hline \\ \hline \\ \hline \\ \text{Output Disable Time} & 3.0 \\ \hline \\ \hline{OE} \text{ to } \overline{Z} & 3.5 \\ \hline \\ \hline \\ \text{Output Disable Time} & 3.0 \\ \hline \\ \hline \\ \hline{OE} \text{ to } Z & 3.5 \\ \hline \\ \hline \\ \hline \\ \hline{Output Disable Time} & 3.0 \\ \hline \\ \hline \\ \hline{OE} \text{ to } Z & 3.5 \\ \hline \\ \hline \\ \hline \\ \hline \\ \hline{Output Disable Time} & 3.0 \\ \hline \\ \hline \\ \hline{OUtput Disable Time} & 3.0 \\ \hline \\ \hline \\ \hline \\ \hline \\ \hline \\ \hline \\ \hline \\ \hline \\ \hline \\ $	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$



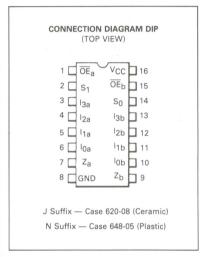
MC54F253 MC74F253

Advance Information

DESCRIPTION — The MC54F/74F253 is a Dual 4-Input Multiplexer with 3-State Outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high-impedance state with a HIGH on the respective Output Enable $\overline{\text{OE}}$ inputs, allowing the outputs to interface directly with bus oriented systems.

LOGIC DIAGRAM $\overline{\text{OE}}_{a}$ l_{1a} $\overline{\mathsf{OE}}_\mathsf{b}$ l_{3a} l_{2a} l_{0a} 13p l_{2b} 1_{1b} l₀b (5) 6 $V_{CC} = Pin 16$ GND = Pin 8 = Pin Numbers

DUAL 4-INPUT MULTIPLEXER
WITH 3-STATE OUTPUTS
FAST™ SCHOTTKY TTL



GUARANTEED OPERATING RANGES

00/110/111/11	01210111110110110					
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage*	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ГОН	Output Current — High	54, 74	_	_	-1.0	mA
loL	Output Current — Low	54, 74	_	_	20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0°C to 70°C temperature range.

FUNCTIONAL DESCRIPTION

The F253 contains two identical 4-Input Multiplexers with 3-State Outputs. They select two bits from four sources selected by common Select Inputs (S_0 , S_1). The 4-input multiplexers have individual Output Enable (\overline{OE}_a , \overline{OE}_b) inputs which when HIGH, force the outputs to a high impedance (high Z) state.

The F253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$\begin{split} Z_{a} &= \overline{OE}_{a} \cdot (I_{0a} \cdot \overline{S}_{1} \cdot \overline{S}_{0} + I_{1a} \cdot \overline{S}_{1} \cdot S_{0} + I_{2a} \cdot S_{1} \cdot \overline{S}_{0} + I_{3a} \cdot S_{1} \cdot S_{0}) \\ Z_{b} &= \overline{OE}_{b} \cdot (I_{0b} \cdot \overline{S}_{1} \cdot \overline{S}_{0} + I_{1b} \cdot \overline{S}_{1} \cdot S_{0} + I_{2b} \cdot S_{1} \cdot \overline{S}_{0} + I_{3b} \cdot S_{1} \cdot S_{0}) \end{split}$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

			NOTT	IADI			
	ECT UTS		DATA I	NPUT	S	OUTPUT ENABLE	ОИТРИТ
s ₀	S ₁	I ₀	11	12	l ₃	ŌE	Z
X	Х	X	Х	X	Χ	Н	(Z)
L	L	L	X	X	X	L	L
L	L	Н	X	X	X	L	Н
Н	L	X	L	X	X	L	L
Н	L	X	Н	X	X	L	Н
L	Н	X	X	L	X	L	L
L	H	X	X	Н	X	L	Н
- H	Н	X	X	X	L	L	,L
Н	Н	X	Х	Χ	Н	L	Н

H = HIGH Level

L = LOW Level

X = Immaterial

(Z) = High Impedance (off)

Address inputs So and S1 are common to both sections.

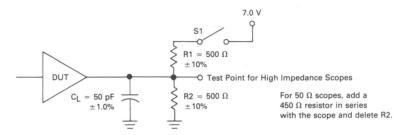
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

				LIMITS	3				
SYMBOL	PARAMETER		MIN	TYP		UNITS	TEST CO	NDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage		
VIL	Input LOW Voltage				0.8	V	Guaranteed Input L	OW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA, V _{CC}	= MIN	
	Output HIGH Voltage		2.5			V	$I_{OL} = -1.0 \text{ mA}$	V MINI	
VOH	Output HIGH Voltage		2.7			V	$I_{OL} = -1.0 \text{ mA}$	V _{CC} = MI	
VOL	Output LOW Voltage				0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
I					20	μΑ	V _{IN} = 2.7 V, V _{CC}	= MAX	
lН	Input HIGH Current				0.1	mA	$V_{IN} = 7.0 V, V_{CC} = MAX$		
ΊL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V, V _{CC} = MAX		
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V, V _{CC} = MAX		
,*	Power Supply Current Total, Output HIGH				16		$\overline{OE}_n = GND, V_{CC}$ $I_0, S_n = 4.5 \text{ V}; I_1$		
ICC	Total, Output LOW				23	mA	$I_n, S_n, \overline{OE}_n = GNE$ $V_{CC} = MAX$)	
	Total at HIGH-Z				23		$\overline{OE}_n = 4.5 \text{ V, V}_{CC}$ $I_n, S_n = GND$	= MAX	

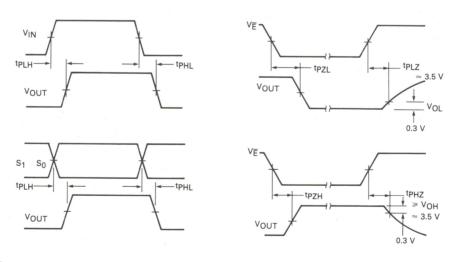
AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		$T_A = -55^{\circ}C$ $V_{CC} = 5.0$	1F C to +125°C 0 V ±10% 50 pF	$T_A = 0^{\circ}C$ $V_{CC} = 5.0$	4F to +70°C 0 V ±5.0% 50 pF	UNITS	S1 POSITION
		MIN	MAX	MIN	MAX	MIN	MAX		
^t PLH ^t PHL	Propagation Delay S _n to Z _n	5.5 4.5	12.5 11	3.5 2.5	15 12	4.5 3.5	13.5 12	ns	OPEN
^t PLH ^t PHL	Propagation Delay I _n to Z _n	3.0 3.0	7.0 7.0	2.5 2.5	9.0 8.0	3.0	8.0 8.0	ns	0, 2,,
^t PZH ^t PZL	Output Enable Time	3.0 3.0	9.0 9.5	2.5 2.5	10.5 11	3.0 3.0	10 10.5	ns	CLOSED
^t PHZ ^t PLZ	Output Disable Time	2.0 2.0	5.0 6.0	2.0 2.0	6.5 9.0	2.0 2.0	6.0 7.0	ns	OPEN CLOSED

AC TEST CIRCUIT



PROPAGATION DELAY MEASUREMENTS



- 1. All input waveforms have the following characteristics: Low Level = 0V High Level = 3.0 V

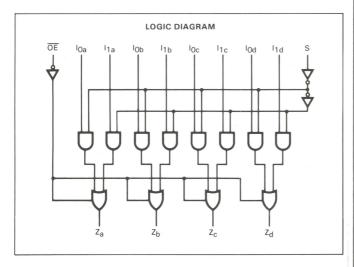
 - Rise and Fall Times (10% to 90%) = 2.5 ns
- 2. All timing is measured at 1.5 V unless otherwise indicated.



QUAD 3-INPUT MULTIPLEXER (With 3-State Outputs)

 $\mbox{DESCRIPTION}$ — The MC54F/74F257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (\overline{OE}) input, allowing the outputs to interface directly with bus oriented systems.

- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS



TRUTH TABLE

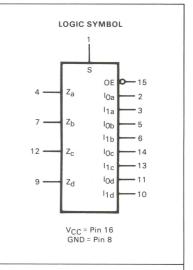
	OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
	ŌĒ	S	lo	l ₁	Z
	Н	Х	Х	Х	(Z)
	L	н	X	L	L
1	L	н	X	Н	н
1	L	L	L	X	L
	L	L	Н	Х	н

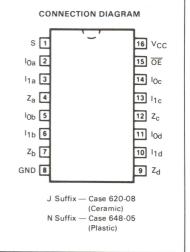
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MC54F257 MC74F257

QUAD 3-INPUT MULTIPLEXER (With 3-State Outputs)

FAST™ SCHOTTKY TTL





H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial (Z) = High Impedance

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER	2.2 4 3	MIN	TYP	MAX	UNIT		
.,	C 1 1/1/1/2 *	54	4.50	5.0	5.50	V		
VCC	Supply Voltage*	74	4.75	5.0	5.25	\ \		
_	0 4	54	-55	25	125	°C		
TA	Operating Ambient Temperature Range	74	0	25	70	٥,		
ГОН	Output Current — High	54, 74			-3.0	mA		
loL	Output Current — Low	54, 74			20	mA		

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DADAMETED		LIMITS			UNITS	TEST CONDITIONS		
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CO	NDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input	HIGH Voltage	
VIL	Input LOW Voltage				0.8	V	Guaranteed Input	LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
	*	54	2.5	3.4		V	I _{OH} = -1.0 mA		
VOH	Output HIGH Voltage	54	2.4	3.3		V	I _{OH} = -3.0 mA	V _{CC} = MIN	
	: "	74	2.7	3.3		V	IOH = -3.0 mA		
VOL	Output LOW Voltage			0.35	0.5	, V	I _{OL} = 20 mA	V _{CC} = MIN	
lozh	Output OFF Current — HIGH				50	μΑ	V _{OUT} = 2.4 V	V _{CC} = MAX	
lozL	Output OFF Current — LOW				-50	μΑ	V _{OUT} = 0.5 V	V _{CC} = MAX	
1	1				20		V _{IN} = 2.7 V	V _{CC} = MAX	
lН	Input HIGH Current			100	μΑ	V _{IN} = 7.0 V	ACC - INIAX		
IIL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX	
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX	
Іссн				9.0	15		S, I _{1x} = 4.5 V OE , I _{0x} = Gnd		
ICCL	Power Supply Current			14.5	22	mA	$\frac{I_{1x}}{OE}$ = 4.5 V $\frac{I_{0x}}{OE}$, I_{0x} , S = Gnd	V _{CC} = MAX	
ICCZ				15	23		S, I _{Ox} = Gnd OE, I _{1x} = 4.5 V		

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION — The F257 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the l_{0x} inputs are selected and when Select is HIGH, the l_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\begin{split} Z_{a} &= \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \\ Z_{C} &= \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \\ \end{split} \qquad Z_{b} &= \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S}) \\ Z_{d} &= \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S}) \end{split}$$

When the Output Enable input (\overline{OE}) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

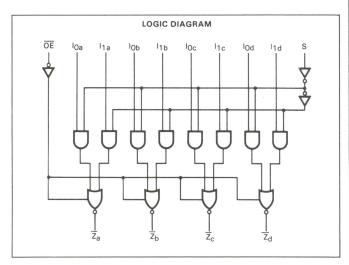
			54/74F		54	54F		4F		
	PARAMETER		T _A = +25°	C	$T_A = -55 \text{ to } +125^{\circ}\text{C}$		$T_A = 0 \text{ to } +70^{\circ}\text{C}$			
SYMBOL		\	CC = +5.0	V	V _{CC} = 5.	0 V ±10%	$V_{CC} = 5.0 V \pm 5\%$		UNITS	
			$C_L = 50 pf$		CL=	C _L = 50 pF		C _L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
tPLH	Propagation Delay	3.0	4.5	6.0	3.0	8.0	3.0	7.0		
tPHL	I _n to Z _n	2.5	4.2	5.5	2.5	8.0	2.5	6.5	ns	
tPLH	Propagation Delay	4.5	10.1	13	4.5	15.5	4.5	15		
t _{PHL}	S to Z _n	3.5	6.5	8.5	3.5	10.5	3.5	9.5	ns	
tPZH	O to the French In Time	3.0	5.9	7.5	3.0	9.5	3.0	8.5		
tPZL	Output Enable Time	3.0	5.5	7.5	3.0	10	3.0	8.5	ns	
tPZH	O to the District Time	2.0	4.3	6.0	2.0	7.0	2.0	7.0		
tPZL	Output Disable Time	2.0	4.5	6.0	2.0	9.5	2.0	7.0	ns	



QUAD 2-INPUT MULTIPLEXER (With 3-State Outputs)

DESCRIPTION — The MC54F/74F258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (\overline{OE}) input, allowing the outputs to interface directly with bus oriented systems.

- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- INVERTING 3-STATE OUTPUTS



TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
ŌĒ	S	lo lı		Z
н	Х	х х		Z
L	н	X L		Н
L	н	X	Н	L
L	L	L X		Н
L	L	Н	X	L

H = HIGH Voltage Level

L = LOW Voltage Level X = Immaterial

Z = High Impedance

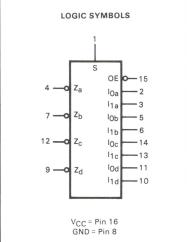
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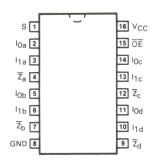
MC54F258 MC74F258

QUAD 2-INPUT MULTIPLEXER (With 3-State Outputs)

FASTTM SCHOTTKY TTL



CONNECTION DIAGRAM



J Suffix — Case 620-08

(Ceramic)

N Suffix — Case 648-05 (Plastic)

GUARANTEED OPERATING RANGES

TYP	MAX	
	IVIAA	UNIT
5.0	5.50	V
5.0	5.25	7 V
25	125	0.0
25	70	°C
	-3.0	mA
	20	mA
	5.0	5.0 5.25 25 125 25 70 -3.0

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DARAMETER		LIMITS			LINUTC	TEST CONDITIONS		
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CO	NULLIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input	HIGH Voltage	
VIL	Input LOW Voltage				0.8	V	Guaranteed Input	LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
		54	2.5	3.4		V	IOH = -1.0 mA		
Vон	Output HIGH Voltage	54	2.4	3.3		V	IOH = -3.0 mA	V _{CC} = MIN	
		74	2.7	3.3		V	I _{OH} = -3.0 mA		
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
lozh	Output OFF Current — HIGH				50	μА	V _{OUT} = 2.4 V	V _{CC} = MAX	
lozL	Output OFF Current — LOW				-50	μΑ	V _{OUT} = 0.5 V	V _{CC} = MAX	
					20		V _{IN} = 2.7 V	\/ B4A\/	
lН	Input HIGH Current			100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX		
IIL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX	
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX	
Іссн				6.2	9.5		S, I _{1x} = 4.5 V OE, I _{0x} = Gnd		
ICCL	Power Supply Current			15.1	23	mA	$\frac{I_{1x}}{OE}$, I_{0x} , S = Gnd	V _{CC} = MAX	
Iccz				11.3	17		S, I _{OX} = Gnd OE, I _{1X} = 4.5 V		

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION — The F258 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the 1_{1} inputs are selected and when Select is HIGH, the 1_{1} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The F258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\begin{split} \overline{Z}_a &= \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \\ \overline{Z}_c &= \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \\ \end{split} \qquad \begin{aligned} \overline{Z}_b &= \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S}) \\ \overline{Z}_d &= \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S}) \end{aligned}$$

When the Output Enable input (\overline{OE}) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

			54/74F		54F		7	4F		
		T _A = +25°C			$T_A = -55 \text{ to } +125^{\circ}\text{C}$		T _A = 0 to +70°C			
SYMBOL	PARAMETER	V _{CC} = +5.0 V			VCC = 5.0	0 V ±10%	V _{CC} = 5.0 V ±5%		UNITS	
		C _L = 50 pF			CL=	50 pF	C _L = 50 pF			
		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
tPLH	Propagation Delay	2.5	4.0	5.3	2.0	7.5	2.5	6.0		
tPHL	In to \overline{Z}_n	2.0	3.5	4.7	1.5	6.0	2.0	5.5	ns	
tPLH	Propagation Delay	4.0	6.5	8.5	4.0	12	4.0	9.5		
^t PHL	S to \overline{Z}_n	4.0	7.3	9.5	4.0	11.5	4.0	11	ns	
tPZH	0	3.0	5.9	7.5	3.0	11	3.0	8.5		
tPZL	Output Enable Time	3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns	
tPZH	0	2.0	4.3	6.0	1.5	7.0	2.0	7.0		
tPZL	Cluthuit Disable Time		4.5	6.0	2.0	9.0	2.0	7.0	ns	



4-BIT BINARY FULL ADDER (With Fast Carry)

DESCRIPTION — MC54F/74F283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words (A $_0$ -A $_3$, B $_0$ -B $_3$) and a Carry input(C $_0$). It generates the binary Sum outputs (S $_0$ -S $_3$) and the Carry output(C $_4$) from the most significant bit. The 'F283 will operate with either active-HIGH or active-LOW operands (positive or negative logic).

FUNCTIONAL DESCRIPTION — The 'F283 adds two 4-bit binary words (A plus B) plus the incoming carry C_0 . The binary sum appears on the Sum (S_0-S_3) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^{0} (A_0 + B_0 + C_0) + 2^{1} (A_1 + B_1)$$

 $+ 2^{2} (A_2 + B_2) + 2^{3} (A_3 + B_3)$
 $= S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$
Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0,A_0,B_0 can be arbitrarily assigned to pins 5,6 and 7. Due to the symmetry of the binary add function, the 'F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See Figure A. Note that if C_0 is not used it must be tied LOW for active-HIGH logic or tied HIGH for active-LOW logic.

Due to pin limitations, the intermediate carries of the 'F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure B shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A3, B3) LOW makes S3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure C shows a way of dividing the 'F283 into a 2-bit and a 1-bit adder. The third stage adder (A2 B2, S2) is used merely as a means of getting a carry (C₁₀) signal into the fourth stage (via A₂ and B₂) and bringing out the carry from the second stage on S2. Note that as long as A2 and B₂ are the same, whether HIGH or LOW, they do not influence S₂. Similarly, when A2 and B2 are the same the carry into the third stage does not influence the carry out of the third stage. Figure D shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs So, S1 and S2 present a binary number equal to the number of inputs I1 -I5 that are true. Figure E shows one method of implementing a 5-input majority gate. When three or more of the inputs I1 -I5 are true, the output M5 is true.

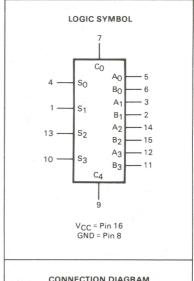
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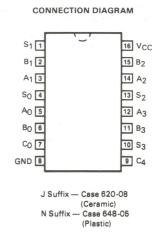
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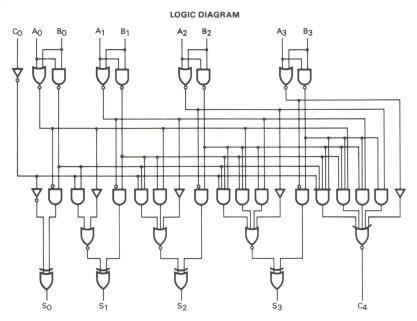
MC54F283 MC74F283

4-BIT BINARY FULL ADDER (With Fast Carry)

FAST™ SCHOTTKY TTL







Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

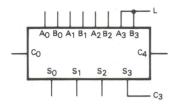
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT		
Vcc	C 1 1/1 *	54	4.50	5.0	5.50			
	Supply Voltage*	74	4.75	5.0	5.25	V		
-	Operating Ambient Temperature Range	54	-55	25	125	0.0		
TA		74	0	25	70	°C		
ЮН	Output Current — High	54, 74		_	-1.0	mA		
lOL	Output Current — Low	54, 74			20	mA		

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

FIGURE A — Active-HIGH versus Active-LOW Interpretation

	C ₀	A ₀	A ₁	A ₂	A ₃	B ₀	B ₁	B ₂	Вз	S ₀	S ₁	S ₂	S ₃	C ₄
Logic Levels	L	L	Н	L	Н	Н	L	L	Н	Н	Н	L	L	Н
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

FIGURE B - 3-Bit Adder



 ${\sf FIGURE\,D-5-Input\,Encoder}$

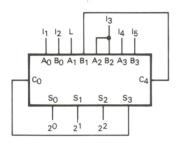


FIGURE C - 2-Bit and 1-Bit Adders

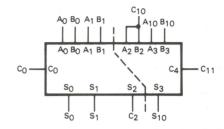
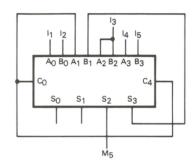


FIGURE E - 5-Input Majority Gate



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			LIMITS		UNITS	TECT CO	TEST COMPITIONS	
STIVIBUL			MIN	TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpu	it HIGH Voltage	
VIL	Input LOW Voltage				0.8	V	Guaranteed Inpu	it LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA V _{CC} = MIN		
1/	Outros HICH Valence	54	2.5	3.4		V	I _{OH} = -1.0 mA	VCC = MIN	
VOH	Output HIGH Voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	ACC - IAIIM	
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
lee e					20	μΑ	V _{IN} = 2.7 V	\/aa = MAY	
lН	Input HIGH Current				100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX	
	Input LOW Current								
IL	CO Input				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX	
	A and B Inputs				-1.2	mA			
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX	
Icc	Power Supply Current			36	55	mA	Inputs = 4.5 V	V _{CC} = MAX	

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

70 0117	MACIEMOTICS								
SYMBOL			54/74F		5	4F	7	UNITS	
	PARAMETER	\	T _A = +25°('CC = +5.0 C _L = 50 pf	V	V _{CC} = 5.	to +125°C 0 V ±10% 50 pF	T _A = 0 to +70°C V _{CC} = 5.0 V ±5% C _L = 50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	3.5	7.0	9.5	3.5	14	3.5	10.5	ns
tPHL	C ₀ to S _n	4.0	7.0	9.5	4.0	14	4.0	10.5	
tPLH	Propagation Delay	4.0	7.0	9.5	4.0	14	4.0	10.5	ns
tPHL	A _n or B _n to S _n	3.5	7.0	9.5	3.5	14	3.5	10.5	
tPLH	Propagation Delay	3.5	5.7	7.5	3.5	10.5	3.5	8.5	ns
tPHL	C ₀ to C ₄	3.0	5.4	7.0	3.0	10	3.0	8.0	
tPLH	Propagation Delay	3.5	5.7	7.5	3.5	10.5	3.5	8.5	ns
tPHL	A _n or B _n to C ₄	3.0	5.3	7.0	3.0	10	3.0	8.0	



4-BIT SHIFTER (With 3-State Outputs)

DESCRIPTION — MC54F/74F350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select (S0, S1) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the 3-state outputs of different packages and using the Output Enable (\overline{OE}) inputs as a third Select level. With appropriate interconnections, the F350 can perform zero-backfill, sign-extend or end-around (barrel) shift functions.

- Linking Inputs for Word Expansion
- 3-State Outputs for Extending Shift Range

FUNCTIONAL DESCRIPTION — The 'F350 is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes successive one-bit shifts of the data word. This internal connection makes it possible to perform shifts of 0, 1, 2 or 3 places on words of any length.

A 7-bit data word is introduced at the I_n inputs and is shifted according to the code applied to the select inputs $S_0,\,S_1$. Outputs $O_0\text{-}O_3$ are 3-state, controlled by an active-LOW output enable (\overline{OE}) . When \overline{OE} is LOW, data outputs will follow selected data inputs; when HIGH, the data outputs will be forced to the high-impedance state. This feature allows shifters to be cascaded on the same output lines or to a common bus. The shift function can be logical, with zeros pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

LOGIC EQUATIONS

 $\begin{array}{l} O_0 = \overline{S_0} \ \overline{S_1} \ |_0 + S_0 \ \overline{S_1} \ |_{-1} + \overline{S_0} \ S_1 \ |_{-2} + S_0 \ S_1 \ |_{-3} \\ O_1 = \overline{S_0} \ \overline{S_1} \ |_1 + S_0 \ \overline{S_1} \ |_0 + \overline{S_0} \ S_1 \ |_{-1} + S_0 \ S_1 \ |_{-2} \\ O_2 = \overline{S_0} \ \overline{S_1} \ |_2 + S_0 \ \overline{S_1} \ |_1 + \overline{S_0} \ S_1 \ |_0 + S_0 \ S_1 \ |_{-1} \\ O_3 = \overline{S_0} \ \overline{S_1} \ |_3 + S_0 \ \overline{S_1} \ |_2 + \overline{S_0} \ S_1 \ |_1 + S_0 \ S_1 \ |_0 \end{array}$

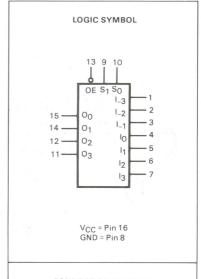
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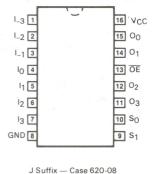
MC54F350 MC74F350

4-BIT SHIFTER (With 3-State Outputs)

FAST™ SCHOTTKY TTL



CONNECTION DIAGRAM



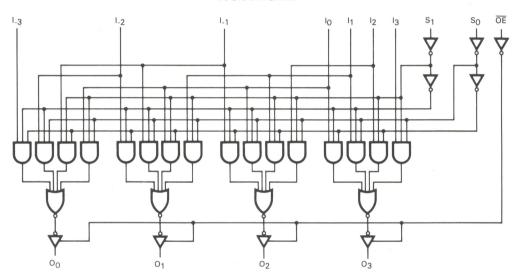
(Ceramic)
N Suffix — Case 648-05
(Plastic)

TRUTH TABLE

	NPUTS	3		OUT	PUTS	
OE	S ₁	S ₀	O ₀	O ₁	O ₂	O ₃
Н	Х	X	Z	Z	Z	Z
L	L	L	lo	11	12	13
L	L	Н	I_1	I ₀	11	12
L	Н	L	I_2	I-1	lo	I ₁
L	Н	Н	I_3	1-2	I_1	I ₀

H = HIGH Voltage Level L = LOW Voltage Level Z = High Impedance X = Immaterial

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

00/11//	TILLE OF ENAMED HANGED					
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
.,	C - L Walter *	54	4.50	5.0	5.50	V
VCC	Supply Voltage*	74	4.75	5.0	5.25	\ \
-	O A Li A T	54	-55	25	125	0.0
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ЮН	Output Current — High	54, 74	_	_	-3.0	mA
IOL	Output Current — Low	54, 74	_	_	20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			LIMITO	TEST COMPITIONS			
STIVIBUL			MIN	TYP	MAX	UNITS	TEST CONDITIONS			
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpu	Guaranteed Input HIGH Voltage		
VIL	Input LOW Voltage				0.8	V	Guaranteed Inpu	it LOW Voltage		
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN		
		54	2.5	3.4		V	I _{OH} = -1.0 mA			
Vон	Output HIGH Voltage	54	2.4	3.3		V	IOH = -3.0 mA	V _{CC} = MIN		
		74	2.7	3.3		V	IOH = -3.0 mA			
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN		
lozh	Output OFF Current — HIGH				50	μΑ	V _{OUT} = 2.4 V	V _{CC} = MAX		
lozL	Output OFF Current — LOW				-50	μА	V _{OUT} = 0.5 V	V _{CC} = MAX		
les e	Input HIGH Current				20		V _{IN} = 2.7 V	V _{CC} = MAX		
lН					100	μΑ	V _{IN} = 7.0 V			
IIL	Input LOW Current				-1.2	mA	V _{IN} = 0.5 V	V _{CC} = MAX		
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX		
Іссн				22	35		Outputs HIGH			
ICCL	Power Supply Current			26	41	mA	Outputs LOW	V _{CC} = Max		
ICCZ				26	42		Outputs OFF			

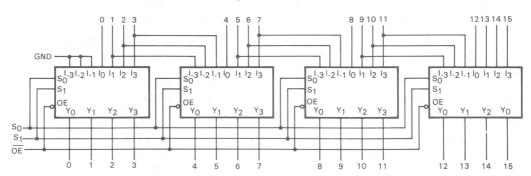
NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

SYMBOL			54/74F		54	1F	7	UNITS	
			T _A = +25°(2	$T_A = -55$	to +125°C	$T_A = 0$		
	PARAMETER	V	'CC = +5.0	V	V _{CC} = 5.	0 V ±10%	V _{CC} = 5		
		*	$C_L = 50 pF$		CL=	50 pF	C _L =	50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	3.0	4.5	6.0	3.0	7.5	3.0	7.0	
tPHL .	I _n to O _n	2.5	4.0	5.5	2.5	7.0	2.5	6.5	ns
tPLH	Propagation Delay	4.0	7.8	10	4.0	13	4.0	- 11	
^t PHL	S _n to O _n	3.0	6.5	8.5	3.0	10	3.0	9.5	ns
tPZH	Outside Facility Time	2.5	5.0	7.0	2.5	8.5	2.5	8.0	
tPZL	Output Enable Time	4.0	7.0	9.0	4.0	11	4.0	10	ns
tPHZ tPLZ		2.0	3.9	5.5	2.0	7.0	2.0	6.5	
	Output Disable Time	2.0	4.0	5.5	2.0	8.5	2.0	6.5	ns

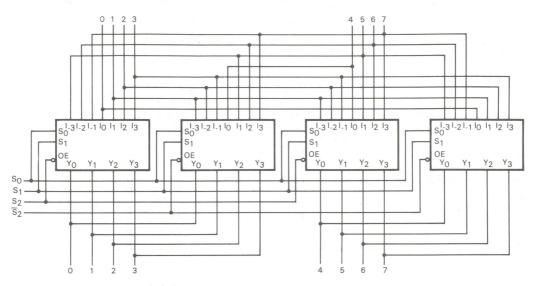
APPLICATIONS

16-Bit Shift-Up 0 to 3 Places, Zero Backfill



- S₁ S₀
- L L NO SHIFT
- L H SHIFT 1 PLACE
- H L SHIFT 2 PLACES
- H H SHIFT 3 PLACES

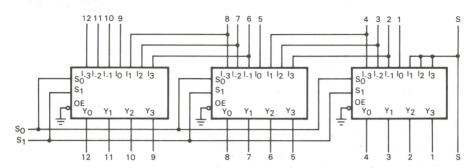
8-Bit End Around Shift 0 to 7 Places



- S2 S1 S0
- S₂ S₁ S₀ L L L NO SHIFT
- H L H SHIFT END AROUND 5
- L L H SHIFT END AROUND 1 L H L SHIFT END AROUND 2
- H H L SHIFT END AROUND 6
- L H H SHIFT END AROUND 3
- H H H SHIFT END AROUND 7
- H L L SHIFT END AROUND 4

MOTOROLA SCHOTTKY TTL DEVICES

13-Bit Twos Complement Scaler



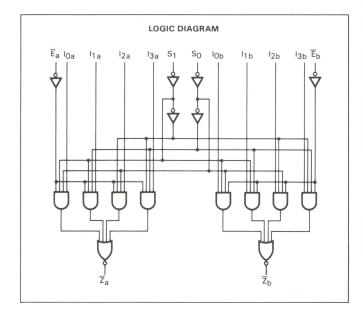


Advance Information

DUAL 4-INPUT MULTIPLEXER

DESCRIPTION — The MC54F/74F352 is a very high speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The 'F352 is the functional equivalent of the 'F153 except with inverted outputs.

- Inverted Version of the 'F153
- Separate Enables for Each Multiplexer
- Input Clamp Diode Limits High Speed Termination Effects



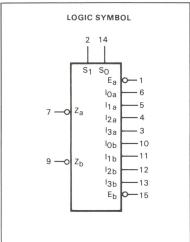
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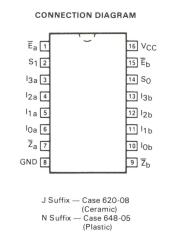
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MC54F352 MC74F352

DUAL 4-INPUT MULTIPLEXER

FAST™ SCHOTTKY TTL





GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V	S.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	54	4.50	5.0	5.50	V
VCC	Supply Voltage*	74	4.75	5.0	5.25	\ \
т.	O	54	-55	25	125	00
TA	Operating Ambient Temperature Range	74	0	25	70	°C
Іон	Output Current — High	54, 74	_	_	-1.0	mA
loL	Output Current — Low	54, 74	T -	_	20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

 $FUNCTIONAL\ DESCRIPTION — The `F352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S0, S1). The two 4-input multiplexer circuits have individual active-LOW Enables (\overline{E}_a, \overline{E}_b) which can be used to strobe the outputs independently. When the Enables (\overline{E}_a, \overline{E}_b) are HIGH, the corresponding outputs (\overline{Z}_a, \overline{Z}_b) are forced HIGH. }$

The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{E_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 \bullet I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)}$$

$$\overline{Z}_b = \overline{E_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 \bullet I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)}$$

The 'F352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'F352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

	LECT PUTS		INP	UTS	(a or	p)	OUTPUT
S ₀	S ₁	Ē	I ₀	l ₁	l ₂	13	Z
Х	X	Н	Х	Х	Х	Х	Н
L	L	L	L	X	X	X	н
L	L	L	Н	X	X	X	L
Н	L	L	Х	L	X	X	Н
н	L	L	X	Н	X	X	L
L	Н	L	X	X	L	X	н
L	Н	L	Х	X	Н	X	L
Н	Н	L	Х	X	X	L	Н
Н	Н	L	X	X	X	Н	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

0)/14001	DADAMETER			LIMITS		LINUTO	TECT Of	NOTIONS	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CC	out LOW Voltage VCC = MIN VCC = MIN VCC = MIN VCC = MAX VCC = MAX	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpo	ut HIGH Voltage	
VIL	Input LOW Voltage				0.8	V	Guaranteed Inpo	ut LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
Vон	Output HIGH Voltage	54	2.5	3.4		V	I _{OH} = -1.0 mA	Voc - MIN	
vон	Output high voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	$V_{CC} = MIN$ $V_{CC} = MIN$ $V_{CC} = MIN$ $V_{CC} = MAX$	
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
					20		V _{IN} = 2.7 V	V 844V	
JIH .	Input HIGH Current				100	μΑ	V _{IN} = 7.0 V	ACC = INIXX	
IL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX	
los	Output Short Circuit Current (Note 2)		-60		-150	mA .	V _{OUT} = 0 V	V _{CC} = MAX	
^I ССН	Power Supply Current			9.3	14	mA	V _{IN} = Gnd	V _{CC} = MAX	
CCL	Current			13.3	20	IIIA	V _{IN} = HIGH		

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

		54/74F		5	4F	74	4F	
	T	A = +25°0	2	T _A = -55	to +125°C	T _A = 0 t		
PARAMETER	$V_{CC} = +5.0 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 10\%$				V _{CC} = 5.	UNITS		
	($C_L = 50 pF$		CL=	50 pF	CL = !		
	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay	4.0	7.4	13	3.5	14.5	4.0	14	
S_n to \overline{Z}_n	4.0	7.0	13	3.5	15	4.0	14	ns
Propagation Delay	5.0	8.7	14	4.5	17	5.0	15	
E _n to Z _n	4.0	8.6	11	4.0	13	4.0	12	ns
Propagation Delay	2.0	4.9	7.0	2.0	9.0	2.0	8.0	
I_n to \overline{Z}_n	2.0	3.0	6.0	2.0	7.5	2.0	7.0	ns
	$\begin{array}{c} \text{Propagation Delay} \\ S_n \text{ to } \overline{Z}_n \\ \\ \underline{Propagation Delay} \\ \overline{E}_n \text{ to } \overline{Z}_n \\ \\ \\ \underline{Propagation Delay} \end{array}$	$\begin{array}{c c} \text{PARAMETER} & V \\ \hline & MIN \\ \hline \\ \text{Propagation Delay} & 4.0 \\ S_n \text{ to } \overline{Z}_n & 4.0 \\ \hline \\ \text{Propagation Delay} & 5.0 \\ \hline \\ \overline{E}_n \text{ to } \overline{Z}_n & 4.0 \\ \hline \\ \text{Propagation Delay} & 2.0 \\ \hline \end{array}$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$



Advance Information

DUAL 4-INPUT MULTIPLEXER (With 3-State Outputs)

DESCRIPTION — The MC54F/74F353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (\overline{OE}) inputs, allowing the outputs to interface directly with bus oriented systems.

- Inverted Version of 'F253
- Multifunction Capability
- Separate Enables for Each Multiplexer

FUNCTIONAL DESCRIPTION — The 'F353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S₀, S₁). The 4-input multiplexers have individual Output enable (\overline{OE}_a , \overline{OE}_b) inputs which, when HIGH, force the outputs to a high impedance (high Z) state. The logic equations for the outputs are shown below:

$$\begin{split} \overline{Z}_a &= \overline{OE}_a \bullet (I_{Oa} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0) \\ &= I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0) \\ \overline{Z}_b &= \overline{OE}_b \bullet (I_{Ob} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0) \\ &= I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0) \end{split}$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

_							
	LECT PUTS	DA	TAI	NPU'	TS	OUTPUT ENABLE	OUTPUT
S ₀	S ₁	I ₀	I ₁	l ₂	l ₃	ŌĒ	Z
X	Х	Х	Х	X	X	Н	(Z)
L	L	L	X	X	X	L	н
L	L	Н	X	X	X	L	L
Н	L	X	L	X	X	L	н
Н	L	X	Н	X	X	L	L
L	Н	X	X	L	X	L	Н
L	Н	Х	X	Н	X	L	L
Н	Н	X	X	X	L	L	Н
Н	Н	X	X	X	Н	L	L

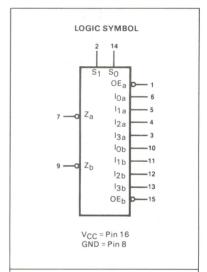
H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial (Z) = High Impedance

Address inputs S₀ and S₁ are common to both sections.

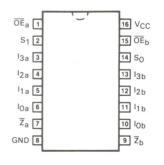
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MC54F353 MC74F353

DUAL 4-INPUT MULTIPLEXER (With 3-State Outputs)

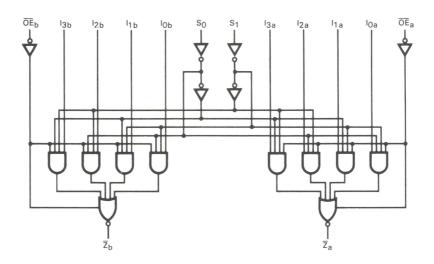


CONNECTION DIAGRAM



J Suffix — Case 620-08 (Ceramic) N Suffix — Case 648-05 (Plastic)

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
	C	54	4.50	5.0	5.50	.,
VCC	Supply Voltage*	74	4.75	5.0	5.25	V
T .	0 1	54	-55	25	125	0.0
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ГОН	Output Current — High	54, 74			-3.0	mA
lOL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

AC CHARACTERISTICS

			54/74F		54	1F	7	4F	
			T _Δ = +25°(2	TA = -55 t	to +125°C	$T_A = 0 \text{ to } +70^{\circ}\text{C}$ $V_{CC} = 5.0 \text{ V } \pm 5\%$		
SYMBOL	PARAMETER	\ \	CC = +5.0	V	V _{CC} = 5.0) V ±10%			UNITS
			C _L = 50 pf	:	CL=	50 pF	CL=	50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH tPHL	Propagation Delay S _n to Z _n	5.0 4.0	8.8 7.4	14 11	5.0 4.0	16 14	5.0 4.0	15 12	ns
tPLH tPHL	Propagation Delay	3.0	5.6 2.8	7.0 6.0	3.0 2.0	9.0 7.5	3.0 2.0	8.0 7.0	ns
tPZH tPZL	Output Enable Time	3.0	6.8 7.2	9.0 9.5	3.0 3.0	11 12	3.0 3.0	10 10.5	ns
tPHZ tPLZ	Output Disable Time	2.0 2.0	3.7 4.4	5.0 6.0	2.0 2.0	6.5 8.5	2.0 2.0	6.0 7.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMPOL	DADAMETED			LIMITS		LINITC	TEST COL	NDITIONS	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	IESI COI	t LOW Voltage VCC = MIN VCC = MIN VCC = MIN VCC = MAX VCC = MAX VCC = MAX VCC = MAX VCC = MAX	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input	HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage		
VIK	Input Clamp Diode Voltage	,			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
		54	2.5	3.4		V	I _{OH} = -1.0 mA		
Vон	Output HiGH Voltage	54	2.4	3.3		V	I _{OH} = -3.0 mA	V _{CC} = MIN	
		74	2.7	3.3		V	IOH = -3.0 mA		
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
lozh	Output OFF Current — HIGH				50	μΑ	V _{OUT} = 2.4 V	V _{CC} = MAX	
lozL	Output OFF Current — LOW				-50	μΑ	V _{OUT} = 0.5 V	V _{CC} = MAX	
I.e.	I				20		V _{IN} = 2.7 V	V MAAV	
lΗ	Input HIGH Current				100	μА	V _{IN} = 7.0 V	ACC = MAX	
IIL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX	
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX	
ICCH ICCL ICCZ	Power Supply Current			9.3 13.3 15	14 20 23	mA	I_n , S_n , \overline{OE}_n =Gnd I_n , S_n = Gnd \overline{OE}_n = 4.5 V	V _{CC} = Max	

NOTES:

- For conditions such as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.



MC54F373 MC74F373

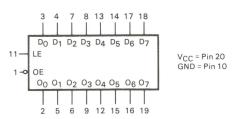
Advance Information

OCTAL TRANSPARENT LATCH (With 3-State Inputs)

DESCRIPTION — The MC54F/74F373 consists of eight latches with 3-state outputs for bus organized system applications. The flipflops appear transparent to the data when Latch Enable (Le) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the bus output is in the high impedance state.

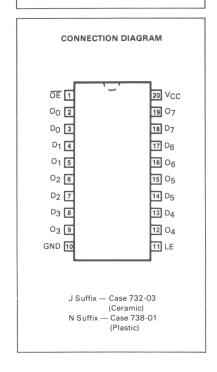
- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing

LOGIC SYMBOL



OCTAL TRANSPARENT LATCH (With 3-State Inputs)

FAST™ SCHOTTKY TTL



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
1/	S*	54	4.50	5.0	5.50	
VCC	Supply Voltage*	74	4.75	5.0	5.25	_ v
т.	O	54	-55	25	125	00
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ІОН	Output Current — High	54, 74			-3.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

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are subject to change without notice.

FUNCTIONAL DESCRIPTION — The 'F373 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_{Π} inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DARAMETER			LIMITS		LINUTC	TECT OF	NIDITIONIC	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	IEST CC	t HIGH Voltage	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpu	OH = -1.0 mA OH = -3.0 mA OH = -3.0 mA OL = 20 mA VCC = MIN VCC = MIN VCC = MIN VCC = MIN VCC = MAX VCC = MAX VCC = MAX VCC = MAX VCC = MAX VCC = MAX VCC = MAX	
VIL	Input LOW Voltage				0.8	V	Guaranteed Inpu	it LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
		54	2.5	3.4		V	I _{OH} = -1.0 mA		
Vон	Output HIGH Voltage	54	2.4	3.3		V	I _{OH} = -3.0 mA	V _{CC} = MIN	
		74	2.7	3.3		V	I _{OH} = -3.0 mA		
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
lozh	Output OFF Current — HIGH				50	μΑ	V _{OUT} = 2.4 V	V _{CC} = MAX	
lozL	Output OFF Current — LOW				-50	μΑ	V _{OUT} = 0.5 V	V _{CC} = MAX	
l	Janua HICH Command				20		V _{IN} = 2.7 V	V MAY	
ΙН	Input HIGH Current				100	μА	V _{IN} = 7.0 V	VCC = MAX	
IIL.	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX	
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX	
loo=	Power Supply Current			35	55	mA	OE = 4.5 V	= 4.5 V	
ICCZ	(All Outputs OFF)			35	55	IIIA	D _n , LE = Gnd	VCC = MAX	

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

			54/74F		5-	4F	7-	4F		
		T _A = +25°C			T _A = -55	to +125°C	$T_A = 0 t$	o +70°C		
SYMBOL	PARAMETER	V	CC = +5.0	V	V _{CC} = 5.	0 V ±10%	V _{CC} = 5.0 V ±5%		UNITS	
	y		C _L = 50 pl	F	C _L =	50 pF	CL=	50 pF		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
tPLH tPHL	Propagation Delay D _n to O _n	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.5 6.0	3.0 2.0	8.0 6.0	ns	
^t PLH ^t PHL	Propagation Delay LE to O _n	5.0 3.0	9.0 5.2	11.5 7.0	5.0 3.0	15 8.5	5.0 3.0	13 8.0	ns	
tPZH tPZL	Output Enable Time	2.0 2.0	5.0 5.6	11 7.5	2.0 2.0	13.5 10	2.0 2.0	12 8.5	ns	
tPHZ tPLZ	Output Disable Time	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	10 7.0	2.0	7.5 6.0	ns	

AC OPERATING REQUIREMENTS:

			54/74F		5	4F	74	4F	
SYMBOL	PARAMETER		T _A = +25° CC = +5.0		$T_A = -55 \text{ to } +125^{\circ}\text{C}$ $V_{CC} = 5.0 \text{ V} \pm 10\%$				UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _S (H) t _S (L)	Setup Time, HIGH or LOW D _n to LE	2.0 2.0			2.0 2.0		2.0		
t _h (H) t _h (L)	Hold Time, High or LOW D _n to LE	3.0 3.0			3.0		3.0 3.0		ns
t _W (H)	LE Pulse Width HIGH	6.0			6.0		6.0		ns



Advance Information

OCTAL D-TYPE FLIP-FLOP (With 3-State Outputs)

DESCRIPTION — The MC54F/74F374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops.

- Edge-triggered D-Type Inputs
- Buffered Positive Edge-triggered Clock
- 3-State Outputs for Bus Oriented Applications

FUNCTIONAL DESCRIPTION — the 'F374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable $(\overline{\text{OE}})$ LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{\text{OE}}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{\text{OE}}$ input does not affect the state of the flip-flops.

TRUTH TABLE

INP	UTS	OUTPUTS				
Dn	СР	ŌĒ	On			
Н	7	L	Н			
L	X	L	L 7			

H = HIGH Voltage Level

L = LOW Voltage Level

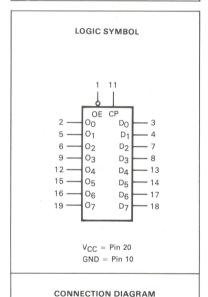
X = Immaterial

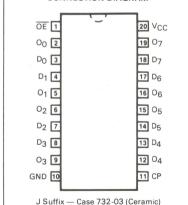
Z = High Impedance

MC54F374 MC74F374

OCTAL D-TYPE FLIP-FLOP (With 3-State Outputs)

FAST™ SCHOTTKY TTL

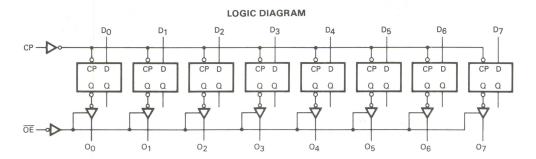




N Suffix — Case 738-01 (Plastic)

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GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V	C	54	4.50	5.0	5.50	V
VCC	Supply Voltage*	74	4.75	5.0	5.25	\ \
т.	0	54	-55	25	125	0.0
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ЮН	Output Current — High	54, 74			-3.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMETER			LIMITS		LINUTO	TECT OF	PAIDITIONS
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CC	ONDITIONS
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpi	ut HIGH Voltage
VIL	Input LOW Voltage				0.8	V	Guaranteed Inpi	ut LOW Voltage
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
	54		2.5	3.4			I _{OH} = -1.0 mA	
Vон	Output HIGH Voltage 54		2.4	3.3		V	IOH = -3.0 mA	V _{CC} = MIN
			2.7	3.3		V	IOH = -3.0 mA	
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
lozh	Output OFF Current — HIGH				50	μΑ	V _{OUT} = 2.4 V	V _{CC} = MAX
lozL	Output OFF Current — LOW				-50	μΑ	V _{OUT} = 0.5 V	V _{CC} = MAX
l	Innut HICH Current				20		V _{IN} = 2.7 V	\/ B4AV
lН	Input HIGH Current				100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX
IIL	Input LOW Current				-0.6	. mA	V _{IN} = 0.5 V	V _{CC} = MAX
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
ICCL	Power Supply Current (All Outputs OFF)			55	86	mA	$D_n = Gnd$ $\overline{OE} = 4.5V$	V _{CC} = MAX

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

			54/74F		5	4F	7	4F	
			T _A = +25°C			$T_A = -55 \text{ to } +125^{\circ}\text{C}$		T _A = 0 to +70°C	
SYMBOL	PARAMETER	V _{CC} = +5.0 V				0 V ±10%	$V_{CC} = 5.0 V \pm 5\%$		UNITS
			$C_{L} = 50 \text{ pl}$	F	CL=	C _L = 50 pF		50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}	Maximum Clock Frequency	100	v		60		70		MHz
tPLH	Propagation Delay	4.0	6.5	8.5	4.0	10.5	4.0	10	
tPHL .	CP to On	4.0	6.5	8.5	4.0	11	4.0	10	ns
tPZH	Outside Facility Time	2.0	9.0	11.5	2.0	14	2.0	12.5	
tPZL	Output Enable Time	2.0	5.8	7.5	2.0	10	2.0	8.5	ns
tPHZ	Outnut Diaghla Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0	
tPLZ	Output Disable Time	2.0	4.3	5.5	2.0	7.5	2.0	6.5	

AC OPERATING REQUIREMENTS:

SYMBOL PARAMETER		54/74F T _A = +25°C V _{CC} = +5.0 V			T _A = -55	4F to +125°C 0 V ±10%			UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _S (H) t _S (L)	Setup Time, HIGH or LOW D _n to CP	2.0 2.0			2.5 2.0		2.0 2.0		
t _h (H)	Hold Time, HIGH or LOW D _n to CP	2.0 2.0			2.0 2.5		2.0 2.0		ns
t _W (H)	CP Pulse Width, HIGH or LOW	7.0 6.0			7.0 6.0		7.0 6.0		ns



MC54F381 MC74F381

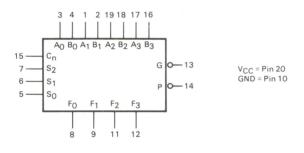
Advance Information

4-BIT ARITHMETIC LOGIC UNIT

DESCRIPTION — The MC54F/74F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. Carry Propagate and Generate outputs are provided for use with the 'F182 Carry Lookahead Generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the 'F382 ALU data sheet.

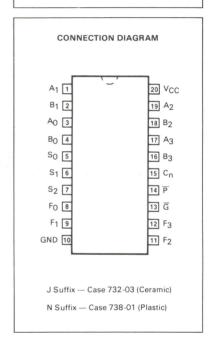
- Low Input Loading Minimizes Drive Requirements
- Performs Six Arithmetic and Logic Functions
- Selectable Low (Clear) and High (Preset) Functions
- Carry Generate and Propagate Outputs for use with Carry Lookahead Generator

LOGIC SYMBOL



4-BIT ARITHMETIC LOGIC UNIT

FAST™ SCHOTTKY TTL



GUARANTEED OPERATING RANGES

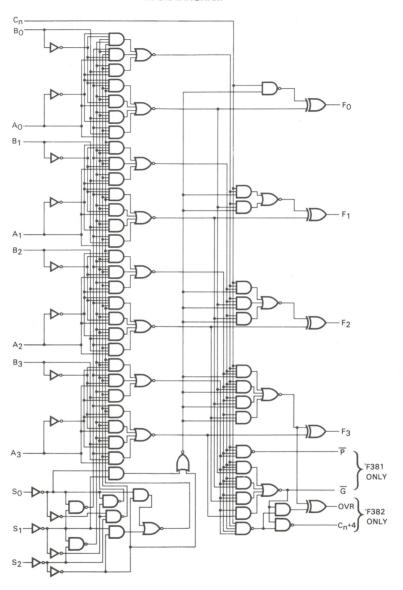
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
1/	C - 1 V 1: *	54	4.50	5.0	5.50	V
VCC	Supply Voltage*	74	4.75	5.0	5.25	V
т.	O	54	-55	25	125	00
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ІОН	Output Current — High	54, 74			-1.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

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LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

0)/14001	DADAMETED			LIMITS		LINUTC	TECT COA	IDITIONS	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input	HIGH Voltage	
VIL	Input LOW Voltage				0.8	V	Guaranteed Input	ut LOW Voltage	
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
V/	Output HICH Valtage	54	2.5	3.4		V	I _{OH} = -1.0 mA	VCC = MIN	
VOH	Output HIGH Voltage 74		2.7	3.4		V	I _{OH} = -1.0 mA	ACC = IAIIIA	
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
	1				20	μΑ	V _{IN} = 2.7 V	\/ - BAA\/	
lН	Input HIGH Current			100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX		
In	Input LOW Current SO - S2 Inputs				-0.6	mA	V _{IN} = 0.5 V	Vcc = MAX	
IIL	Other Inputs				-2.4	mA	V _{IN} = 0.5 V	ACC - INIAX	
los	Output Short Circuit Current (Note 2)		-60		-150	mA .	V _{OUT} = 0 V	V _{CC} = MAX	
ICC	Power Supply Current			59	89	mA	S _O – S ₃ = GND; Other Inputs HIGH	V _{CC} = MAX	

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

 $FUNCTIONAL \ DESCRIPTION \ - \ Signals \ applied to the Select inputs \ S_0-S_2 \ determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active-HIGH or active-LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active-HIGH operands, LOW for active-LOW operands) into the <math>C_0$ input of the least significant package.

The Carry Generate (\overline{G}) and Carry Propagate (\overline{P}) outputs supply input signals to the 'F182 carry lookahead generator for expansion to longer word length, as shown in Figure A. Note that an 'F382 ALU is used for the most significant package. Typical delays for Figure A are given in Figure B.

FUNCTION SELECT TABLE

	SELECT		OPERATION
S ₀	S ₁	S ₂	
L	L	L	Clear
н	L	L	B Minus A
L	Н	L	A Minus B
Н	Н	L	A Plus B
L	L	Н	A⊕B
Н	L	Н	A + B
L	Н	. н	AB
Н	Н	Н	Preset

H = HIGH Voltage Level

L = LOW Voltage Level

A₁₂-A₁₅ B₁₂-B₁₅ A₀-A₃ B₀-B₃ A4-A7 B4-B7 A8-A11 B8-B11 CIN ► C_{OUT} Cn+4 ^Cn F381 F381 F381 S F G s F382 OVR - OVERFLOW G P F G P SELECT 3 F0-F3 F4-F7 F₁₂-F₁₅ F8-F11 G₀ P₀ C_{n + x} G₁ P₁ C_{n+y} G₂ P₂ C_{n+z} Cn 'F182 CLA

FIGURE A - 16-Bit Lookahead Carry ALU Expansion

FIGURE B - 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT Cn + 4, OVR
$\begin{array}{c} A_i \text{ or } B_i \text{ to } \overline{P} \\ \overline{P}_i \text{ to } C_n +_j \text{ ('F182')} \\ C_n \text{ to } F \\ C_n \text{ to } C_{n+4}, \text{ OVR} \end{array}$	7.2 ns 6.2 ns 8.1 ns	7.2 ns 6.2 ns — 8.0 ns
Total Delay	21.5 ns	21.4 ns

AC CHARACTERISTICS

			54/74F		5	4F	7	4F	
					$T_A = -55 \text{ to } +125^{\circ}\text{C}$		$T_A = 0 \text{ to } +70^{\circ}\text{C}$		
SYMBOL	PARAMETER	00			V _{CC} = 5.0 V ±10%		$V_{CC} = 5.0 \text{ V} \pm 5\%$ $C_{I} = 50 \text{ pF}$		UNITS
			C _L = 50 p	F	CL=	50 pF	CL=	50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	2.5	8.1	10.5	2.5	15	2.5	11.5	
tPHL	C _n to F _i	2.5	5.7	8.0	2.5	11.5	2.5	9.0	ns
tPLH	Propagation Delay	4.0	10.4	13.5	4.0	19	4.0	14.5	
t _{PHL}	Any A or B to Any F	3.5	8.2	11	3.5	15.5	3.5	12	ns
tPLH	Propagation Delay	4.5	8.3	11	4.5	15.5	4.5	12	
TPHL	S _i to F _i	4.0	8.2	11	4.0	15.5	4.0	12	ns
tPLH	Propagation Delay	3.5	6.4	9.0	3.5	12.5	3.5	10	
t _{PHL}	A _i or B _i to \overline{G}	4.0	6.8	10	4.0	14	4.0	11	ns
tPLH	Propagation Delay	4.0	7.2	10.5	4.0	15	4.0	11.5	
t _{PHL}	A _i or B _i to P	3.5	6.5	9.5	3.5	13	3.5	10.5	ns
tPLH	Propagation Delay	4.0	7.8	10.5	4.0	15	4.0	11.5	
tPHL	S _i to G or P	4.5	10.2	13.5	4.5	19	4.5	14.5	ns

TRUTH TABLE

			INP	UTS				(DUT	PUTS	 3	
FUNCTION	S ₀	S ₁	S ₂	Cn	An	Bn	F ₀	F ₁	F ₂	F ₃	G	P
CLEAR	0	0	0	Х	Х	Х	0	0	0	0	0	0
B MINUS A	1	0	0	0 0 0 0 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1	1 0 0 1 0 1 1	1 1 0 1 0 1 0	1 1 0 1 0 1 0	1 1 0 1 0 1 0	1 0 1 1 1 0	0 0 1 0 0 0
A MINUS B	0	1	0	0 0 0 0 1 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1	1 0 0 1 0 1 1	1 0 1 1 0 0 1 0	1 0 1 1 0 0 1 0	1 0 1 1 0 0 1 0	1 1 0 1 1 1 0	0 1 0 0 0
A PLUS B	1	1	0	0 0 0 0 1 1 1	0 0 1 1 0 0 1	0 1 0 1 0 1 0	0 1 1 0 1 0 0	0 1 1 1 0 0 0	0 1 1 1 0 0 0	0 1 1 1 0 0 0	1 1 1 0 1 1 1	1 0 0 0 1 0
А⊕В	0	0	1	X X X	0 0 1 1	0 1 0 1	0 1 1 0	0 1 1 0	0 1 1 0	0 1 1 0	0 1 1 0	0 1 0
A + B	1	0	1	X X X	0 0 1 1	0 1 0 1	0 1 1	0 1 1 1	0 1 1	0 1 1 1	0 1 1 1	0 1 1 0
AB	0	1	1	X X X	0 0 1 1	0 1 0 1	0 0 0 1	0 0 0	0 0 0 1	0 0 0 1	0 1 0 1	0 1 0 0
PRESET	1	1	1	X X X	0 0 1 1	0 1 0 1	1 1 1	1 1 1 1	1 1 1	1 1 1	1 1 1	1 1 1 0

^{1 =} HIGH Voltage Level 0 = LOW Voltage Level

X = Immaterial



MC54F521 MC74F521

Advance Information

8-BIT IDENTITY COMPARATOR

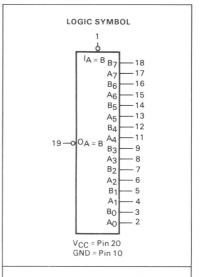
DESCRIPTION — The MC54F/74F521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_A = B$ also serves as an active-LOW enable input.

- Compares Two 8-Bit Words in 6.5 ns Typ
- Expandable to Any Word Length
- 20-Pin Package

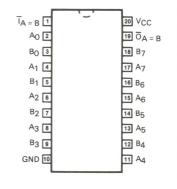
LOGIC DIAGRAM A0 B0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7 TA = B Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

8-BIT IDENTITY COMPARATOR

FAST™ SCHOTTKY TTL







J Suffix — Case 732-03 (Ceramic) N Suffix — Case 738-01 (Plastic)

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GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
\/	S*	54	4.50	5.0	5.50	V
VCC	Supply Voltage*	74	4.75	5.0	5.25	V
т.	O	54	-55	25	125	00
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ІОН	Output Current — High	54, 74			-1.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMETED			LIMITS		UNITS	TECT OF	MIDITIONIC	
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CC	ONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage		
VIL	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage		
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
	0	54	2.5	3.4		- V	IOH = -1.0mA		
VOH	Output HIGH Voltage	74	2.7	3.4		V	I _{OH} = -1.0 mA	V _{CC} = MIN	
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
lini	Input HIGH Current				20	μΑ	V _{IN} = 2.7 V	V _{CC} = MAX	
lн	input high current				100	μΑ	V _{IN} = 7.0 V	VCC - IVIAX	
IIL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V CC = MAX	
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX	
Іссн	Power Supply Current			24	36		T _A = B = Gnd V _{CC} = MAX		
ICCL	Fower Supply Current			15.5	23	mA	IA - B - Glid	VCC = MAX	

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

TRUTH TABLE

	Inputs	Output
TA = B	A, B	OA = B
L	A = B*	L
L	A ≠ B	Н
Н	$A = B^*$	Н
н	A ≠ B	Н

H = HIGH Voltage Level

L = LOW Voltage Level

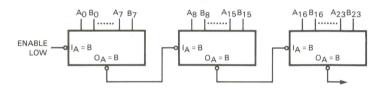
 $*A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

AC CHARACTERISTICS

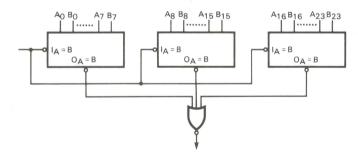
			54/74F		54	4F	74	4F	
		1	A = +25°0	2	T _A = -55	to +125°C	T _A = 0 to +70°C		
SYMBOL	PARAMETER	V	CC = +5.0	V	V _{CC} = 5.	0 V ±10%	V _{CC} = 5	.0 V ±5%	UNITS
			$C_L = 50 pF$:	CL=	50 pF	CL=	50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	3.5	6.5	9.5	3.5	15	3.5	11	
tPHL	A_n or B_n to $\overline{O}_A = B$	4.0	6.5	9.0	4.0	12	4.0	10.5	ns
tPLH	Propagation Delay	3.0	4.5	6.5	3.0	8.5	3.0	7.5	
tPHL	$\overline{I}A = B$ to $\overline{O}A = B$	3.5	5.0	7.0	3.5	9.0	3.5	8.0	ns

APPLICATIONS

Ripple Expansion



Parallel Expansion





MC54F533 MC74F533

Advance Information

OCTAL TRANSPARENT LATCH (With 3-State Outputs)

DESCRIPTION — The MC54F/74F533 consists of eight latches with 3-state outputs for bus organized system applications. The flipflops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the bus output is in the high-impedance state. The F533 is the same as the F373, except that the outputs are inverted. For description and logic diagram please see the F373 data sheet.

LOGIC SYMBOL

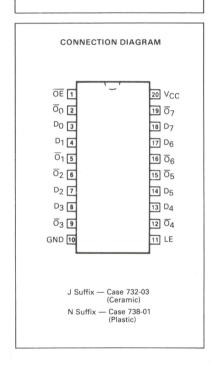
12 15 16 19

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing

3 4 7 8 13 14 17 18 DO D1 D2 D3 D4 D5 D6 D7 E VCC = Pin 20 GND = Pin 10

OCTAL TRANSPARENT LATCH (With 3-State Outputs)

FAST™ SCHOTTKY TTL



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
\/	S*	54	4.50	5.0	5.50	V
VCC	Supply Voltage*	74	4.75	5.0	5.25	V
т.	O	54	-55	25	125	0.0
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ЮН	Output Current — High	54, 74			-3.0	mA
loL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70° C temperature range.

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVAADOL	DADAMETED			LIMITS		LINUTC	TECT OC	MIDITIONIC		
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CC	NDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage			
VIL	Input LOW Voltage				0.8	V	Guaranteed Inpu	Guaranteed Input LOW Voltage		
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	I _{IN} = -18 mA V _{CC} = MIN		
		54	2.5	3.4		V	I _{OH} = -1.0 mA			
Vон	Output HIGH Voltage	54	2.4	3.3		V	IOH = -3.0 mA	V _{CC} = MIN		
		74	2.7	3.3		V	I _{OH} = -3.0 mA			
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN		
lozh	Output OFF Current — HIGH	+			50	μΑ	V _{OUT} = 2.4 V	V _{CC} = MAX		
lozL	Output OFF Current — LOW	/			-50	μΑ	V _{OUT} = 0.5 V	V _{CC} = MAX		
Local	1				20	μА	V _{IN} = 2.7 V	V B4AV		
lН	Input HIGH Current				100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX		
IIL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX		
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX		
ICCZ	Power Supply Current			41	61	mA	OE = 4.5 V D _n , LE = Gnd	V _{CC} = MAX		

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

			54/74F		54	ŀF	74	4F	
		T _A = +25°C			$T_A = -551$	to +125°C	$T_A = 0 t$	o +70°C	
SYMBOL	PARAMETER	V	CC = +5.0	V	V _{CC} = 5.0) V ±10%	V _{CC} = 5.	0 V ±5%	UNITS
			$C_L = 50 pF$		C _L = !	50 pF	CL=	50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Propagation Delay	4.0	6.9	9.0	4.0	12	4.0	10	
tPHL	D_n to \overline{O}_n	3.0	5.2	7.0	3.0	9.0	3.0	8.0	ns
tPLH	Propagation Delay	5.0	8.5	11	5.0	14	5.0	13	
tPHL	LE to \overline{O}_n	3.0	5.6	7.0	3.0	9.0	3.0	8.0	ns
tPZH	0	2.0	7.7	10	2.0	12.5	2.0	11	
tPZL	Output Enable Time	2.0	5.1	6.5	2.0	9.0	2.0	7.5	ns
tPHZ	0	2.0	4.7	6.0	2.0	8.5	2.0	7.0	
tPLZ	Output Disable Time	2.0	4.1	5.5	2.0	7.5	2.0	6.5	ns

AC CHARACTERISTICS

			54/74F		54	1F	7	4F	
SYMBOL	PARAMETER	TER $T_A = +25^\circ$				to +125°C 0 V ±10%			UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _S (H) t _S (L)	Setup Time, HIGH or LOW D _n to LE	2.0			2.0 2.0		2.0 2.0		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW D _n to LE	3.0 3.0	,		3.0 3.0		3.0 3.0		ns
t _w (H)	LE Pulse Width HIGH	6.0			6.0		6.0		ns



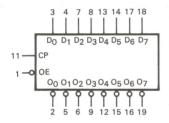
Advance Information

OCTAL D-TYPE FLIP-FLOP (With 3-State Outputs)

DESCRIPTION — The MC54F/74F534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops. The 'F534 is the same as the 'F374 except that the outputs are inverted.

- Edge-triggered D-Type Inputs
- Buffered Positive Edge-triggered Clock
- 3-State Outputs for Bus Oriented Applications

LOGIC SYMBOL

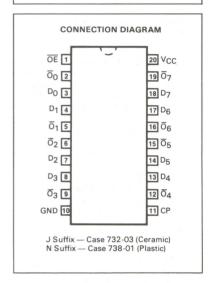


V_{CC} = Pin 20 GND = Pin 10

MC54F534 MC74F534

OCTAL D-TYPE FLIP-FLOP (With 3-State Outputs)

FAST™ SCHOTTKY TTL



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
1/	C	54	4.50	5.0	5.50	V
VCC	Supply Voltage*	74	4.75	5.0	5.25	V .
т.	O	54	-55	25	125	00
TA	Operating Ambient Temperature Range	74	0	25	70	°C
ІОН	Output Current — High	54, 74			-3.0	mA
lOL	Output Current — Low	54, 74			20	mA

^{*74}F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

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LOGIC DIAGRAM D3 D₆ D₁ D_2 D₄ D_5 D7 Do D D D D 0 Ω Ω 0 0 Ω \cap 0

 $\overline{0}_{6}$

07

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION — The 'F534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

CVMBOL	BABAMETER			LIMITS		LINITO	TEST CO	NUDITIONS		
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CC	ONDITIONS		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Inpu	Guaranteed Input HIGH Voltage		
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Inpu	Guaranteed Input LOW Voltage		
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	I _{IN} = -18 mA V _{CC} = MIN		
		54	2.5	3.4		V	I _{OH} = -1.0 mA			
Vон	Output HIGH Voltage	54	2.4	3.3		V	IOH = -3.0 mA	V _{CC} = MIN		
		74	2.7	3.3		V	I _{OH} = -3.0 mA			
VOL	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN		
lozh	Output OFF Current — HIGH				50	μА	V _{OUT} = 2.4 V	V _{CC} = MAX		
lozL	Output OFF Current — LOW				-50	μА	V _{OUT} = 0.5 V	V _{CC} = MAX		
I	I t III CII C				20	^	V _{IN} = 2.7 V	V NAAV		
lн	Input HIGH Current				100	μΑ	V _{IN} = 7.0 V	V _{CC} = MAX		
IIL	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V CC = MAX		
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX		
Iccz	Power Supply Current (All Outputs OFF)			55	86	mA	$\frac{D_n}{OE} = Gnd$	V _{CC} = MAX		

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

			54/74F		54	4F	74	1F	
			T _A = +25°	С	T _A = -55	to +125°C	$T_A = 0 t$	o +70°C	
SYMBOL	PARAMETER	\	CC = +5.0	V	V _{CC} = 5.0	0 V ±10%	V _{CC} = 5.	0 V ±5%	UNITS
			$C_L = 50 p$	F	CL=	50 pF	C _L = .	50 pF	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax	Maximum Clock Frequency	100			60		70	MHz	
tPLH	Propagation Delay	4.0	6.5	8.5	4.0	10.5	4.0	10	
^t PHL	CP to \overline{O}_n	4.0	6.5	8.5	4.0	11	4.0	10	ns
tPZH	Outside Frankla Fina	2.0	9.0	11.5	2.0	14	2.0	12.5	
tPZL	Output Enable Time	2.0	5.8	7.5	2.0	10	2.0	8.5	
tPHZ	Out of Disable Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0	
tPLZ	Output Disable Time	2.0	4.3	5.5	2.0	7.5	2.0	6.5	ns

AC OPERATING REQUIREMENTS

			54/74F		54	1F	74	4F	
SYMBOL	YMBOL PARAMETER		T _A = +25°C V _{CC} = +5.0 V			T _A = -55 to +125°C V _{CC} = 5.0 V ±10%		$T_A = 0 \text{ to } +70^{\circ}\text{C}$ $V_{CC} = 5.0 \text{ V } \pm 5\%$	
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	0.00
t _S (H) ~t _S (L)	Setup Time, HIGH or LOW D _n to CP	2.0 2.0			2.5 2.0		2.0 2.0		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW D _n to CP	2.0 2.0			2.0 2.5		2.0 2.0		110
t _W (H) t _W (L)	CP Pulse Width HIGH or LOW	7.0 6.0			7.0 6.0		7.0 6.0		ns



MC74F2960 (Formerly SN74ALS790)

Product Preview

ERROR DETECTION AND CORRECTION CIRCUIT

DESCRIPTION — The MC74F2960 Error Detection and Correction Unit (EDAC) contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the MC74F2960 will correct any single bit error* and will detect all double and some triple bit errors. For 16-bit words, 6 check bits are used. The MC74F2960 is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

The MC74F2960 also features two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions. The product will be supplied in a 48-lead DIP package.

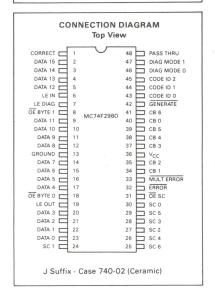
*Double bit errors can also be corrected if at least one of the two errors is a hard error. This requires extra processor cycles.

- PIN AND FUNCTIONALLY COMPATIBLE WITH THE Am2960
- BOOSTS MEMORY RELIABILITY
- EXPANDABLE TO 64-BIT DATA WORDS
- BUILT-IN DIAGNOSTICS PERMITS SOFTWARE SYSTEM CHECK
- SEPARATE BYTE CONTROLS FACILITATE BYTE OPERATIONS
- COMPATIBLE WITH MC68000 AND OTHER PROCESSORS

16-BIT TIMING (WORST CASE)
CHECK BIT GENERATION — 23 ns
SINGLE ERROR DETECTION — 23 ns
SINGLE ERROR CORRECTION — 48 ns

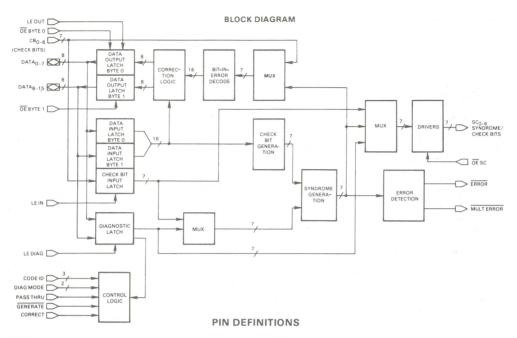
ERROR DETECTION AND CORRECTION CIRCUIT

ADVANCED LOW POWER SCHOTTKY



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VCC	Supply Voltage	4.75	5.0	5.25	V.
TA	Operating Ambient Temperature Range	0	25	70	°C
ІОН	Output Current — High			-0.8	mA
lOL	Output Current — Low			8.0	mA



DATA₀₋₁₅

16 bidirectional data lines. They provide input to the Data Input Latch and Diagnostic Latch, and receive output from the Data Output Latch, DATAO is the least significant bit; DATA15 the most significant.

CB₀₋₆

Seven Check Bit input lines. The check bit lines are used to input check bits for error detection. They are also used to input syndrome bits for error correction in 32 and 64-bit configurations.

LE IN

Latch Enable — Data Input Latch. Controls latching of the input data. When HIGH the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.

GENERATE

Generate Check Bits input. When this input is LOW the EDAC is in the Check Bit Generate Mode. When HIGH the EDAC is in the Detect Mode or Correct Mode.

In the Generate Mode the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs.

In the Detect or Correct Modes the EDAC detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct Mode, single-bit errors are also automatically corrected — corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the bit-in-error.

SC₀₋₆

Syndrome/Check Bit outputs. These seven lines hold the check/partial-check bits when the EDAC is in Generate Mode, and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct Modes. These are 3-state outputs.

OF SC

Output Enable — Syndrome/Check Bits. When LOW, the 3-state output lines SC_{0-6} are enabled. When HIGH, the SC outputs are in the high impedance state.

ERROR

Error Detected output. When the EDAC is in Detect or Correct Mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate Mode, ERROR is forced HIGH. (In a 64-bit configuration, ERROR must be externally implemented.)

MULTERROR

Multiple Errors Detected output. When the EDAC is in Detect or Correct Mode, this output if LOW indicates that there are two or more bit errors that have been detected. If HIGH this indicates that either one or no errors have been detected. In Generate mode, MULT ERROR is forced HIGH. (In a 64-bit configuration, MULT ERROR must be externally implemented.)

CORRECT

Correct input. When HIGH this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it onto the Data Output Latch. When LOW the EDAC will drive data directly from the Data Input Latch to the Data Output Latch without correction.

PIN DEFINITIONS (continued)

LE OUT

Latch Enable — Data Output Latch. Controls the latching of the Data Output Latch. When LOW the Data Output Latch is latched to its previous state. When HIGH the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are unspecified if the EDAC is in Generate Mode.

OE BYTE 0. OE BYTE 1

Output Enable — Bytes 0 and 1, Data Output Latch. These lines control the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW these lines enable the Data Output Latch and when HIGH these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output Latch at a time.

PASS THRU

Pass Thru input. This line when HIGH forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SCO-6) and the unmodified contents of

the Data Input Latch onto the inputs of the Data Output Latch

DIAG MODEO-1

Diagnostic Mode Select. These two lines control the initialization and diagnostic operation of the EDAC.

CODE ID₀₋₂

Code Identification inputs. These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDAC is processing. The three allowable data word sizes are 16, 32 and 64-bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID2, ID1, ID0) is also used to instruct the EDAC that the signals CODE ID0–2, DIAG MODE0–1, CORRECT and PASS THRU are to be taken from the Diagnostic Latch, rather than from the input control lines.

LE DIAG

Latch Enable — Diagnostic Latch. When HIGH the Diagnostic Latch follows the 16-bit data on the input lines. When LOW the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits, and internal control signals for CODE ID0–2, DIAG MODE0–1, CORRECT and PASS THRU.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

01/14001	PARAMETER		LIMITS			LINUTO	TEST CONDITIONS	
SYMBOL	PARAME	IEK	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
VIL	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
VIK	Input Clamp Diode V	'oltage			-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
Vон	Output HIGH Voltage	е	2.7			V	V _{CC} = MIN, I _{OH} = -0.8 mA	
VOL	Output LOW Voltage	9			0.5	V	V _{CC} = MIN, I _{OL} = 8.0 mA	
lozu	Output Off	DATA ₀₋₁₅			70	μΑ	Voc - MAX Voux - 2.4 V	
lozh	Current-HIGH	SC ₀₋₆			50	μА	Guaranteed Input LOW Voltage V _{CC} = MIN, I _{IN} = -18 mA V _{CC} = MIN, I _{OH} = -0.8 mA	
lozu	Output Off	DATA ₀₋₁₅	×		-410	μА	Voc = MAX Voux = 0.5 V	
IOZL	Current-LOW	SC ₀₋₆			-50	μΑ	Guaranteed Input HIGH Volta Guaranteed Input LOW Volta VCC = MIN, IIN = -18 mA VCC = MIN, IOH = -0.8 mA VCC = MIN, IOH = 8.0 mA VCC = MIN, IOH = 2.4 V VCC = MAX, VOUT = 2.4 V VCC = MAX, VIN = 2.7 V VCC = MAX, VIN = 5.5 V VCC = MAX, VIN = 0.5 V VCC = MAX, VIN = 0.5 V	
Loca	Input High	DATA ₀₋₁₅			70	μΑ	V00 = MAX VIII = 2.7 V	
ΊΗ	Current	OTHERS			50	μΑ	VCC - WAX, VIN - 2.7 V	
		ALL			1.0	mA	V _{CC} = MAX, V _{IN} = 5.5 V	
T	Input Low	DATA ₀₋₁₅			-410	μΑ	V MAY V 0 5 V	
IIL	Current	OTHERS			-360	μА	ACC - MAY, AIN = 0.9 A	
los	Short Circuit Current (1)		-25		-85	mA	V _{CC} = MAX, V _O = 0.0 V	
Icc	Power Supply Current				400	mA	V _{CC} = MAX	

⁽¹⁾ Not more than one output should be shorted at a time.

MC74F2960

FUNCTIONAL DESCRIPTION

The MC74F2960 contains the necessary logic to generate check bits on a 16-bit data field according to a modified Hamming code. This code allows the EDAC to 1) be cascaded, 2) detect all double bit errors, 3) detect RAM failure (all 1 or 0 data).

The EDAC may be configured to work on data words from 8- to 64-bits in length. When cascaded for word lengths in excess of 16 bits, each EDAC must know which bits it is processing. This is done with Code ID inputs as shown in Table I. The Internal Control Mode is described later.

MODE SELECTION

The device control lines are $\overline{\text{GENERATE}}$, CORRECT, PASS THRU, DIAG MODE₀₋₁ and CODE ID₀₋₂. Table II lists the MC74F2960 modes of operation.

PASS THRU MODE

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on the SC outputs. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in this mode.

GENERATE MODE

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the SC outputs.

DETECT MODE

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, ERROR goes LOW. If two or more errors are detected, MULT ERROR goes LOW. Both error indicators are HIGH if there are no errors.

Also available on the SC outputs are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without correction.

CORRECT MODE

In this mode, the EDAC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified.

DIAGNOSTIC GENERATE DIAGNOSTIC DETECT DIAGNOSTIC CORRECT

These are special diagnostic modes where check bits loaded into the Diagnostic Latch are substituted for either normal check bit inputs or outputs.

INITIALI7F

The inputs of the Data Output Latch are forced to zeroes. The check bit outputs (SC) are generated to correspond to the all-zero data. ERROR and MULT ERROR are forced HIGH in the initialize Mode.

Initialize Mode is useful after power up when RAM contents are random. The EDAC may be placed in initialize mode and its' outputs written into all memory locations by the processor.

INTERNAL CONTROL MODE

When in the internal control mode, the EDAC takes the CODE ${\rm ID}_{0-2}$, DIAG ${\rm MODE}_{0-1}$, CORRECT and PASS THRU control signals from the Internal Diagnostic Latch rather than from the external input lines.

TABLE I. HAMMING CODE AND SLICE IDENTIFICATION

CODE ID ₂	CODE ID ₁	CODE ID ₀	Hamming Code and Slice Selected
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Bytes 0 and 1
0	1	1	Code 32/39, Bytes 2 and 3
1	0	0	Code 64/72, Bytes 0 and 1
1	0	1	Code 64/72, Bytes 2 and 3
1	1	0	Code 64/72, Bytes 4 and 5
1	1	1	Code 64/72, Bytes 6 and 7

TABLE II. INTERNAL CONTROL MODE

	CONTROL INPUTS						
	DIAG	DIAG		GENERATE	CORRECT		
	MODE	MODE	THRU				
OPERATING MODE	1	0					
PASS THRU	X	Х	1	X	×		
GENERATE	X	0	0	0	X		
DETECT	0	X	0	1	0		
CORRECT	0	X	0	1	1		
DIAGNOSTIC GENERATE	0	1	0	0	X		
DIAGNOSTIC DETECT	-1	0	0	1	0		
DIAGNOSTIC CORRECT	1	0	0	1	1		
INITIALIZE	1	1	0	Х	X		



MC74F2968 MC74F2969 MC74F2970

Product Preview A NEW GENERATION OF MEMORY SUPPORT PRODUCTS

Motorola and Advanced Micro Devices have agreed to cooperate on the development of the next generation of the F2960 Family of Memory Support products. These devices are designed to maximize the speed and minimize the cost of memory systems based on the new generation of high performance 64K and 256K MOS Dynamic RAMs (DRAMs).

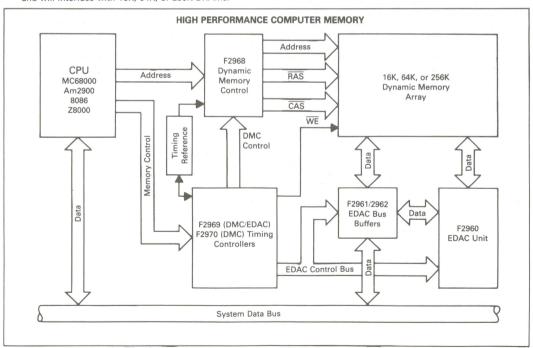
The products included in this joint development and alternate sourcing agreement are a Dynamic Memory Controller (DMC), the F2968, and two Memory Timing Controllers (MTC), the F2969 and F2970. These functions are partitioned such that address generation and refresh are provided by the F2968. Memory timing and control is achieved with either the F2969 or F2970. This partitioning allows greater design flexibility and higher system performance than would be possible by combining the DMC and MTC functions on a single chip. All three devices will be fabricated using the high performance, oxide-isolated bipolar technologies with TTL compatible I/O levels.

The Dynamic Memory Controller, F2968, will provide complete address multiplexing, refreshing, and output drive for up to 88 Dynamic Random Access Memories (DRAMs). The F2968 will be packaged in a 48-pin DIP and will interface with 16K, 64K, or 256K DRAMs.

The memory timing controller will be available in two versions. The F2969, a 48-pin version, will provide all control signals for both the F2968 Memory Controller and the F2960 Error Detection and Correction circuit (EDAC). The F2969 Timing Controller will support error logging and also handle memory initialization, refresh timing, and memory cycle arbitration. The general purpose microprocessor interface on the F2969 will facilitate its use with most microprocessors with minimal external logic. The MC68000 AMD/Intel iAPX86, and AMD 2900 bit-slice and 29116 devices are notable examples. System timing for all memory functions is derived from an external delay line to provide maximum performance and flexibility.

For systems not utilizing the F2960 Error Detection and Correction circuit (EDAC), a second version of the timing controller, the F2970, will be available without (EDAC) interface/functions. The F2970 will save on IC cost and board space as it will be packaged in 24-pin, 300-mil wide DIP.

Sample quantities on the F2968, F2969, and the F2970 are expected in the fourth quarter 1983, with production commencing early in 1984. F2960 samples are expected in the third quarter of 1983.

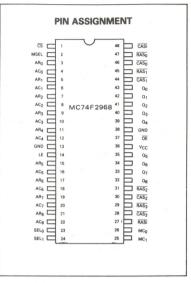


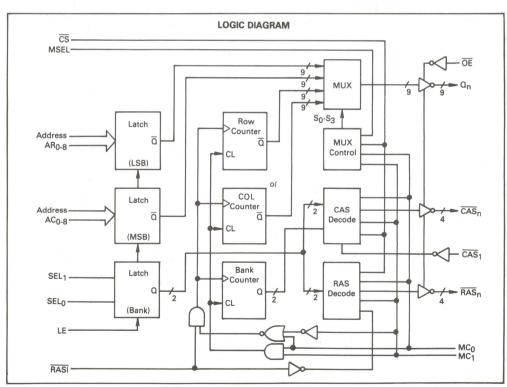
DYNAMIC MEMORY CONTROLLER

The MC74F2968 Dynamic Memory Controller is intended to be used with today's high performance memory systems. It has two 9-bit address latches which allow the chip to be used with 16K, 64K, or 256K dynamic RAMs. A two-bit bank select latch for the two high order address bits is provided to select one each of the four RAS and CAS outputs.

In the refresh mode, two counters cycle through the refresh address. Only the ROW counter is used for refresh without scrubbing, generating up to 512 addresses to refresh a 512-cycle-refresh DRAM. The column counter is used only for refresh with scrubbing. In this mode all RAS outputs are generated with only one CAS output.

- Provides Control for 16K, 64K, or 256K Dynamic RAM Systems
- Outputs Directly Drive Up to 88 DRAMs
- Highest Order Two Address Bits Select One of Four Banks of RAMs
- Separate RAS and CAS Lines for Each Bank of DRAM
- Supports Memory Scrubbing During Refresh
- Supports Nibble Mode Access
- Separate Output Enable for Multi-Channel Access-to-Memory
- Chip Select for Easy Expansion
- 48-Pin Dual In-Line Package





DYNAMIC MEMORY TIMING CONTROLLERS

The MC74F2969/2970 Dynamic Memory Timing Controllers are intended to be used with today's high performance memory systems. They have been designed to offer the system designer maximum flexibility and performance. Timing for both circuits is derived from an external delay line.

The F2969 is designed to control the timing for systems incorporating the MC74F2960 Error Detection And

MC74F2969

- Provides Complete Timing Control for 16K, 64K, or 256K Dynamic RAM Systems Which Utilize F2960, F2961/2962, and F2968
- WE Output Directly Drives Up to 88 DRAMs
- Delay-Line Controlled Timing for Maximum Performance
- Synchronous or Asynchronous Arbitration of Memory Cycles
- Supports Memory Scrubbing During Refresh
- Internal or External Control of Refresh
- Burst or Distributed Refresh Modes
- 128-, 256-, or 512-Cycle Burst Refresh
- Performs Hidden Refresh When Processor Accesses Other Devices (Distributed Mode)
- Supports Byte-Writes for Memory Up to 32-Bits Wide
- Supports the Bus Retry Feature of the MC68010

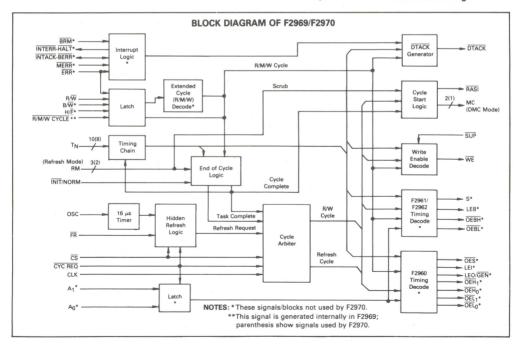
Correction circuit, the MC74F2961/62 EDAC Bus Buffers, and the MC74F2968 Dynamic Memory Controller.

For memory systems not utilizing the F2960 EDAC unit, the F2970 will provide all control signals for the F2968 while reducing IC cost and circuit board area. The F2970 supports functions which are a subset of the F2969. By choosing not to utilize EDAC support functions, the F2970 can be packaged in a 24-pin DIP.

- Initializes Memory
- 48-Pin Dual In-Line Package

MC74F2970

- Provides Complete Timing Control for 16K, 64K, or 256K Dynamic RAM Systems Which Utilize the F2968
- WE Output Directly Drives Up to 88 DRAMs
- Delay-Line Controlled Timing for Maximum Performance
- Synchronous or Asynchronous Arbitration of Memory Cycles
- Internal or External Control of Refresh
- Burst or Distributed Refresh Modes
- 128-, 256-, or 512-Cycle Burst Refresh
- Performs Hidden Refresh When Processor Accesses Other Devices (Distributed Mode)
- 24-Pin, 300 Mil Wide Dual In-Line Package



SCHOTTKY TTL



RAM/PROM Data Sheets



2048-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7621 and MCM7621A, together with various other 76xx series TTL PROMS, have common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available with three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

All pinouts are compatible to industry-standard PROMs and ROMs.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1.0 Second per 1024 Bits, Typical)
- Expandable Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
 Low Input Current 250 μA Logic "0", 40 μA Logic "1"
 Full Output Drive 16 mA Sink, 2.0 mA Source
- Fast Access Time Guaranteed for Worst-Case N² Sequencing, Over Commercial Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Operating Supply Voltage	Vcc	+7.0	Vdc
Input Voltage	Vin	+5.5	Vdc
Operating Output Voltage	Voн	+7.0	Vdc
Supply Current	Icc	650	mAdd
Input Current	lin	-20	mAdd
Output Sink Current	l _o	100	mAdd
Operating Temperature Range MCM7621xxx	ТА	0 to +75	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Maximum Junction Temperature	TJ	+175	°C

NOTE:

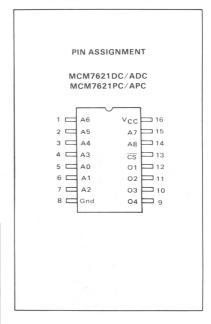
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

MCM7621 MCM7621A

TTL

2048-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7621,A — 512 × 4 THREE-STATE



GUARANTEED OPERATING RANGE (TA = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	Vcc	4.75	5.0	5.25	Vdc
Input High Voltage	VIH	2.0	_	_	Vdc
Input Low Voltage	VIL	_	_	0.8	Vdc

C OPERATING CONDITIONS AND CHARACTERISTICS				Th			
Symbol	Paramete	r	Test Conditions	Min	Тур	Max	Unit
I _{IH}	Address/Enable Input Current	"1"	V _{IH} = V _{CC} Max V _{IL} = 0.45 V	1 -	_ -0.1	40 -0.25	μAdc mAdc
V _{OH} V _{OL}	Output Voltage	"1" "0"	I_{OH} = -2.0 mA, V_{CC} Min I_{OL} = +16 mA, V_{CC} Min	2.4	3.4 0.35	0.45	Vdc Vdc
IOHE IOLE	Output Disabled Current	1	V _{OH} = +5.25 V, V _{CC} Max V _{OL} = +0.3 V, V _{CC} Max		7	40 -40	μAdc μAdc
VIK	Input Clamp Voltage		I _{in} = -18 mA	_	_	-1.2	Vdc
los	Output Short Circuit	Current	V _{CC} Max, V _{out} = 0.0 V One Output Only for 1.0 s Max	-15	_	-70	mAdc
Icc	Power Supply Curre	nt	V _{CC} Max All Inputs Grounded	_	60	100	mAdc

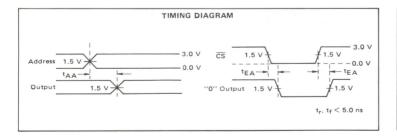
CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

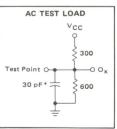
Characteristic	Symbol	Тур	Unit
Input Capacitance	Cin	8.0	pF
Output Capacitance	C _{out}	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature)

	4	MCM	MCM7621		MCM7621A	
		0 to +75°C		0 to +75°C		
Characteristic	Symbol	Тур	Max	Тур	Max	Unit
Address to Output Access Time	tAA	45	70	45	60	ns
Chip Enable Access Time	tEA	15	25	15	25	ns

NOTE: AC limits guaranteed for worst case N² sequential with maximum test frequency of 5.0 MHz.





*Includes Scope and Test Fixture Capacitance

7

The PROMs are manufactured with all bits/outputs Logical "11" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

- Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM
- Disable the chip by applying input high (V_{IH}) to the CS input. CS input must remain at V_{IH} for programming. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
- Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
- 4. Raise VCC to VpH with rise time equal to tr.
- After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPF} and duration of t_n to the output selected

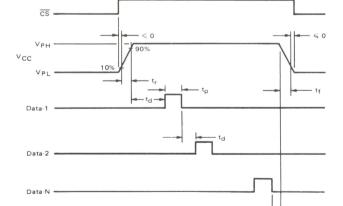
- for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
- 6. Other bits in the same word may be programmed while the V_{CC} input is raised to VPH by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t₁₄.
- Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
- 8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the CS input.
- 9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
- Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
- 11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occured.

TABLE 1 — PROGRAMMING SPECIFICATIONS

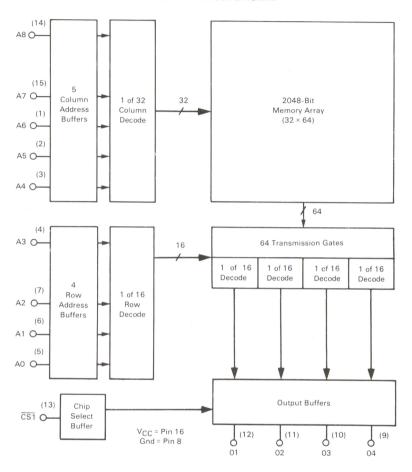
Symbol	Parameter	Min	Тур	Max	Unit
V _{IH} V _{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V
V _{PL}	Programming/Verify Voltage to VCC	11.75 4.5	12.0 4.5	12.25 5.5	V
ICCP	Programming Voltage Current Limit with VPH Applied	600	600	650	mA
t _r	Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 10	μs μs
t _d	Programming Delay	10	10	100	μS
tp	Programming Pulse Width	100	_	1000	μs
DC	Programming Duty Cycle	_	50	90	%
V _{OPE} V _{OPD}	Output Voltage Enable Disable (2)	10.0 4.5	10.5 5.0	11.0 5.5	V
IOPE	Output Voltage Enable Current	2.0	4.0	10	mA
TA	Ambient Temperature	_	25	75	°C

FIGURE 1 - TYPICAL PROGRAMMING WAVEFORMS

- (1) Address and chip select should not be left open for VIH.
- (2) Disable condition will be met with output open circuit.



MCM7621/21A BLOCK DIAGRAM





4096-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7641 and MCM7641A, together with various other 76xx series TTL PROMS, comprise a complete and compatible family having common de electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

All pinouts are compatible to industry-standard PROMs and ROMs

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1.0 Second per 1024 Bits, Typical)
- Expandable Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
 Low Input Current 250 μA Logic "0", 40 μA Logic "1"
 Full Output Drive 16 mA Sink, 2.0 mA Source
- Fast Access Time Guaranteed for Worst-Case N² Sequencing, Over Commercial Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

ABSOLUTE MAXIMUM RATINGS (See Note)

Symbol	Value	Unit
Vcc	+7.0	Vdc
Vin	+5.5	Vdc
Voн	+7.0	Vdc
Icc	650	mAdo
lin	-20	mAdo
Io	100	mAdc
ТА	0 to +75	°C
T _{stg}	-55 to +150	°C
TJ	+175	°C
	VCC Vin VOH ICC Iin Io TA	VCC +7.0 Vin +5.5 VOH +7.0 ICC 650 Iin -20 Io 100 TA 0 to +75 Tstg -55 to +150

NOTE

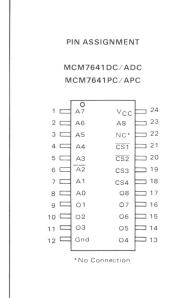
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

MCM7641 MCM7641A

TTI

4096-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7641,A — 512 × 8 THREE-STATE



GUARANTEED OPERATING RANGE (TA = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	VCC	4.75	5.0	5.25	Vdc
Input High Voltage	VIH	2.0	_	_	Vdc
Input Low Voltage	VIL	_	_	0.8	Vdc

DC OPERATING CONDITIONS AND CHARACTERISTICS

Three-State Output

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
I _{IH}	Address/Enable "1 Input Current "0	I AIH - ACC INIAX	=======================================	-0.1	40 -0.25	μAdc mAdc
V _{OL}	Output Voltage "1	IOH = -2.0 mA, VCC MIN	2.4	3.4 0.35	0.45	Vdc Vdc
IOHE IOLE	Output Disabled '11 Current '10	VOH - 13.23 V, VCC WIAX	_	_	40 -40	μAdc μAdc
VIK	Input Clamp Voltage	I _{in} = -18 mA	_	_	-1.2	Vdc
los	Output Short Circuit Curre	V _{CC} Max, V _{out} = 0.0 V One Output Only for 1.0 s Max	-15	_	-70	mAdc
Icc	Power Supply Current	V _{CC} Max All Inputs Grounded	_	60	140	mAdc

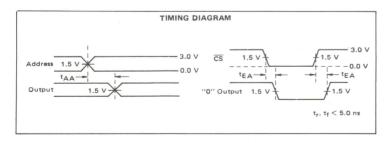
CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

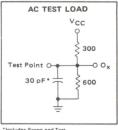
Characteristic	Symbol	Тур	Unit
Input Capacitance	Cin	8,0	pF
Output Capacitance	C _{out}	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature)

		MCM7641 0 to +75°C				
Characteristic	Symbol	Тур	Max	Тур	Max	Unit
Address to Output Access Time	tAA	45	70	45	60	ns
Chip Enable Access Time	tEA	30	40	30	40	ns

NOTE: AC limits guaranteed for worst case N² sequential with maximum test frequency of 5.0 MHz.





*Includes Scope and Test Fixture Capacitance

7

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

- Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
- Disable the chip by applying input high (V_{IH}) to the CS input. CS input must remain at V_{IH} for programming. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
- Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
- 4. Raise $V_{\mbox{CC}}$ to $V_{\mbox{PH}}$ with rise time equal to $t_{\mbox{r}}$
- 5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPF} and duration of t_D to the output selected

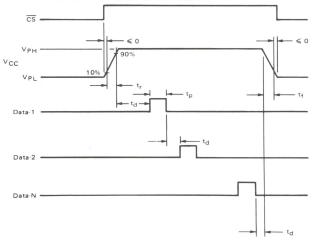
- for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
- Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t₄.
- Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
- Enable the PROM for verification by applying a logic "O"
 (V_{IL}) to the CS input.
- 9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
- Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
- 11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occured.

TABLE 1 — PROGRAMMING SPECIFICATIONS

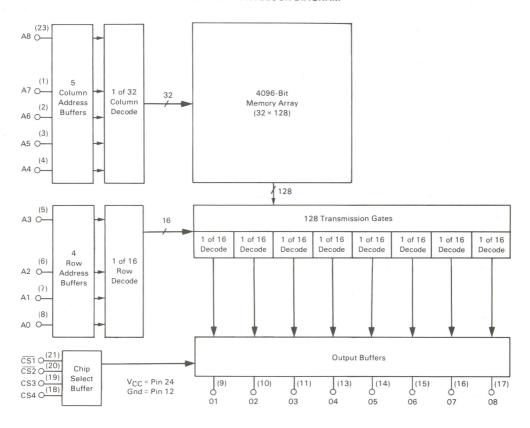
Symbol	Parameter	Min	Тур	Max	Unit
V _{IH} V _{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V
V _{PH} V _{PL}	Programming/Verify Voltage to VCC	11.75 4.5	12.0 4.5	12.25 5.5	V
ICCP	Programming Voltage Current Limit with VPH Applied	600	600	650	mA
t _r .	Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 10	μS μS
t _d	Programming Delay	10	10	100	μS
tp	Programming Pulse Width	100	_	1000	μS
DC	Programming Duty Cycle	_	50	90	%
VOPE VOPD	Output Voltage Enable Disable (2)	10.0 4.5	10.5 5.0	11.0 5.5	V
IOPE	Output Voltage Enable Current	2.0	4.0	10	mA
TA	Ambient Temperature	_	25	75	°C

- (1) Address and chip select should not be left open for VIH.
- (2) Disable condition will be met with output open circuit.

FIGURE 1 - TYPICAL PROGRAMMING WAVEFORMS



MCM7641/41A BLOCK DIAGRAM





4096-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7643 and MCM7643A, together with various other 76xx series TTL PROMS, comprise a complete and compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

All pinouts are compatible to industry-standard PROMs and ROMs.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1.0 Second per 1024 Bits, Typical)
- Expandable Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
 Low Input Current 250 μA Logic "0", 40 μA Logic "1"

 Full Output Drive 16 mA Sink, 2.0 mA Source
- Fast Access Time Guaranteed for Worst-Case N² Sequencing, Over Commercial Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Operating Supply Voltage	Vcc	+7.0	Vdc
Input Voltage	Vin	+5.5	Vdc
Operating Output Voltage	Voн	+7.0	Vdc
Supply Current	lcc	650	mAdc
Input Current	lin	-20	mAdc
Output Sink Current	Io	100	mAdc
Operating Temperature Range MCM7643xxx	TA	0 to +75	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Maximum Junction Temperature	TJ	+175	°C

NOTE

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

MCM7643 MCM7643A

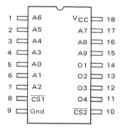
TTL

4096-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7643,A — 1024 × 4 THREE-STATE

PIN ASSIGNMENT

MCM7643DC/ADC MCM7643PC/APC



GUARANTEED OPERATING RANGE (T_A = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	VCC	4.75	5.0	5.25	Vdc
Input High Voltage	VIH	2.0	_	_	Vdc
Input Low Voltage	VIL	_	_	0.8	Vdc

OC OPERATING CONDITIONS AND CHARACTERISTICS		Thr					
Symbol	Paramete	r	Test Conditions	Min	Тур	Max	Unit
I _{IH}	Address/Enable Input Current	''1'' ''0''	V _{IH} = V _{CC} Max V _{IL} = 0.45 V	_	-0.1	40 -0.25	μAdc mAdc
V _{OH}	Output Voltage	''1'' ''0''	I_{OH} = -2.0 mA, V_{CC} Min I_{OL} = +16 mA, V_{CC} Min	2.4	3.4 0.35	0.45	Vdc Vdc
I _{OHE}	Output Disabled Current	''1'' ''0''	V _{OH} = +5.25 V, V _{CC} Max V _{OL} = +0.3 V, V _{CC} Max	_	_	40 -40	μAdc μAdc
VIK	Input Clamp Voltage		I _{in} = -18 mA	_	_	-1.2	Vdc
los	Output Short Circuit	Current	V _{CC} Max, V _{out} = 0.0 V One Output Only for 1.0 s Max	-15	-	-70	mAdc
lcc	Power Supply Currer	it	V _{CC} Max All Inputs Grounded	_	100	140	mAdc

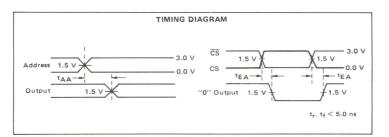
CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

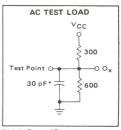
Characteristic	Symbol	Тур	Unit
Input Capacitance	Cin	8.0	pF
Output Capacitance	C _{out}	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature)

		MCM	17643	MCM7643A			
		0 to +75°C		0 to +75°C			
Characteristic	Symbol	Тур	Max	Тур	Max	Unit	
Address to Output Access Time	tAA	50	70	40	50	ns	
Chip Enable Access Time	tEA	25	30	25	30	ns	

NOTE: AC limits guaranteed for worst case N² sequential with maximum test frequency of 5.0 MHz.





*Includes Scope and Tes Fixture Capacitance

MCM7643/MCM7643A

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

- Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM
- Disable the chip by applying input high (V_{IH}) to the CS input. CS input must remain at V_{IH} for programming. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
- Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
- 4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
- 5. After a delay equal to or greater than t_d , apply a pulse with amplitude of V_{OPE} and duration of t_D to the output selected

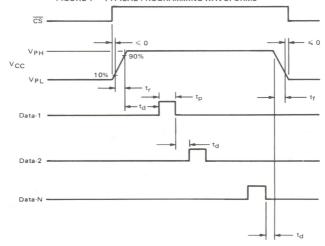
- for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
- Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t₄.
- Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
- Enable the PROM for verification by applying a logic "0" (V_{IL}) to the CS input.
- 9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
- Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
- 11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occured.

TABLE 1 - PROGRAMMING SPECIFICATIONS

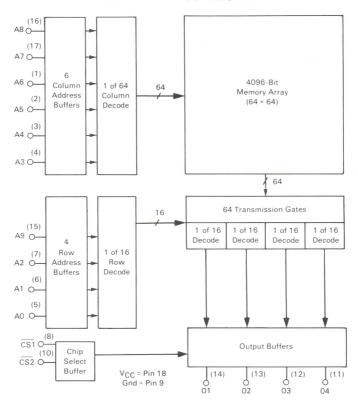
Symbol	Parameter	Min	Тур	Max	Unit
V _{IH} V _{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V
V _{PH} V _{PL}	Programming/Verify Voltage to VCC	11.75 4.5	12.0 4.5	12.25 5.5	V
ICCP	Programming Voltage Current Limit with V _{PH} Applied	600	600	650	mA'
t _r	Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 10	μs μs
t _d	Programming Delay	10	10	100	μS
tp	Programming Pulse Width	100	_	1000	μS
DC	Programming Duty Cycle	_	50	90	%
V _{OPE} V _{OPD}	Output Voltage Enable Disable (2)	10.0 4.5	10.5 5.0	11.0 5.5	V
IOPE	Output Voltage Enable Current	2.0	4.0	10	mA
TA	Ambient Temperature	_	25	75	°C

- (1) Address and chip select should not be left open for VIH.
- (2) Disable condition will be met with output open circuit.

FIGURE 1 - TYPICAL PROGRAMMING WAVEFORMS



MCM7643/43A BLOCK DIAGRAM





8192-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7681 and MCM7681A, together with various other 76xx series TTL PROMS, comprise a complete and compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

Pinouts are compatible to industry-standard PROMs and ROMs. In addition, the MCM7681 is a pin compatible replacement for the 512×8 with Pin 22 connected as A9 on the 1024×8 .

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1.0 Second per 1024 Bits, Typical)
- Expandable Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
 Low Input Current 250 μA Logic "0", 40 μA Logic "1"

 Full Output Drive 16 mA Sink, 2.0 mA Source
- Fast Access Time Guaranteed for Worst-Case N² Sequencing, Over Commercial Temperature Ranges and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Operating Supply Voltage	Vcc	+7.0	Vdc
Input Voltage	Vin	+5.5	Vdc
Operating Output Voltage	Voн	+7.0	Vdc
Supply Current	¹cc	650	m Add
Input Current	lin	-20	mAdd
Output Sink Current	I _o	100	m Add
Operating Temperature Range MCM7681xxx	ТА	0 to +75	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Maximum Junction Temperature	TJ	+175	°C

NOTE

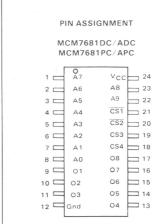
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

MCM7681 MCM7681A

TTL

8192-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7681,A - 1024 × 8 THREE-STATE



MCM7681/MCM7681A

GUARANTEED OPERATING RANGE (TA = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	Vcc	4.75	5.0	5.25	Vdc
Input High Voltage	VIH	2.0	_	_	Vdc
Input Low Voltage	VIL	_	_	0.8	Vdc

DC OPER	PERATING CONDITIONS AND CHARACTERISTICS		Thi				
Symbol	Paramete	r	Test Conditions	Min	Тур	Max	Unit
I _{IH}	Address/Enable Input Current	''1''	V _{IH} = V _{CC} Max V _{IL} = 0.45 V	_	 -0.1	40 -0.25	μAdc mAdc
V _{OH} V _{OL}	Output Voltage	"1" "0"	I _{OH} = -2.0 mA, V _{CC} Min I _{OL} = +16 mA, V _{CC} Min	2.4	3.4 0.35	0.45	Vdc Vdc
OHE	Output Disabled Current	''1'' ''0''	V _{OH} = +5.25 V, V _{CC} Max V _{OL} = +0.3 V, V _{CC} Max	_	_	40 -40	μAdc μAdc
VIK	Input Clamp Voltage		I _{in} = -18 mA	_	_	-1.2	Vdc
los	Output Short Circuit	Current	V _{CC} Max, V _{out} = 0.0 V One Output Only for 1.0 s Max	-15	_	-70	mAdc
Icc	Power Supply Curren	it	V _{CC} Max All Inputs Grounded	_	110	150	mAdc

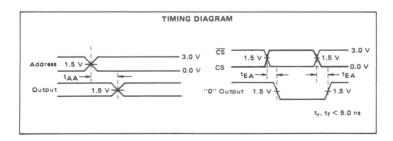
CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

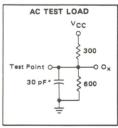
Characteristic	Symbol	Тур	Unit
Input Capacitance	Cin	8.0	pF
Output Capacitance	C _{out}	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature)

		MCM7681 0 to +75°C		MCM7681A 0 to +75°C		
						1
Characteristic	Symbol	Тур	Max	Тур	Max	Unit
Address to Output Access Time	tAA	_	70	_	50	ns
Chip Enable Access Time	t _{EA}	30	40	30	40	ns

NOTE: AC limits guaranteed for worst case N² sequential with maximum test frequency of 5.0 MHz.





*Includes Scope and Test Fixture Capacitance

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "11" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

- Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
- Disable the chip by applying input high (V_{IH}) to the CS input. CS input must remain at V_{IH} for programming. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
- Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
- Raise V_{CC} to V_{PH} with rise time equal to t_r.
- 5. After a delay equal to or greater than t_d , apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected

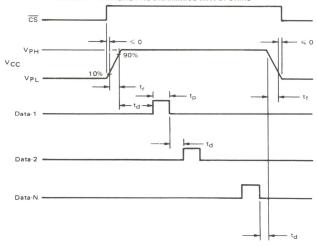
- for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
- Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_f.
- 7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
- Enable the PROM for verification by applying a logic "O" (V_{IL}) to the CS input.
- 9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
- Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
- 11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occured.

TABLE 1 - PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Тур	Max	Unit
V _{IH} V _{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V
V _{PH} V _{PL}	Programming/Verify Voltage to VCC	11.75 4.5	12.0 4.5	12.25 5.5	V
ICCP	Programming Voltage Current Limit with VpH Applied	600	600	650	mA
t _r t _f	Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 10	μs μs
t _d	Programming Delay	10	10	100	μS
tp	Programming Pulse Width	100	_	1000	μS
DC	Programming Duty Cycle	_	50	90	%
V _{OPE} V _{OPD}	Output Voltage Enable Disable (2)	10.0 4.5	10.5 5.0	11.0 5.5	V
IOPE	Output Voltage Enable Current	2.0	4.0	10	mA
TA	Ambient Temperature	_	25	75	°C

- (1) Address and chip select should not be left open for VIH.
- (2) Disable condition will be met with output open circuit.

FIGURE 1 - TYPICAL PROGRAMMING WAVEFORMS



MCM7681/81A BLOCK DIAGRAM (22)A9 O-(23) A8 O-((1) 6 A7 0-8192-Bit Column 1 of 64 64 Memory Array Address Column (2) (64 × 128) Buffers Decode A6 O-(3) A5 O-(4) A4 O-128 128 Transmission Gates 16 1 of 16 1 of 16 1 of 16 1 of 16 1 of 16 1 of 16 1 of 16 1 of 16 A3 O-Decode Decode Decode Decode Decode Decode Decode Decode 4 (6) Row 1 of 16 Address A2 O-Row Buffers Decode (7) A1 O-(8) A0 O- $\frac{\overline{CS1}}{\overline{CS2}} \circ \frac{(21)}{(20)}$ $CS3 \circ \frac{(19)}{(18)}$ **Output Buffers** Chip (9) 01 Select V_{CC} = Pin 24 Gnd = Pin 12 (11) (10) (13) (14) (15) (16) (17) CS4 O (18) Buffer 02 03 04 05 06 07 08



8192-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7685 and MCM7685A, together with various other 76xx series TTL PROMS, comprise a complete and compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable PROMs and are available in commonly used organizations, with three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

Pinouts are compatible to industry-standard PROMs and ROMs. The MCM7685 is a pin compatible replacement for the 1024×4 organization with Pin 8 connected as A10 on the 2048×4 .

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1.0 Second per 1024 Bits, Typical)
- Expandable Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
 Low Input Current 250 μA Logic "0", 40 μA Logic "1"
 Full Output Drive 16 mA Sink, 2.0 mA Source
- Fast Access Time Guaranteed for Worst-Case N² Sequencing, Commercial Temperature Ranges and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Operating Supply Voltage	Vcc	+7.0	Vdc
Input Voltage	Vin	+5.5	Vdc
Operating Output Voltage	Voн	+7.0	Vdc
Supply Current	lcc	650	mAdo
Input Current	lin	-20	mAdo
Output Sink Current	Io	100	mAdo
Operating Temperature Range MCM7685xxx	ТД	0 to +75	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Maximum Junction Temperature	TJ	+175	°C

NOTE

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

MCM7685 MCM7685A

TTL

8192-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7685,A — 2048 × 4 THREE-STATE

PIN ASSIGNMENT MCM7685DC/ADC MCM7685PC/APC V_{CC} 18 1 H A6 2 A5 A8 16 3 A4 4 C A3 A9 15 5 A AO 01 14 02 13 6 🖂 A 1 7 🗖 A2 03 12 04 11 8 A10 Gnd CS 10 9 🗆

GUARANTEED OPERATING RANGE (TA = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	Vcc	4.75	5.0	5.25	Vdc
Input High Voltage	VIH	2.0	_	_	Vdc
Input Low Voltage	VIL	_	_	0.8	Vdc

OC OPERATING CONDITIONS AND CHARACTERISTICS		The					
Symbol	Paramete	er	Test Conditions	Min	Тур	Max	Unit
IIH IIL	Address/Enable Input Current	"1"	V _{IH} = V _{CC} Max V _{IL} = 0.45 V	_	-0.1	40 -0.25	μAdc mAdc
V _{OH}	Output Voltage	"1" "0"	I _{OH} = -2.0 mA, V _{CC} Min I _{OL} = +16 mA, V _{CC} Min	2.4	3.4 0.35	0.45	Vdc Vdc
I _{OHE}	Output Disabled Current	"1" "0"	V _{OH} = +5.25 V, V _{CC} Max V _{OL} = +0.3 V, V _{CC} Max	_	_	40 -40	μAdc μAdc
VIK	Input Clamp Voltage		I _{in} = -18 mA	_	_	-1.2	Vdc
los	Output Short Circuit	Current	V _{CC} Max, V _{out} = 0.0 V One Output Only for 1.0 s Max	-15	-	-70	mAdc
ICC	Power Supply Curre	nt	V _{CC} Max All Inputs Grounded	_	80	150	mAdc

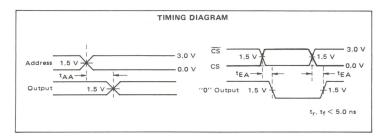
CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

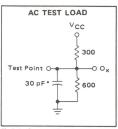
Characteristic	Symbol	Тур	Unit
Input Capacitance	Cin	8.0	pF
Output Capacitance	C _{out}	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature)

		MCM7685 0 to +75°C		MCM7685A 0 to +75°C		
Characteristic	Symbol	Тур	Max	Тур	Max	Unit
Address to Output Access Time	†AA	45	70	40	55	ns
Chip Enable Access Time	tEA	30	40	30	40	ns

NOTE: AC limits guaranteed for worst case N^2 sequential with maximum test frequency of 5.0 MHz.





*Includes Scope and Test Fixture Capacitance

MCM7685/MCM7685A

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

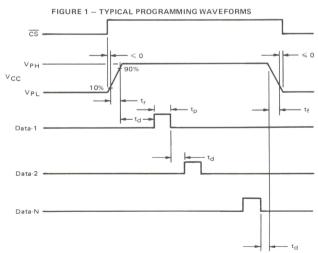
- Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
- Disable the chip by applying input high (V_{IH}) to the CS input. CS input must remain at V_{IH} for programming. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
- Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
- 4. Raise VCC to VPH with rise time equal to tr.
- 5. After a delay equal to or greater than t_d , apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected

- for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
- Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_t.
- Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
- 8. Enable the PROM for verification by applying a logic "0" (VIL) to the CS input.
- 9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
- Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
- 11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occured.

TABLE 1 — PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Тур	Max	Unit
V _{IH} V _{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V
V _{PH} V _{PL}	Programming/Verify Voltage to VCC	11.75 4.5	12.0 4.5	12.25 5.5	V V
ICCP	Programming Voltage Current Limit with VPH Applied	600	600	650	mA
t _r	Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 10	μs μs
td	Programming Delay	10	10	100	μS
tp	Programming Pulse Width	100	_	1000	μS
DC	Programming Duty Cycle	_	50	90	%
VOPE VOPD	Output Voltage Enable Disable (2)	10.0 4.5	10.5 5.0	11.0 5.5	V
IOPE	Output Voltage Enable Current	2.0	4.0	10	mA
TA	Ambient Temperature	_	25	75	°C

- (1) Address and chip select should not be left open for VIH.
- (2) Disable condition will be met with output open circuit.



MCM7685/85A BLOCK DIAGRAM (15) A9 O-(16)A8 O_ (17) 6 A7 O-8192-Bit Column 1 of 64 64 Memory Array (64 × 128) Address Column (1) Buffers Decode A6 O-(2) A5 O-(3) A4 O-128 A10 (8) 128 Transmission Gates 32 1 of 32 1 of 32 1 of 32 1 of 32 A2 O-Decode Decode Decode Decode Row 1 of 32 (6) A1 Ò-Address Row Buffers Decode A0 O-(4) A3 O-Output Buffers (10)Chip (11) O 04 CS O-Select Buffer (14) O 01 V_{CC} = Pin 18 Gnd = Pin 9 (12) 03 (13)

02



16384-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM76161 and MC76161A, together with various other 76xx series TTL PROMS, comprise a complete and compatible family having common de electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time.

Pinouts are compatible to industry-standard PROMs and ROMs. The MCM76161 is a pin compatible replacement for the 1024×8 with Pin 21 connected as A10 on the 2048×8 .

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1.0 Second per 1024 Bits, Typical)
- Expandable Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
 Low Input Current 250 μA Logic "0", 40 μA Logic "1"
 Full Output Drive 16 mA Sink, 2.0 mA Source
- Fast Access Time Guaranteed for Worst-Case N² Sequencing, Over Commercial Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Operating Supply Voltage	Vcc	+7.0	Vdc
Input Voltage	Vin	+5.5	Vdc
Operating Output Voltage	Voн	+7.0	Vdc
Supply Current	lcc	650	mAdo
Input Current	lin	-20	mAdd
Output Sink Current	Io	100	mAdd
Operating Temperature Range MCM76161xxx	ТА	0 to +75	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Maximum Junction Temperature	TJ	+175	°C

Note:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

MCM76161 MCM76161A

TTL

16384-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM76161,A — 2048 × 8 THREE-STATE

PIN ASSIGNMENT

MCM76161DC/ADC MCM76161PC/APC



GUARANTEED OPERATING RANGE (T_A = 0°C to +75°C)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	VCC	4.75	5.0	5.25	Vdc
Input High Voltage	VIH	2.0	_	-	Vdc
Input Low Voltage	V _{IL}	_	_	0.8	Vdc

C OPER	C OPERATING CONDITIONS AND CHARACTERISTICS			Three-State Output			
Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit	
IH IIL	Address/Enable "1" Input Current "0"	AIH ACC MAY		 -0.1	40 -0.25	μAdc mAdc	
V _{OL}	Output Voltage "1"	10H5.0 HIM, ACC MILL	2.4	3.4 0.35	0.45	Vdc Vdc	
IOHE IOLE	Output Disabled "1" Current "0"	TOH OLEG T, TCC Max	_	_	40 -40	μAdc μAdc	
VIK	Input Clamp Voltage	I _{in} = -18 mA	_	_	-1.2	Vdc	
los	Output Short Circuit Curren	V _{CC} Max, V _{out} = 0.0 V One Output Only for 1.0 s Max	-15	-	-70	mAdc	
Icc	Power Supply Current	V _{CC} Max All Inputs Grounded	_	130	180	mAdc	

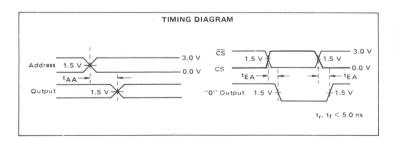
CAPACITANCE (f = 1.0 MHz, $T_A = 25$ °C, periodically sampled rather than 100% tested.)

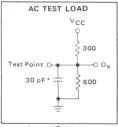
Characteristic	Symbol	Тур	Unit
Input Capacitance	C _{in}	8.0	pF
Output Capacitance	C _{out}	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature)

	MCM7616		76161	MCM76161A		
		0 to +	75°C	0 to +	- 75 °C	
Characteristic	Symbol	Тур	Max	Тур	Max	Unit
Address to Output Access Time	†AA	45	70	35	60	ns
Chip Enable Access Time	t _{EA}	30	40	30	40	ns

NOTE: AC limits guaranteed for worst case N² sequential with maximum test frequency of 5.0 MHz.





*Includes Scope and Test Fixture Capacitance

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "O" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

- 1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
- 2. Disable the chip by applying input high (VIH) to the CS input. CS input must remain at VIH for programming. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
- 3. Disable the programming circuitry by applying an Output Voltage Disable of less than VOPD to the output of the PROM. The output may be left open to achieve the disable.
- 4. Raise VCC to VpH with rise time equal to tr.
- 5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_D to the output selected

- for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
- 6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of td.
- 7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
- Enable the PROM for verification by applying a logic "O" (VII) to the CS input.
- 9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulse of durations shorter than 1.0 ms may be used to enhance programming speed.
- 10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
- 11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occured.

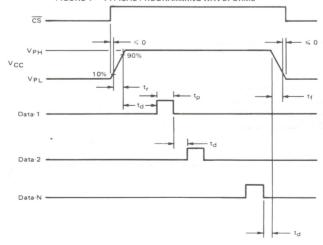
TABLE 1 - PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Тур	Max	Unit
V _{IH} V _{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V
V _{PH} V _{PL}	Programming/Verify Voltage to VCC	11.75 4.5	12.0 4.5	12.25 5.5	V
ICCP	Programming Voltage Current Limit with VpH Applied	600	600	650	mA
t _r	Voltage Rise and Fall Time	1.0	1.0 1.0	10	μs μs
td	Programming Delay	10	10	100	μS
tp	Programming Pulse Width	100	<u> </u>	1000	μS
DC	Programming Duty Cycle	_	50	90	%
V _{OPE} V _{OPD}	Output Voltage Enable Disable (2)	10.0 4.5	10.5 5.0	11.0 5.5	V
IOPE	Output Voltage Enable Current	2.0	4.0	10	mA
TA	Ambient Temperature		25	75	°C

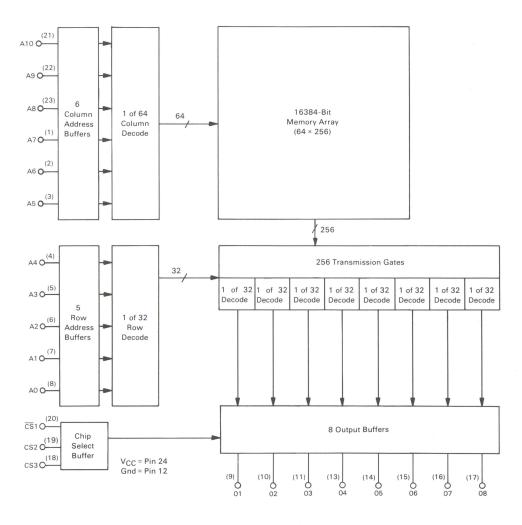
⁽¹⁾ Address and chip select should not be left open for VIH

⁽²⁾ Disable condition will be met with output open circuit





MCM76161/161A BLOCK DIAGRAM





1024-BIT RANDOM ACCESS MEMORY

The MCM93415 is a 1024-bit Read/Write RAM organized 1024 words by 1 bit.

The MCM93415 is designed for buffer control storage and high performance main memory applications, and has a typical access time of $35\,\mathrm{ns}$.

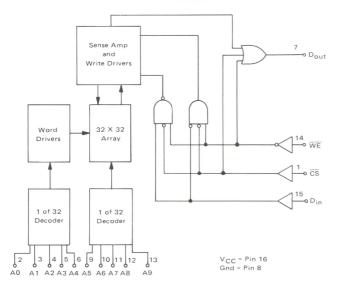
The MCM93415 has full decoding on-chip, separate data input and data output lines, and an active low chip select. The device is fully compatible with standard DTL and TTL logic families and features an uncommitted collector output for ease of memory expansion.

- Uncommitted Collector Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed —

Access Time – 35 ns Typical Chip Select – 15 ns Typical

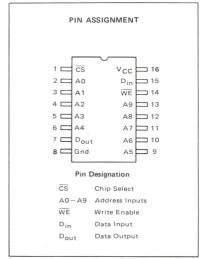
- Power Dissipation Decreases with Increasing Temperature
- Power Dissipation 0.5 mW/Bit Typical
- Organized 1024 Words X 1 Bit

BLOCK DIAGRAM



MCM93415

TTL 1024 X 1 BIT RANDOM ACCESS MEMORY



Z

FUNCTIONAL DESCRIPTION

The MCM93415 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The Chip Select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of Chip Select $\overline{(\text{CS})}$ from the address without affecting system performance.

The read and write operations are controlled by the state of the active low Write Enable (WE, Pin 14). With WE held low and the chip selected, the data at $D_{\rm in}$ is written into the addressed location. To read, WE is held high and the chip selected. Data in the specified location is presented at $D_{\rm OU}$ and is non-inverted.

Uncommitted collector outputs are provided to allow wired-OR applications. In any application an external pull-up resistor of RL value must be used to provide a high at the output when it is off. Any RL value within the range specified below may be used.

 $\frac{\mathsf{V}_{\mathsf{CC}}(\mathsf{Min})}{\mathsf{I}_{\mathsf{OL}} - \mathsf{FO}(1.6)} \leqslant \mathsf{R}_{\mathsf{L}} \leqslant \frac{\mathsf{V}_{\mathsf{CC}}(\mathsf{Min}) - \mathsf{V}_{\mathsf{OH}}}{\mathsf{n}(\mathsf{I}_{\mathsf{CEX}}) + \mathsf{FO}(0.04)}$

R $_{\mathsf{L}}$ is in $\mathsf{k}\Omega$

n = number of wired-OR outputs tied together

FO = number of TTL Unit Loads (UL) driven

ICEX = Memory Output Leakage Current

VOH = Required Output High Level at Output Node

IOL = Output Low Current

The minimum R $_{\rm L}$ value is limited by output current sinking ability. The maximum R $_{\rm L}$ value is determined by the output and input leakage current which must be supplied to hold the output at $V_{\rm OH}$. One Unit Load = 40 μ A High/1.6 mA Low.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	FF00 - 140F00
Ceramic Package (D and F Suffix)	-55°C to +165°C
Plastic Package (P Suffix)	-55°C to +125°C
Operating Junction Temperature, TJ	
Ceramic Package (D and F Suffix)	< 165°C
Plastic Package (P Suffix)	< 125°C
V _{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage (dc)	-0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	-0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	-12 mA to +5.0 mA

TRUTH TABLE

	Inputs		Output	
CS	WE	Din	Open Collector	Mode
Н	×	×	Н	Not Selected
L	L	L	Н	Write "0"
L	L	Н	Н	Write "1"
L	Н	×	Dout	Read

H = High Voltage Level

L = Low Voltage Level

X = Don't Care (High or Low)

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

GUARANTEED OPERATING RANGES (Note 2)

	Supply Voltage (V _{CC})			
Part Number	Min	Nom	Max	Ambient Temperature (TA)
MCM93415DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
MCM93415FM, DM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

		Limits			
Symbol	Characteristic	Min	Max	Unit	Conditions
VOL	Output Low Voltage		0.45	Vdc	V _{CC} = Min, I _{OL} = 16 mA
VIH	Input High Voltage	2.1		Vdc	Guaranteed Input High Voltage for All Inputs
VIL	Input Low Voltage		0.8	Vdc	Guaranteed Input Low Voltage for All Inputs
IIL	Input Low Current		-400	μAdc	V _{CC} = Max, V _{in} = 0.4 V
ΊΗ	Input High Current		40	μAdc	V _{CC} = Max, V _{in} = 4.5 V
			1.0	mAdc	V _{CC} = Max, V _{in} = 5.25 V
ICEX	Output Leakage Current		100	μAdc	V _{CC} = Max, V _{out} = 4.5 V
V _{CD}	Input Diode Clamp Voltage		-1.5	Vdc	V _{CC} = Max, I _{in} = -10 mA
Icc	Power Supply Current		130	mAdc	T _A = Max
			155	mAdc	$T_A = 0^{\circ}C$ $V_{CC} = Max$, All Inputs Grounded
			170	mAdc	T _A = Min

7

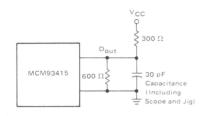
AC OPERATING CONDITIONS AND CHARACTERISTICS

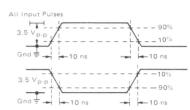
(Full operating voltage and temperature unless otherwise noted)

AC TEST LOAD AND WAVEFORM

Loading Condition

Input Pulses



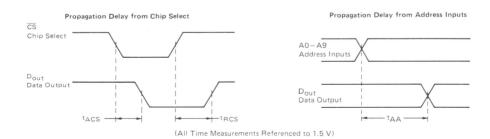


		MCM934	15DC,PC	MCM934	15DM, FM		
Symbol	Characteristic (Notes 2, 3)	Min	Max	Min	Max	Unit	Conditions
READ MODE	DELAY TIMES					ns	
†ACS	Chip Select Time		35		45		See Test Circuit
†RCS	Chip Select Recovery Time		35		50		and Waveforms
t _{AA}	Address Access Time		45		60		
WRITE MODE	DELAY TIMES					ns	
tws	Write Disable Time		35		45		See Test Circuit
twR	Write Recovery Time		40		50		and Waveforms
	INPUT TIMING REQUIREMENTS					ns	
tw	Write Pulse Width (to guarantee write)	30		40			See Test Circuit
twsp	Data Setup Time Prior to Write	5		5			and Waveforms
twhD	Data Hold Time After Write	5		5			
twsa	Address Setup Time (at t _W = Min)	10		15			
twha .	Address Hold Time	10		10			
twscs	Chip Select Setup Time	5		5			
^t WHCS	Chip Select Hold Time	5		5			

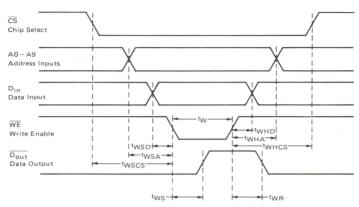
NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air. Contact your Motorola Sales Representative if extended temperature or modified operating conditions are desired.

NOTE 3: The AC limits are guaranteed to be the worst case bit in the memory.

READ OPERATION TIMING DIAGRAM



WRITE CYCLE TIMING



(All Time Measurements Referenced to 1.5 V)

	θ JA (Junction	n to Ambient)	
Package	Blown Still (θ JC (Junction to Case)
D Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15 ⁰ C/W
P Suffix	65°C/W	100°C/W	25°C/W

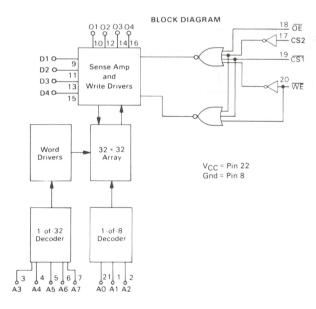


1024-BIT RANDOM ACCESS MEMORY

The MCM93422/MCM93L422 are 1024-bit Read/Write RAMs, organized 256 words by 4 bits, designed for high performance main memory and control storage applications.

They have full decoding on-chip, separate data input and data output lines, an active low-output enable, write enable, and two chip selects, one active high, one active low. These memories are fully compatible with standard TTL logic families. A three-state output is provided to drive bus-organized systems and/or highly capacitive loads.

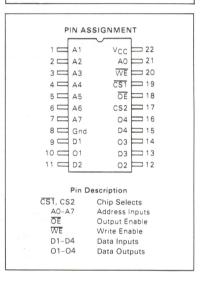
- Three-State Outputs
- TTL Inputs and Outputs
- Non-Inverting Data Outputs
- High Speed —
 Access Time 30 ns Typical
 Chip Select 15 ns Typical
- Power Dissipation 0.26 mW/Bit Typical
- Standard 22-Pin, 400 Mil Wide Package
- Power Dissipation Decreases with Increasing Temperature
- Organized 256 Words × 4 Bits
- Two Chip Select Lines for Memory Expansion



MCM93422 MCM93L422

TTL 256 × 4-BIT RANDOM ACCESS MEMORY

MCM93422 — THREE-STATE MCM93L422 — THREE-STATE



FUNCTIONAL DESCRIPTION

The MCM93422/MCM93L422 are fully decoded 1024-bit random access memories organized 256 words by 4 bits. Word selections are achieved by means of an 8-bit address, A0-A7.

The Chip Select ($\overline{\text{CS1}}$ and CS2) inputs provide for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active low Write Enable (\overline{WE} , Pin 20). With \overline{WE} and $\overline{CS1}$ held low and the CS2 held high, the data at Dn is written into the addressed location. To read, \overline{WE} and CS2 are held high and $\overline{CS1}$ is held low. Data in the specified location is presented at the output (O1–O4) and is non-inverted.

The three-state outputs of the MCM93422/MCM93L422 provide drive capability for higher speeds with capacitive load systems. The third state (high impedance) allows bus-organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in a high-impedance state.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature Ceramic Package (D Suffix) Plastic Package (P Suffix)	-65°C to +150°C -55°C to +125°C
Operating Junction Temperature, TJ	-55°C (0 +125°C
Ceramic Package (D Suffix)	<165°C
Plastic Package (P Suffix)	<125°C
V _{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage (dc)	-0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	-0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	-12 mA to +5.0 mA

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

GUARANTEED OPERATING RANGES

Part Number	Suppl	y Voltage	(VCC)	Ambient Temperature (T _A)
rait isumber	Min	Nom	Max	Ambient remperature (1 _A)
 CM93422DC, PC CM93L422DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range)

C b l	Observe	4 t - 4t -	Lin	nits	11-14-	0 - 122		
Symbol	Charac	teristic	Min	Max	Units	Conditions		
VOL	Output Low Voltage		_	0.45	Vdc	V _{CC} = Min, I _{OL} = 8.0 mA		
V _{IH}	Input High Voltage	,	2.1		Vdc	Guaranteed Input High Voltage for all Inpu	ts	
VIL	Input Low Voltage		_	0.8	Vdc	Guaranteed Input Low Voltage for all Input	ts	
Iμ	Input Low Current		_	-300	μAdc	V _{CC} = Max, V _{in} = 0.4 V		
lін	Input High Current		_	40 1.0	μAdc mAdc	00		
l _{off}	Output Current (High Z)		50 -50	μAdc	V _{CC} = Max, V _{out} = 2.4 V V _{CC} = Max, V _{out} = 0.5 V			
los	Output Current Short C	rcuit to Ground	_	-70	mAdc	V _{CC} = Max (Note 2)		
Vон	Output High Voltage		2.4	_	Vdc	V _{CC} = Min, I _{OH} = -5.2 mA		
VIK	Input Diode Clamp Volta	age	_	-1.5	Vdc	V _{CC} = Max, I _{in} = -10 mA		
		MCM93422	_	130	mAdc	T _A = Max		
1	D	IVICIVI93422	_	155	mAdc	T _A = Min V _{CC} = Max,		
lcc	Power Supply Current	MCM93L422	_	75	mAdc	T _A = Max All Inputs Grounded		
		WICIVIO3L422	1 -	80	mAdc	T _A = Min		

TRUTH TABLE

		Inputs			Output	Mada
ŌĒ	CS1	CS2	WÈ	D1-D4	01-04	Mode
Х	Н	Х	X	X	High Z	Not Selected
X	Х	L	Х	X	High Z	Not Selected
X	L	Н	L	L	High Z	Write "0"
X	L	Н	L	н	High Z	Write "1"
Н	Х	X	X	X	High Z	Output Disabled
L	L	Н	Н	X	01-04	Read

- H = High Voltage Level
- L = Low Voltage Level
- X = Don't Care (High or Low)

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range)
AC TEST LOAD AND WAVEFORMS

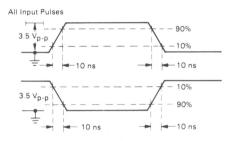
Loading Conditions

D.U.T. D_{out} 550 30 pF D.U.T. D_{out} 950 30 pF

D.U.T. Dout \$ 950

(Capacitance Includes Load B Scope and Test Fixture)

Input Pulses

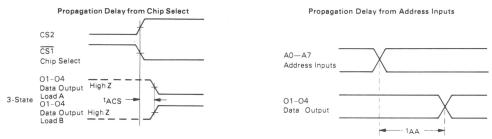


Symbol	Characteristic (Notes 2, 3, 4, 5)	MCM934	22DC,PC	MCM93L4	22DC,PC	Units	Conditions
Symbol	Characteristic (Notes 2, 5, 4, 5)	Min	Max	Min	Max	011110	Contantions
READ MODE	DELAY TIMES					ns	
tACS	Chip Select Time	_	30	_	35		See Test Circuit
†ZRCS	Chip Select to High Z	_	30	_	35		and Waveforms
tAOS	Output Enable Time	_	30	_	35		
TZROS	Output Enable to High Z	_	30	_	35		
t _{AA}	Address Access Time	_	45	_	60		
WRITE MODE	DELAY TIMES			-		ns	See Test Circuit
tzws	Write Disable to High Z	_	35	_	40		and Waveform
twR	Write Recovery Time	_	40	_	45		~
	INPUT TIMING REQUIREMENTS					ns	
tw	Write Pulse Width (to guarantee write)	30	_	45	_		See Test Circuit
twsp	Date Setup Time Prior to Write	5.0	_	5.0	_		and Waveforms
tWHD	Data Hold Time After Write	5.0	_	5.0	_		
tWSA	Address Setup Time (at tw = Min)	10	_	10	_		
tWHA	Address Hold Time	5.0	_	5.0	-		
twscs	Chip Select Setup Time	5.0	_	5.0			
tWHCS	Chip Select Hold Time	5.0	_	5.0	_		

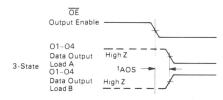
- NOTE 2: Output short circuit conditions must not exceed 1 second duration.
 - 3: The maximum address access time is guaranteed to be the worst-case bit in the memory.
 - 4: Load A used to measure transitions between logic levels and from High Z state to logic Low state. Load B used to measure transitions between High Z state to logic High state. Load C used to measure transitions from either logic High or Low state to High Z state.
 - 5: All time measurements are referenced to +1.5 Vdc except transitions into the High Z state where outputs are referenced to a delta of 0.5 Vdc from the logic level using Load C.

READ OPERATION TIMING DIAGRAM

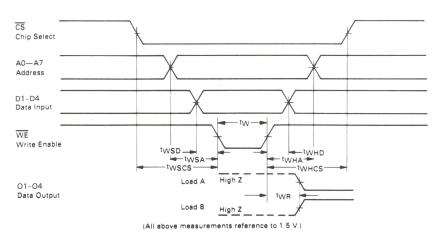
(All Time Measurements Referenced to 1.5 V)



Propagation Delay from Output Enable

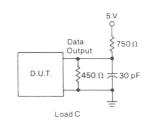


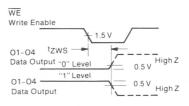
WRITE CYCLE TIMING



7

WRITE ENABLE TO HIGH Z DELAY

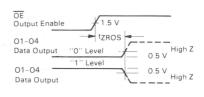




Propagation Delay from Chip Select to High Z

CS2 Chip Select CS1 Chip Select 01-04 Data Output 01-04 Data Output 11" Level 0.5 V High Z High Z

Propagation Delay from Output Enable to High Z



(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C.)

Package	θ _{JA} (Junction	n to Ambient)	θ.jc (Junction to Case)
ruckago	Blown*	Still	36 (0
D Suffix	50°C/W	85°C/W	15°C/W
P Suffix	50°C/W	85°C/W	15°C/W

^{*500} linear ft. per minute blown air



1024-BIT RANDOM ACCESS MEMORY

The MCM93425 is a 1024-bit Read/Write RAM, organized 1024 words by 1 bit.

The MCM93425 is designed for high performance main memory and control storage applications and has a typical address time of 35 ns.

The MCM93425 has full decoding on-chip, separate data input and data output lines, and an active low-chip select and write enable. The device is fully compatible with standard DTL and TTL logic families. A three-state output is provided to drive bus-organized systems and/or highly capacitive loads.

- Three-State Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed —

Access Time – 35 ns Typical Chip Select – 15 ns Typical

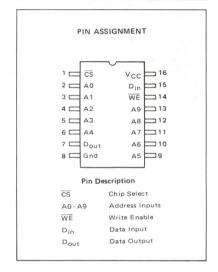
- Power Dissipation 0.5 mW/Bit Typical
- Power Dissipation Decreases With Increasing Temperature

BLOCK DIAGRAM Sense Amp and Write Drivers Word 32 X 32 Drivers Array 1 of 32 1 of 32 Decoder Decoder V_{CC} = Pin 16 4 5 6 9 10 11 Gnd = Pin 8 A1 A2 A3 A4 A5 A6 A7 A8

NOTE: Logic driving sense amp/write drivers depicts negative-only write used on C4m.

MCM93425

TTL 1024 X 1 BIT RANDOM ACCESS MEMORY



7

FUNCTIONAL DESCRIPTION

The MCM93425 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Word selection is achieved by means of a 10-bit address, A0-A9.

The Chip Select $(\overline{\text{CS}})$ input provides for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active low Write Enable (\overline{WE} , Pin 14). With \overline{WE} and \overline{CS} held

low, the data at D_{1n} is written into the addressed location. To read, \overline{WE} is held high and \overline{CS} held low. Data in the specified location is presented at D_{out} and is non-inverted.

The three-state output provides drive capability for higher speeds with capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high-impedance state.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	
Ceramic Package (D and F Suffix) Plastic Package (P Suffix)	-55°C to +165°C -55°C to +125°C
Operating Junction Temperature, TJ	
Ceramic Package (D and F Suffix)	< 165°C
Plastic Package (P Suffix)	< 125°C
V _{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage (dc)	-0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	-0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	-12 mA to +5.0 mA

TRUTH TABLE

	Inputs		Output	
cs	WE	Din	D _{out}	Mode
Н	X	X	High Z	Not Selected
L	L	L	High Z	Write "0"
L	L	Н	High Z	Write "1"
L	Н	×	Dout	Read

H = High Voltage Level

L = Low Voltage Level

X = Don't Care (High or Low)

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

GUARANTEED OPERATING RANGES (Notes 2 and 3)

	Supply Voltage (V _{CC})			
Part Number	Min	Nom	Max	Ambient Temperature (TA)
MCM93425DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
MCM93425FM, DM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

			Limi	ts					
Symbol	Charact	eristic	Min	Max	Units	Conditions			
VOL	Output Low Voltage			0.45	Vdc	V _{CC} = Min, I _{OL} = 16 mA			
VIH	Input High Voltage		2.1		Vdc	Guaranteed Input High Voltage for all Inputs			
VIL	Input Low Voltage			0.8	Vdc	Guaranteed Input Low Voltage for all Inputs			
IIL	Input Low Current			-400	μAdc	V _{CC} = Max, V _{in} = 0.4 V			
IIH	Input High Current			40	μAdc	V _{CC} = Max, V _{in} = 4.5 V			
				1.0	mAdc	V _{CC} = Max, V _{in} = 5.25 V			
loff	Output Current (High	Z)		50	μAdc	V _{CC} = Max, V _{out} = 2.4 V			
				-50		V _{CC} = Max, V _{out} = 0.5 V			
los	Output Current Short	Circuit to Ground		-100	mAdc	V _{CC} = Max			
Voн	Output High Voltage	MCM93425DC, PC	2.4		Vdc	$I_{OH} = -10.3 \text{ mA}, V_{CC} = 5.0 \text{ V} \pm 5\%$			
		MCM93425FM, DM	2.4		Vdc	I _{OH} = -5.2 mA			
V _{CD}	Input Diode Clamp Vo	Itage		-1.5	Vdc	V _{CC} = Max, I _{in} = -10 mA			
¹ CC	Power Supply Current			130	mAdc	TA = Max			
				155	mAdc	$T_A = 0^{\circ}C$ V _{CC} = Max, All Inputs Grounded			
				170	mAdc	T _A = Min			

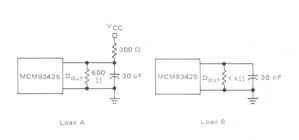
AC OPERATING CONDITIONS AND CHARACTERISTICS

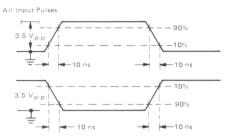
(Full operating voltage and temperature unless otherwise noted)

AC TEST LOAD AND WAVEFORMS

Loading Conditions

Input Pulses





	a 2 a1	MCM934	25DC, PC	MCM9342	25DM, FM		
Symbol	Characteristic (Notes 2, 4)	Min	Max	Min	Max	Units	Conditions
READ MODE	DELAY TIMES					ns	
†ACS	Chip Select Time		35		45		See Test Circuit
[†] ZRCS	Chip Select to High Z		35		50		and Waveforms
^t AA	Address Access Time		45		60		
WRITE MODE	DELAY TIMES					ns	
^t zws	Write Disable to High Z		35		45		See Test Circuit
^t w R	Write Recovery Time		40	10 N	50		and Waveforms
	INPUT TIMING REQUIREMENTS					ns	
t _W	Write Pulse Width (to guarantee write)	30		40			See Test Circuit
twsp	Data Setup Time Prior to Write	5		5			and Waveforms
twhD	Data Hold Time After Write	5		5			
twsa	Address Setup Time (at t _W = Min)	10		15			
^t WHA	Address Hold Time	10		10			
twscs	Chip Select Setup Time	5		5			
^t WHCS	Chip Select Hold Time	5		5			

NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air. Contact your Motorola Sales Representative if extended temperature or modified operating conditions are desired.

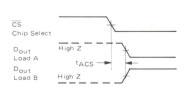
NOTE 3: Output short circuit conditions must not exceed 1 second duration.

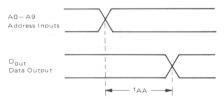
NOTE 4: The maximum address access time is guaranteed to be the worst case bit in the memory.

READ OPERATION TIMING DIAGRAM

Propagation Delay from Chip Select

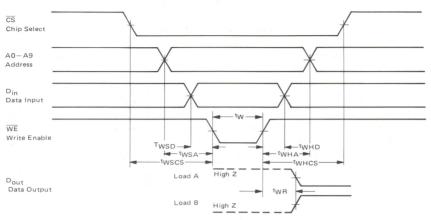
Propagation Delay from Address Inut





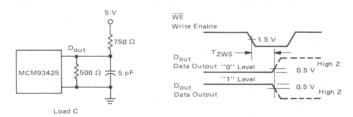
(All time measurements referenced to 1.5 V)

WRITE CYCLE TIMING

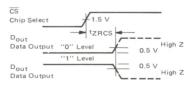


(All above measurements reference to 1.5 V)

WRITE ENABLE TO HIGH Z DELAY



Propagation Delay from Chip Select to High Z



(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C)

	θ JA (Junction to Ambient)		
Package	Blown	Still	θ JC (Junction to Case)
D Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15 ⁰ C/W
P Suffix	65°C/W	100°C/W	25°C/W

SCHOTTKY TTL



HIGH RELIABILITY

STANDARD PROGRAMS

MIL-STD-883 OPERATIONS METHOD	PROCESSING PER 5004/5005	HI-REL J		MIL-M-38510 JAN QUALIFIED
SCREEN	CLASS B METHOD	CLASS B	CLASS C	CLASS B
Internal Visual (Precap)	2010 Condition B and 38510	100%	100%	100%
Stabilization Bake	1008 Condition C or Equivalent	100%	100%	100%
Temperature Cycling	1010 Condition C	100%	100%	100%
Constant Acceleration	2001 Condition E (min.) Y ¹ Plane	100%	100%	100%
Seal (a) Fine (b) Gross	1014, Condition B 1014, Condition C	100% 100%	100% 100%	100% 100%
Interim Electrical Parameters	Per applicable device specification	Optional ¹		Optional ¹
Burn-in Test	1015 160 Hrs. @ 125° C Min. (4)	100%		100%
Final Electrical Tests (a) Static tests (1) 25°C (subgroup 1, table 1, 5005) (2) Max. and min. rated operating temp. (subgroups 2 and 3, table 1, 5005)	Per applicable device specification	100% 100% ⁽⁵⁾	100% (2)	100% 100% ⁽⁵⁾
(b) Dynamic tests and/or switching tests @ 25°C (subgroup 4 and 9, table 1, 5005)		100%	(2)	100%
(c) Functional test @ 25°C (subgroup 7, table 1, 5005)		100%	100%	100%
Qualification or Quality Conformance Inspection	5005	Group A ³	Group A ³	per 38510 ³
External Visual	2009	100%	100%	100%

- 1. When specified in the applicable device specification, 100% of the devices shall be tested at Manufacturer's option.
- 2. Sample at Group A.
- 3. Full 5005 Conformance testing performed on Jan qualified product. Group A performed on Motorola HI-REL JEDEC processed product with either Generic or group B, C, D testing available.
- 4. Optional 0.44 eV time-temperature "equivalent" burn-in per Figure 1015-1.

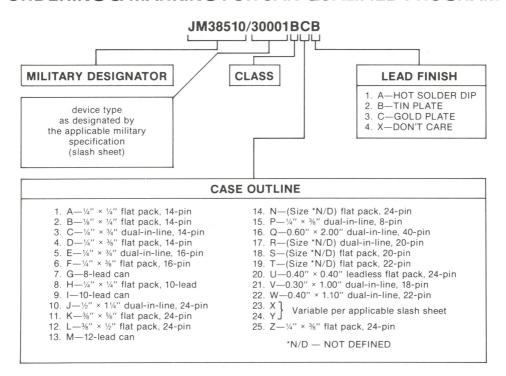
 5. AC sample testing at +125°C and -55°C on those types which require subgroup 10 and 11 testing per MIL-M-38510. Slash Sheet Specifications.
- 6. Devices Processed to earlier HI-REL "SNC" and "SNJ" program still available contact nearest Motorola Sales Office for ordering information.

LOW POWER SCHOTTKY INTEGRATED CIRCUITS

ORDERING & MARKING FOR JEDEC HI-REL PROCESSING PROGRAM

54LS00	/	B	C	В	JC
†	†	†	†	†	1
Device	Slash	Device	Case	Lead	JEDEC
Type		Class	Outline	Finish	Designator

ORDERING & MARKING FOR JAN QUALIFIED PROGRAM





The "BETTER" program is offered on TTL/LS, in dual-in-line ceramic and plastic packages.

Motorola's reliability and quality-enhancement program was developed to provide improved levels of quality and reliability for standard commercial products.

Motorola standard commercial integrated circuits are manufactured under stringent inprocess controls and quality inspections combined with the industries' finest outgoing quality inspections. The "BETTER" program offers three levels of extra processing, each tailored to meet different user needs at nominal costs.

The program is designed to:

- Eliminate incoming electrical inspection
- Eliminate need for independent test labs and associated extra time and costs
- · Reduce field failures
- Reduce service calls
- · Reduce equipment downtime
- · Reduce board and system rework
- Reduce infant mortality
- Save time and money
- Increase end-customer satisfaction

BETTER PROCESSING — STANDARD PRODUCT PLUS:

LEVEL I (Suffix S)

- 100% temperature cycling per MIL-STD-883. Method 1010C, ten cycles from — 65°C to+150°C.
- 100% functional and dc parametric tests at maximum rated temperature

LEVEL II (Suffix D)

- 100% burn-in to MIL-STD-883 test conditions — 160 hours at +125°C or 1.0 eV Arrhenius time/temperature equivalent.
- 100% post burn-in functional and dc parametric tests at 25°C (or max rated T_A at Motorola's option).

LEVIL III (Suffix DS)

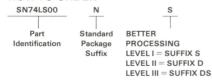
 Combination of Levels I and II above. (Post burn-in functional and dc parametric tests at maximum rated temperature.)

"BETTER" AOL GUARANTEES

TEST	CONDITION		AQL1	
	00110111011	LEVEL I	LEVEL II	LEVEL III
HIGH TEMPERATURE FUNCTIONAL	$T_A = MAX$	0.078		0.078
DC PARAMETRIC	T _A = 25°C	0.078	0.078	0.078
DC PARAMETRIC	T _A MIN, T _A MAX	0.39	0.39	0.39
AC PARAMETRIC	T _A = 25°C	0.078	0.078	0.078
EXTERNAL VISUAL AND MECHANICAL	MAJOR/MINOR	0.078	0.078	0.078
HERMETICITY (NOT APPLICABLE TO PLASTIC PACKAGES)	GROSS/FINE	0.15	0.15	0.15

 "AQL" values shown are for references only—"LTPD" type sampling plans are used that are equal to or tighter than values indicated. Also, the guaranteed electrical and visual/mechanical AQL levels will be tightened each guarter through 1985. Contact nearest Motorola sales office for latest values.

HOW TO ORDER

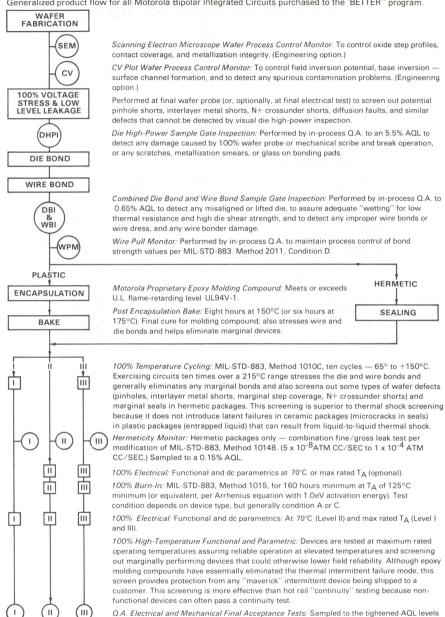


PART MARKING

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

GENERALIZED PRODUCT FLOW

Generalized product flow for all Motorola Bipolar Integrated Circuits purchased to the 'BETTER' program.



CC/SEC). Sampled to a 0.15% AQL.

нм

SHIPPING

Hermeticity Monitor: Hermetic packages only. Combination fine/gross leak test per modification of MIL-STD-883, Method 1014B (5×10^{-8} ATM CC/SEC to 1×10^{-4} A

"RAP" RELIABILITY AUDIT PROGRAM for BIPOLAR DIGITAL INTEGRATED CIRCUITS

1.0 INTRODUCTION

In January, 1977, Motorola Bipolar Digital Reliability Engineering implemented "RRAP" (Rapid Reliability Assessment Program) to provide rapid assessment of the reliability of newly introduced TTL Low-Power Schottky (LS) devices. This RRAP concept permits rapid feedback of information on any reliability problems to the Product Engineering group so that corrective action can be quickly implemented. The RRAP program is performed by the Reliability Engineering Department on samples submitted by Product, Process, or Package Engineering for obtaining a rapid look at the reliability of new products, processes, or packages. This program has been extended to standard ALS, 74F (FAST), TTL, TTL Memories, MDTL, MHTL, MECL III, MECL 10K and 10KH, MECL Memories, Macrocell Arrays, and Phase Lock Loop (PLL) product families. The details of the RRAP program are outlined in Section 2.0

In March, 1977, an addition was made to the RRAP program for the purpose of auditing the reliability of outgoing TTL Low-Power Schottky (LS) product. This audit, called the Reliability Audit Program ("RAP"), is performed weekly by the Quality Assurance Group and reported monthly by Bipolar Digital Reliability Engineering. The details of this "RAP" program are outlined in Section 3.0.

2.0 RAPID RELIABILITY ASSESSMENT PROGRAM (RRAP)

2.1 Hermetic Packaged Devices (50 Units minimum per Evaluation Sample)

- Electrical I (initial rejects removed from test)
- Temp Cycling -100 cycles (-65°C/+150°C) per Method 1010C
- Electrical I (plus Hermeticity per Method 1014 B & C for package evaluations only)
- "Equivalent" Burn-In for 40 hrs at 145°C per Method 1015 A or C
- Electrical I

2.2 Plastic Packaged Devices (100 Units minimum per Evaluation Sample)

S/G 1 (30 Units)

a. Electrical I

- b. Thermal Shock -200 cycles (-55°C/+125°C -30 Sec. dwell) Method 1011B, modified
- c. Electrical I

S/G 2 (40 Units)

- a. Electrical I
- b. 16 hrs, PTHB; Rated V_{CC} (15 psig, b. Temp Cycling -100 cycles 100%RH, 121°C) Motorola test method
- c. Electrical I

S/G 3 (30 Units)

- a. Electrical I
- (-65°C/+150°C). Method 1010C
- c. Electrical I
- d. "Equivalent" Burn-In (40 hrs @ 145°C) per Method 1015 A or C
- e. Electrical I

NOTES:

- 1. All tests per MIL-STD-883 unless stated otherwise.
- 2. Electrical I = DC @ 25°C and functional @ 25°C Go/No/Go
- 3. 40 hr/145°C burn-in is "equivalent" to 160 hr/125°C burn-in using 1.0 eV activation energy and the Arrhenius equation for determining acceleration factor.
- 4. 16 hrs of PTHB testing is equivalent to approximately 800 hrs of standard 85°C/85% RH THB testing for $V_{CC} \le 15 \text{ V}$, based on comparative tests performed by Motorola Reliability Engineering.
- 5. For each evaluation, the goal is zero failures. Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis. Results of evaluation, along with analysis of any failure(s), are reviewed promptly with responsible design, product, process and package engineers.

3.0 RELIABILITY AUDIT PROGRAM (RAP) (per Motorola specification 12 MRM15301A)

- 3.1 PTHB 15 psig/121°C/100% RH at rated V_{CC} for 16 hours performed on a weekly basis 0 rejects allowed out of 45 devices. (To be performed on plastic encapsulated devices only.) 48 hours read out included for reliability engineering information only.
- 3.2 Temp Cycling MIL-STD-833, Method 1010, 1000 cycles, Condition C, —65°C/+150°C. Interim readout at 100 cycles (plastic and hermetic packages). Sample pulled on weekly basis 0 rejects allowed out of 45 devices after 100 cycles; 1 reject allowed out of 45 devices after 1000 cycles.
- 3.3 Op. Life Test MIL-STD-883, Method 1005, Condition A (Reverse Bias) or C (Power plus Reverse Bias), T_A = 145°C; readouts at 40 hrs and 250 hrs (plastic and hermetic packages). Sample pulled on weekly basis 1 reject allowed out of 55 devices at 40 hr readout. No additional rejects allowed at 250 hrs. If no rejects at 40 hrs, 1 reject allowed at 250 hrs.
- 3.4 Report Monthly Reliability Engineering computer printout summarizing test results.

NOTES

- All standard 25°C dc and functional parameters will be measured Go/No/Go at each readout
- Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis.
- If both plastic and hermetic packages are available, package type will be alternated weekly
- Device types sampled will be by generic type within each digital I/C product family (MDTL, MTTL, MTTL-LS, etc.) and will include all major package assembly options (U/S bond, TC bond, ball bond, T.A.B., etc.) and all assembly locations (Korea, Malaysia, etc.).
- 5. 16 hrs PTHB is equivalent to approximately 800 hrs of 85°C/85% RH THB for VCC \leqslant 15 V.
- 6. Only moisture related failures (like corrosion) are criteria for failure on PTHB test.
- 40 hr/145°C Op Life is equivalent to 160 hr/125°C using 1.0 eV in Arrhenius equation.
- 8. 250 hrs/145°C Op Life is equivalent to 1000 hrs/125°C using 1.0 eV in Arrhenius equation
- Special device specifications (48A's) for digital products will reference 12MRM15301A as source of generic data for any customer required monthly audit reports.

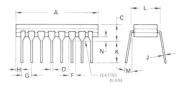
SCHOTTKY TTL



CERAMIC DUAL IN-LINE

Case 620-08 16-Pin Ceramic Dual In-Line





	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
А	19.05	19.94	0.750	0.785
В	6.10	7.49	0.240	0.295
C		5.08	-	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54	BSC	0.100 BSC	
Н	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62	7.62 BSC		BSC
M	-	150	-	15 ⁰
N	0.51	1.02	0.020	0.040

- LEADS WITHIN 0.13 mm (0.005) RADIUS
 OF TRUE POSITION AT SEATING PLANE
 AT MAXIMUM MATERIAL CONDITION.
 PACKAGE INDEX: NOTCH IN LEAD
 NOTCH IN CERAMIC OR INK DOT.
 JOHN "L" TO CENTER OF LEADS WHEN
 FORMED PARALLEL.

- 4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT. 5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

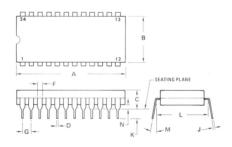


CASE 620-08

NOTES

- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 2. LEADS WITHIN 0.13 mm
- (0.005) RADIUS OF TRUE
 POSITION AT SEATING PLANE
 AT MAXIMUM MATERIAL
 CONDITION. (WHEN FORMED PARALLEL).

Case 623-05 24-Pin Ceramic Dual In-Line



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	31.24	32.77	1.230	1.290
В	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54	BSC	0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24		0.600	
M	00	15 ⁰	00	150
N	0.51	1.27	0.020	0.050

CASE 623-05

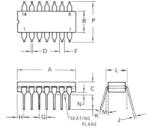


- UTES:

 1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.

 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 3. DIMENSION "A" AND "B" (632-07) DO NOT INCLUDE GLASS RUN-DUT.
 4. LEADS WITHIN 0.25 mm (0.010) DIA
- OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

Case 632-07 14-Pin Ceramic Dual In-Line



	MILLIM	ETERS	INCHES	
DIM	MIN	MAX	MIN	MAX
Α	19.05	19.94	0.750	0.785
В	6.10	7.49	0.240	0.295
C	-	5.08	-	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54	BSC	0.100 BSC	
Н	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300	BSC
M	-	150		150
N	0.51	1.02	0.020	0.040

CASE 632-07

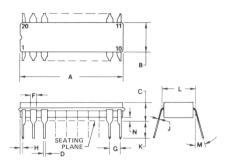
CERAMIC DUAL IN-LINE (continued)

Case 732-03 20-Pin Ceramic Dual In-Line



NOTES:

- TES:
 1. LEADS WITHIN 0.25 mm (0.010)
 DIA, TRUE POSITION AT
 SEATING PLANE, AT MAXIMUM
- MATERIAL CONDITION.
 2. DIM L TO CENTER OF LEADS
 WHEN FORMED PARALLEL.
 3. DIM A AND B INCLUDES
- MENISCUS.



	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	23.88	25.15	0.940	0.990
В	6.60	7.49	0.260	0.295
С	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54	BSC	0.100 BSC	
Н	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62		0.30	0 BSC
M	00	15 ⁰	00	150
N	0.25	1.02	0.010	0.040

CASE 732-03



- 1. DIM A- IS DATUM.

 2. POSITIONAL TOL FOR LEADS:

- 2. PUSHTUNAL TULL FUR LEADS:

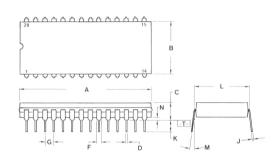
 (♣ Ø 0.25 (0.010) ③ T A ③

 3. TT IS SEATING PLANE.

 4. DIM A AND B INCLUDES MENISCUS.

 5. DIM -L- TO CENTER OF LEADS
 WHEN FORMED PARALLEL.

 6. DIMENSIONING AND TOLERANCING
- PER ANSI Y14.5, 1973



Case 733-02 28-Pin Ceramic Dual In-Line

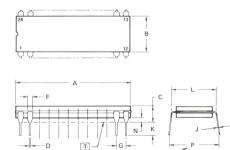
	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	36.45	37.85	1.435	1.490
В	12.70	15.37	0.500	0.605
С	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54	BSC	0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.54	4.06	0.100	0.160
L	15.24	15.24 BSC		DBSC
M	50	15 ⁰	50	150
N	0.51	1.27	0.020	0.050
L	15.24 50	BSC 150	0.600 50	15

CASE 733-02

NOTES

- OTES:
 1. DIMENSION A IS DATUM.
 2. POSITIONAL TOLERANCE
 FOR LEADS: 24 PLACES

 1. IN 15 SEATING PLANE.
 3. IT 15 SEATING PLANE.
 4. DIMENSION L TO CENTER OF
 LEADS WHEN FORMED PARALLEL.
 5. DIMENSIONING AND TOLERANCING
 PER ANSI Y14.5, 1973.



INSIDE OF LEADS

Case 758-01 24-Pin Ceramic Dual In-Line

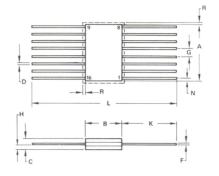
	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	31.50	32.64	1.240	1.285
В	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.57	0.045	0.062
G	2.54	BSC	0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
P	9.14	10.16	0.360	0.400

CASE 758-01

CERAMIC FLATPAK

Case 650-03 16-Pin Ceramic Flatpak





	MILLIN	ETERS	INCHES	
DIM	MIN	MAX	MIN	MAX
Α	9.40	10.16	0.370	0.400
В	6.22	7.24	0.245	0.285
C	1.52	2.03	0.060	0.080
D	0.41	0.48	0.016	0.019
F	0.08	0.15	0.003	0.006
G	1.27	BSC	0.050 BSC	
Н	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	-	0.745	-
N	-	0.51	-	0.020
R	-	0.38	-	0.015

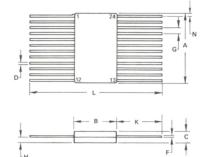
CASE 650-03

- NOTES: 1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.

 - LEADS WITHIN 0.13 mm (0.005)
 TOTAL OF TRUE POSITION AT
 MAXIMUM MATERIAL CONDITION.

Case 652-02 24-Pin Ceramic Flatpak





	MILLIN	METERS	INCHES	
DIM	MIN	MAX	MIN	MAX
Α	14.99	15.49	0.590	0.610
В	9.27	9.91	0.365	0.390
C	1.27	2.03	0.050	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27	BSC	0.050	BSC
Н	0.69	1.02	0.027	0.040
K	6.35	9.40	0.250	0.370
L	21.97	1	0.865	-
N	0.25	0.63	0.010	0.025

CASE 652-02

NOTE:

1. LEADS WITHIN 0.25 mm (0.010)

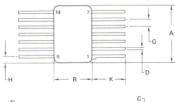
TOTAL OF TRUE POSITION AT

MAXIMUM MATERIAL CONDITION

Case 717-02 14-Pin Ceramic Flatpak









	MILLIN	METERS	INCHES	
DIM	MIN	MAX	MIN	MAX
Α	-	9.91	-	0.390
В	-	6.73	-	0.265
C	-	2.03	0.060	0.080
D	0.38	0.48	0.015	0.019
F	-	0.25	-	0.010
G	1.27	BSC	0.050 BSC	
Н	0.38	0.89	0.015	0.035
J	0.08	0.15	0.003	0.006
K	-	8.26	-	0.325
N	0.64	0.89	0.025	0.035

CASE 717-02

NOTES:

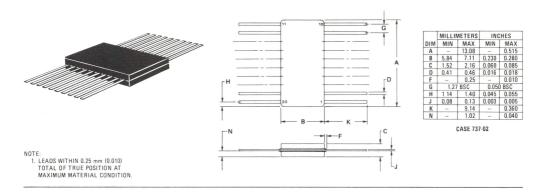
- IOTES:
 1. DIM "F" IS FOR GLASS OVERRUN.
 2. LEADS, TRUE POSITIONED WITHIN
 0.25 mm (0.010) DIA TO DIM "A"
 8. "8" AT MAXIMUM MATERIAL
 CONDITION.

q

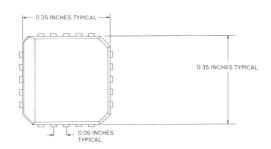
PACKAGE OUTLINES

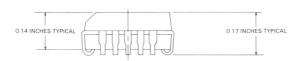
CERAMIC FLATPAK (continued)

Case 737-02 20-Pin Ceramic Flatpak



QUAD PLASTIC CHIP CARRIER





PLASTIC

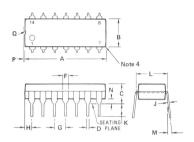
Case 646-05 14-Pin Plastic



NOTES:

- IOTES:

 1. LEADS WITHIN 0.13 mm
 (0.005) RADIUS OF TRUE
 POSITION AT SEATING
 PLANE AT MAXIMUM
 MATERIAL CONDITION.
 2. DIMENSION "L" TO
 CENTER OF LEADS
 WHEN FORMED
 PARALLEL.
 3. DIMENSION "B" DOES NOT
 INCLUDE MOLD FLASH.
 4. ROUNDED CORNERS OPTIONAL.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	18.16	19.56	0.715	0.770
В	6.10	6.60	0.240	0.260
С	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
Н	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	00	100	00	100
N	0.51	1.02	0.020	0.040

CASE 646-05

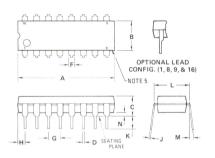


- NOTES:

 1. LEADS WITHIN 0.13 mm
 (0.005) RADIUS OF TRUE
 POSITION AT SEATING
 PLANE AT MAXIMUM
 MATERIAL CONDITION.
 2. DIMENSION "L" TO
 CENTER OF LEADS
 WHEN FORMED
- WHEN FURMED
 PARALLEL.
 3. DIMENSION "B" DDES NOT
 INCLUDE MOLD FLASH.
 4."F" DIMENSION IS FOR FULL
 LEADS. "HALF" LEAD POSITIONS
 1.2.0 a.d.15\] 1, 8, 9, and 16).

 5. ROUNDED CORNERS OPTIONAL.



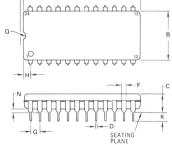


	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	18.80	21.34	0.740	0.840	
В	6.10	6.60	0.240	0.260	
C	4.06	5.08	0.160	0.200	
D	0.38	0.53	0.015	0.021	
F	1.02	1.78	0.040	0.070	
G	2.54	2.54 BSC 0.100 BSC		BSC	
Н	0.38	2.41	0.015	0.095	
J	0.20	0.38	0.008	0.015	
K	2.92	3.43	0.115	0.135	
L	7.62 BSC		0.300	BSC	
M	00	100	00	100	
N	0.51	1.02	0.020	0.040	

CASE 648-05

Case 649-03 24-Pin Plastic







	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	31.50	32.13	1.240	1.265
В	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
Н	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	-	10 ⁰	-	100
N	0.51	1.02	0.020	0.040
Р	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:

1. LEADS WITHIN 0.13 mm (0.005)
RADIUS OF TRUE POSITION AT
SEATING PLANE AT MAXIMUM
MATERIAL CONDITION.

2. DIMENSION "L" TO CENTER OF
LEADS WHEN FORMED PARALLEL.

Case 710-02 28-Pin Plastic

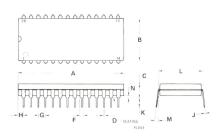


NOTES:

- POSITIONAL TOLERANCE OF LEADS (D),
 SHALL BE WITHIN 0.25mm(0.010) AT
 MAXIMUM MATERIAL CONDITION, IN
 RELATION TO SEATING PLANE AND
- EACH OTHER.

 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

 3. DIMENSION B DOES NOT INCLUDE
- MOLD FLASH.



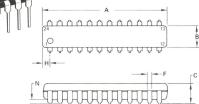
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	36.45	37.21	1.435	1.465
В	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54	1 BSC	0.100	BSC
Н	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24	BSC	0.600	BSC
M	00	150	00	150
N	0.51	1.02	0.020	0.040

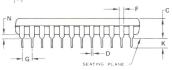
CASE 710-02

Case 724-02 24-Pin Plastic



1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM D).







	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	31.24	32.13	1.230	1.265
В	6.35	6.86	0.250	0.270
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
Н	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	-	100	-	100
N	0.51	1.02	0.020	0.040

CASE 724-02

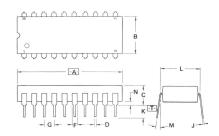
Case 738-01 20-Pin Plastic



NOTES

- 1. DIM A. IS DATUM. 2. POSITIONAL TOL FOR LEADS; ♦ Ø 0.25 (0.010)⊛ T A⊛

- TIS EAST INCUINED | AND |
 3. T. IS SEATING PLANE.
 4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
 5. DIM TO CENTER OF LEADS WHEN FORMED PARALLEL.
 6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	25.65	27.18	1.010	1.070
В	6.10	6.60	0.240	0.260
C	3.94	4.19	0.155	0.165
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	00	150	00	150
N	0.51	1.02	0.020	0.040

CASE 738-01

- Selection Information LS/ALS/FAST
- 2 Circuit Characteristics
- Design Considerations

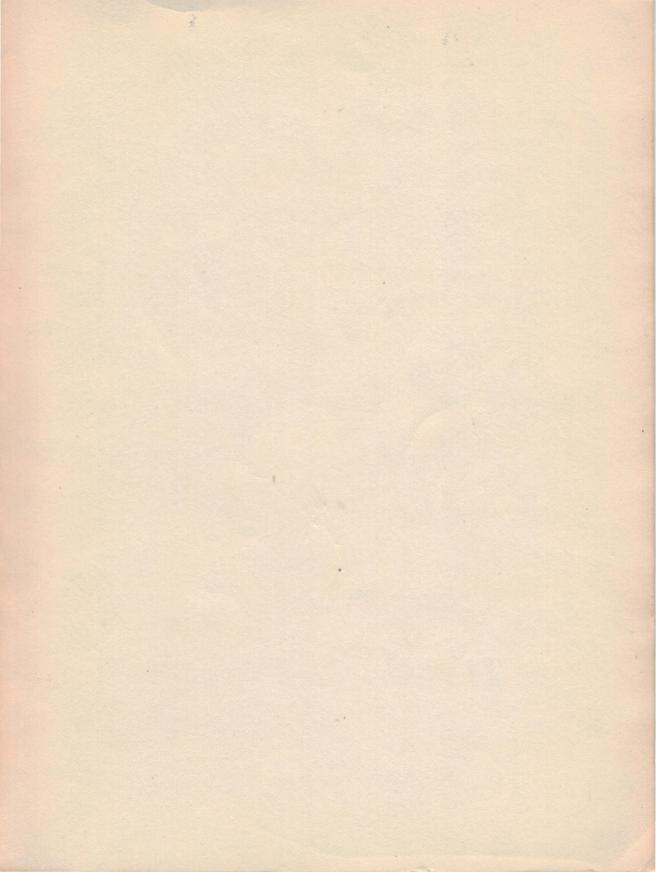
 Symbol Definitions and Testing
- 4 LS Data Sheets
- 5 ALS Data Sheets

6

- **FAST Data Sheets**
- 7 RAM/PROM Data Sheets
- 8 Reliability Data
- 9 Package Outlines

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